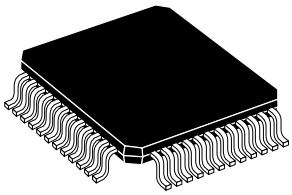
ST75951

V.34/56K ANALOG FRONT END

- V.34/56K MODEM ANALOG FRONT-END (AFE)
- 16 BITS OVERSAMPLING SIGMA DELTA A/D AND D/A CONVERTERS
- 85dB DYNAMIC RANGE
- PROGRAMMABLE SAMPLING FREQUENCY
- AUXILIARY ANALOG INPUT
- MODEM SIDE OF SILICON DATA ACCESS ARRANGEMENT (DAA) INTEGRATED WITH AFE
- KRYPTON ISOLATION INC. PATENTED TECHNOLOGY ELIMINATE TRANSFORMER OR LINEAR OPTO-COUPLERS
- RING DETECT, LINE IN USE, CLID AND OVER LOOP CURRENT DETECT
- 4 GPIO ASSOCIATED WITH 1 GENERAL PURPOSE INTERRUPT OUTPUT
- ANALOG AND DIGITAL LOOP-BACK MODE
- SYNCHRONOUS SERIAL INTERFACE FOR PROCESSORS DATA EXCHANGE
- ON CHIP REFERENCE VOLTAGE
- SINGLE POWER SUPPLY RANGE : 2.7V TO 5.25V
- LOW POWER CONSUMPTION : 40mW @ 3.3V
- TQFP48 PACKAGE
- 0.5µM CMOS PROCESS



TQFP48 (7 x 7 x 1.4mm)
(Full Plastic Quad Flat Pack)

ORDER CODE : ST75951

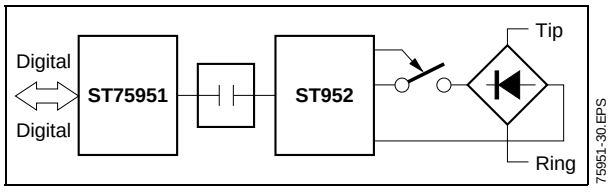
DESCRIPTION

ST75951 is an analog front-end designed to implement modems application up to 56Kbps.

ST75951 interfaces between DSP or HSP signals and capacitive isolation barrier.

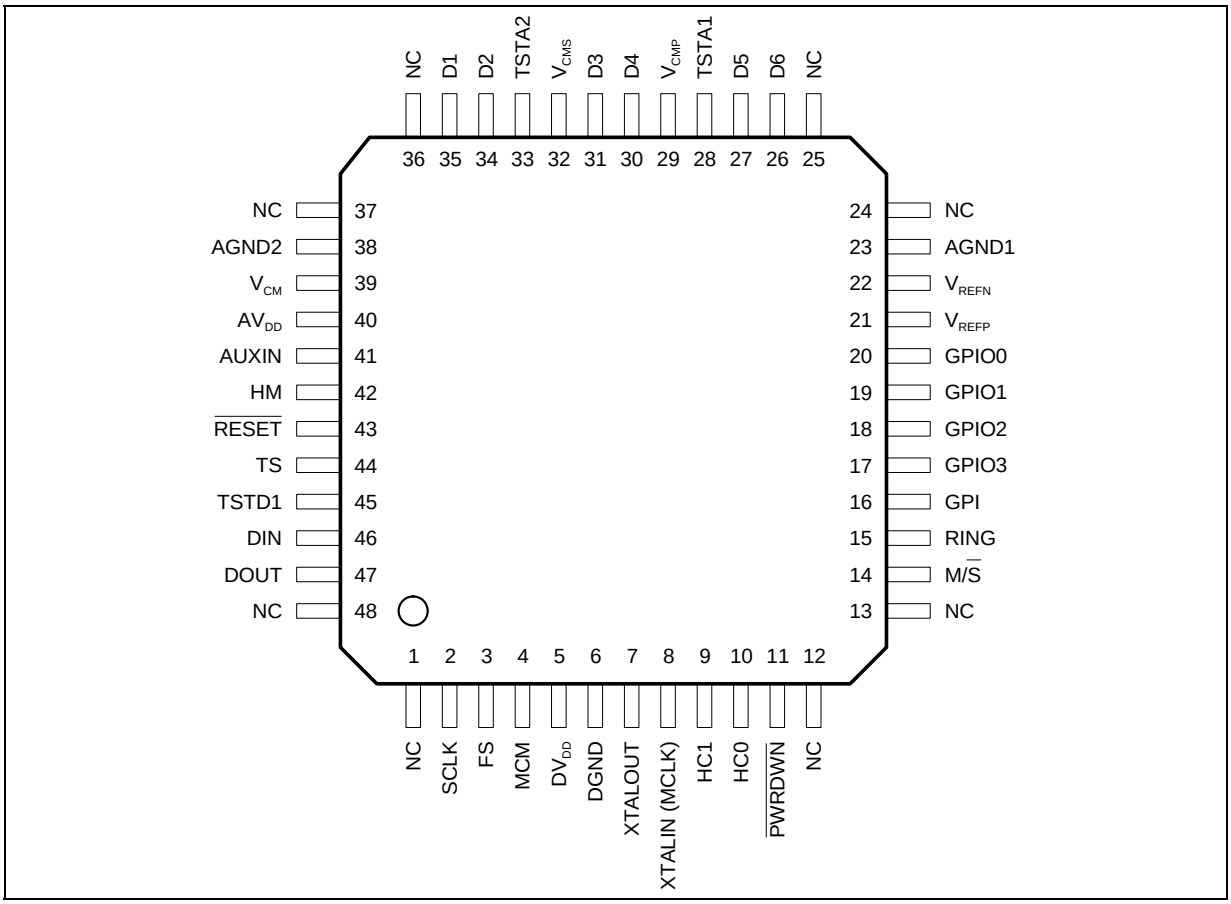
A complete D.A.A. is made with ST952 which interfaces between capacitive isolation barrier and the telephone line.

Figure 1



It integrates a high resolution A/D and D/A converter and incorporates Krypton Isolation Inc. patented silicon D.A.A. technology.

PIN CONNECTIONS



PIN LIST

Pin Number	Name	Type	Description
2	SCLK	O	Bit Shift Clock Output , SCLK = Coeff · FS
3	FS	I/O	Frame Synchronization Input (Slave)/Output (Master)
4	MCM	I	Master Clock Mode
5	DV_{DD}	I	Positive Digital Power Supply
6	DGND	I	Digital Ground (0V) (see Note1)
7	XTALOUT	O	Crystal Output
8	XTALIN	I	Crystal Input
9	HC1	I	Hardware Control Input
10	HC0	I	Hardware Control Input
11	$\overline{PWRDWN}$	I	Power Down Input
14	M/$\overline{S}$	I	Master/slave Control Input
15	RING	O	Ring Detect Output
16	GPI	O	General Purpose Interrupt Output
17	GPIO3	I/O	General Purpose Control Input/Output
18	GPIO2	I/O	General Purpose Control Input/Output
19	GPIO1	I/O	General Purpose Control Input/ Output
20	GPIO0	I/O	General Purpose Control Input/Output
21	V_{REFP}	O	Positive Reference Voltage
22	V_{REFN}	O	Negative Reference Voltage
23	AGND1	I	Analog Ground (0V) (see Note1)
26	D6	O	ST952 Control Output
27	D5	O	ST952 Control Output
28	TSTA1	O	Reserved for test
29	V_{CMP}	I	Common Mode Voltage Input P
30	D4	I	Receive Input
31	D3	I	Receive Input
32	V_{CMS}	I	Common Mode Voltage Input S
33	TSTA2	O	Reserved for test
34	D2	O	Transmit Output
35	D1	O	Transmit Output
38	AGND2	I	Analog Ground (0V) (see Note1)
39	V_{CM}	O	Common Mode Voltage Output
40	AV_{DD}	I	Positive Analog Power Supply
41	AUXIN	I	Receive Auxiliary Analog Input Amplifier
42	HM	I	Hardware Control Input for Clid/Off-hook
43	$\overline{RESET}$	I	Reset Function to initialize the device
44	TS	I	Timeslot Control Input
45	TSTD1	I	Reserved for Test (must be grounded in normal mode)
46	DIN	I	Serial Data Input
47	DOUT	O	Serial Data Output

75951-01.TBL

Note 1 : Digital and Analog ground must be connected externally together.

PIN DESCRIPTION

1 - Power Supply (5 Pins)

1.1 - Power Supply (AV_{DD}, DV_{DD})

These pins are the positive analog and digital power supply input (2.7 to 5.25V).

In any case, the AV_{DD} voltage must always be higher or equal to the DV_{DD} voltage ($AV_{DD} \geq DV_{DD}$).

1.2 - Analog Ground (AGND1, AGND2)

These pins are the ground return of the DAC and ADC analog section.

1.3 - Digital ground (DGND)

This pin is the ground return of the digital circuitry.

Note : In order to obtain published performances, the analog AV_{DD} and digital DV_{DD} should be decoupled with respect to analog ground and digital ground, respectively. Decoupling capacitors should be as close as possible to the supplies pins. All ground must be tied together. In the following section the ground is referred as : GND.

2 - Serial Synchronous Interface (4 Pins)

2.1 Data (DIN, DOUT)

Digital data word input/output of the SSI (16 bits data).

2.2 - Frame Synchronization (FS)

The frame synchronization is used to indicate that the device is ready to send and receive data.

The data transfer begins on the falling edge of frame-sync signal. The frame-SYNC can be generated internally or externally.

2.3 Serial Bit Clock (SCLK)

Clocks the digital data into DIN and out of DOUT during the frame synchronization interval. The serial bit clock is generated internally and equal to MCLK/R (R programmed value in register 3). The serial bit clock is a multiple of FS.

3 - Control Pins (10 Pins)

3.1 - Reset ($\overline{\text{RESET}}$)

This pin initializes the internal counters and control registers to their default value. A minimum low pulse of 100ns is required to reset the chip.

3.2 - Power-Down ($\overline{\text{PWRDWN}}$)

This input powers down the entire chip. In power down mode the existing internally programmed state is maintained. When power down is driven high, full operation resumes after 1ms.

A software powerdown with wake-up on ring detect is also provided with bit 4 in control register 3.

3.3 - Hardware Control (HC0, HC1)

These pins are used for hardware/software control programmation of the device.

3.4 - Hardware Control (HM)

This pin is used for hardware/software control of CLID/OFFHOOK function.

3.5 - Master/Slave (M/$\overline{S}$)

When M/$\overline{S}$ = " 1 " the device is in master mode and FS is generated internally otherwise the device is in slave mode and Fs must be provided externally and equal to SCLK*R / OVER.

3.6 - Timeslot Control (TS)

When TS = " 0 " the data are assigned to the first timeslot (1st 16 bits after falling edge of FS) otherwise the data are on the second timeslot (bits 17 to 32).

3.7 - Control (D5, D6)

These pins transmit the control signals trough isolation capacitors to ST952 which converts and outputs the appropriate control signals.

3.8 - Master Clock Mode (MCM)

When MCM = " 1 ", we have
FS = Master Clock/[M · Q · OVER] otherwise we have FS = Master Clock/OVER and the M, Q dividers are bypassed.

4 - General Purpose Input/Output Circuitry

4.1 - GPIO (4 Pins)

ST75951 offers 4 general purpose Input/Output pins. The setting of the GPIO configuration is done through the control register 1 and the signal level of the GPIO are reflected in the feedback register 2.

At power on the GPIO are programmed as inputs.

In order to take into account the evolution of ST952, thanks to the control register we will be able to send a clock signal equal to F0/N (N programmed in register 2) on GPIO0 and F0 on GPIO3.

When in DAA control hardware mode HM = 1, the CLID and OFF-HOOK control is done by Pin GPIO1 (CLID) and GPIO2 (OFF-HOOK), otherwise when HM = 0 then the CLID/OFF-HOOK control is done by programming the adequate bit in the control register 3 (Bit 2 , Bit 3, see Table 7).

PIN DESCRIPTION (continued)

4.2 - General Purpose Interrupt System (GPI)

The GPI will reflect any change of the GPIO'S inputs or RING output when non-masked, so the processor does not need to read the output control word continuously. GPI level change tells the processor, one of the non-masked input pins level has changed and he can read the control word. So GPIO could extend the number of interrupt pins of the processor.

5 - Ring

This pin is used for the Ring detect but also reports the Line status, current limit.

6 - Digital Test Pin (TSTD1)

This pin is reserved for digital test purpose.

7 - Crystal (XTALIN , XTALOUT)

These pins must be tied to an external crystal or a master clock generator (MCLK).

8 - Analog Interface (12 Pins)

8.1 - DAC and ADC Reference Voltage Output (V_{REFP}, V_{REFN})

These pins provide the positive and negative reference Voltage used by the 16-bit converters. The reference voltage, V_{REF}, is the voltage difference between the V_{REFP} and V_{REFN} outputs.

V_{REFP} and V_{REFN} should be externally decoupled with respect to V_{CM}.

8.2 - Common Mode Voltage Output (V_{CM})

This output pin is the common mode voltage (AV_{DD} - AGND)/2 . This output must be decoupled with respect to GND.

8.3 - Common Mode Voltage Input (V_{CMP}, V_{CMS})

These input pins are the common mode voltage for internal circuitry. They have to be connected externally to V_{CM}.

8.4 - Analog Transmit Output (D1 ,D2)

These pins are the output of the fully differential converted analog signal, modulated at F0 (1MHz < F0 < 1.7MHz).

The digital data IN signal is converted in analog signals (with (Sin X)/X compensation). Two ranges of signal amplitude have to be considered ; modem application with dynamic up to $2.5V_{PP}$ with maximum performances SNDR = 83dB, voice application with dynamic up to $3.2V_{PP}$ differential (SNDR = 75dB).

The transmit output stage can be programmed to +2dB gain, 0db gain, 6dB or infinite attenuation.

8.5 - Analog Receive Inputs (D3, D4)

These pins are the differential analog inputs. These analog inputs are presented to the F0 demodulator and the sigma-delta modulator. The analog input peak-to-peak differential signal range must be less than 2.5 V_{PP}. The gain of the receive stage is programmable to 0dB or 6dB.

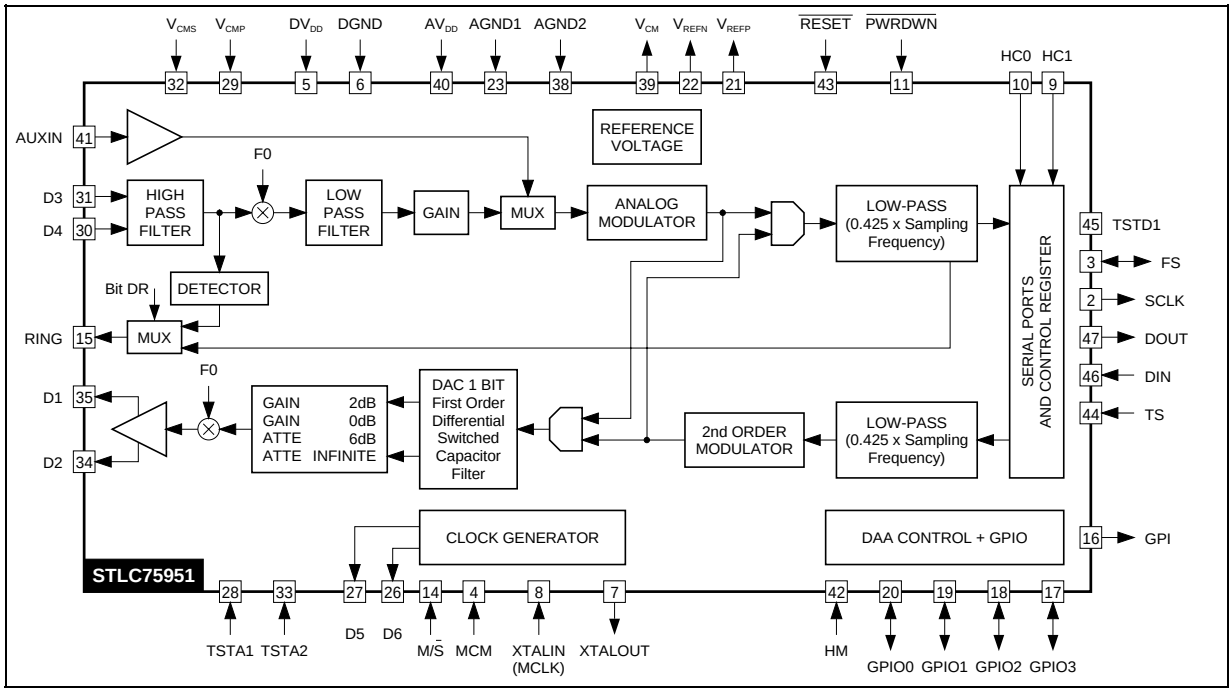
8.6. - Analog Test Pin (TSTA1, TSTA2)

These pins are reserved for analog test purpose.

8.7 Analog Auxiliary Receive Inputs (AUXIN)

This pin is the auxiliary analog input. This analog input is presented to the analog modulator. The analog input peak-to-peak signal range must be less than 1.25 V_{PP}. The gain of the receive stage is 0dB.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

ST75951 is a modem AFE front-end integrating the modem side of Krypton K951 and fully compatible to work with ST952.

1 - Transmit Section

The functions included in the transmit section are :
- D/A converter,
- F0 modulator,
- Programmable stage +2dB gain, 0dB gain, 6dB attenuation or infinite attenuation,
- Transmit Filter including noise shaper and Sinx/x correction.

The digital base Band data (DIN) are converted and modulated at F0 and send differentially (D1, D2) to ST952 through capacitive connection.

2 - Receive Section

The functions included in the receive section are :
- Main and Aux inputs,
- Programmable gain 0/6dB,
- A/D converter,
- F0 demodulator,
- Receive filter.

The analog differential Main input signal (D3, D4) coming from ST952 is demodulated at F0, goes to the multiplexer and gain receive block then is digitally converted and output on DOUT which is the base band data.

Thanks to the multiplexer, we can also process base band analog signal on AUXIN.

3 - Clock Generator

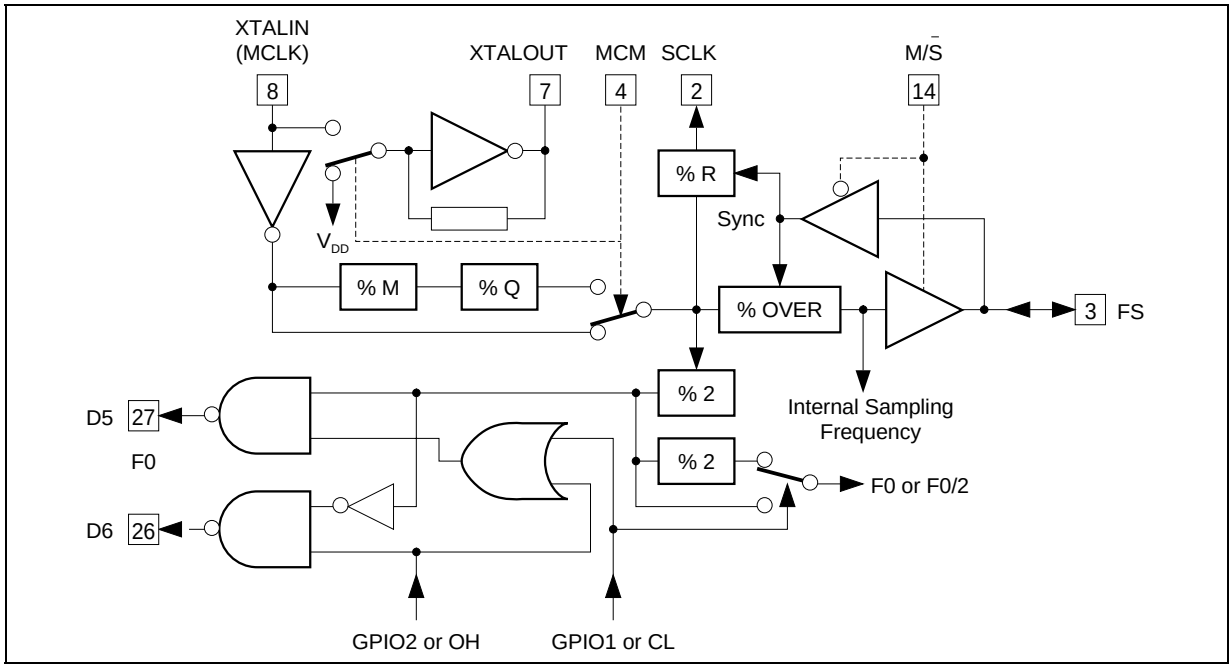
ST75951 generates all clocks from either a Master clock input on XTALIN (MCLK) or a crystal oscillator connected between XTALIN and XTALOUT.

The bypass of the divider M and Q is selected by setting the MCM input pin to '0'.

To be able to provide externally the sampling frequency (Slave mode), M/S input pin must be set to '0' (see Figure 2).

FUNCTIONAL DESCRIPTION (continued)

Figure 2



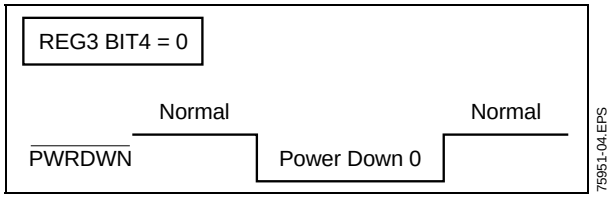
4 - Power Down Mode

Two PowerDown modes are available in ST75951 thanks to bit 4 in control register 3.

4.1 - PowerDown Mode 0

If bit 4 is set to '0' then when $\overline{\text{PWRDWN}}$ is set to '0' the entire chip is in powerdown mode 0.

Figure 3



4.2 - PowerDown Mode 1 (100µW)

When bit 4 is set to '1' then when $\overline{\text{PWRDWN}}$ is set to '0' the chip is in powerdown except the Ring detect circuitry (wake-up on Ring = powerdown mode 1).

The general purpose interrupt is also working in order to wake-up the system for dedicated customer feature associated with a defined GPIO (programmed as input and non-masked).

4.2.1 - Ring Bit and GPIO Bit Masked

In this configuration the processor relies on the Ring output pin to process the wake-up of the system and does not need the SSI to be powered-on. The SSI will be put back in operative mode when PWRDWN is set to '1' (see Figure 4).

4.2.2 - Ring Bit or GPIO Bit Non-Masked

In this configuration the processor relies on the SSI to process the wake-up of the system and needs the SSI to be powered-on.

On an incoming Ring signal or an interrupt coming thanks to the GPIO, ST75951 will generate an interrupt on GPI output pin and power-up the SSI, the processor will be able to read the control register 2 and find out the origine of the interrupt.

After a reading of the register 2, if the processor does not set high PWRDWN ST75951 puts back the SSI off in order to save energy (see Figure 5).

FUNCTIONAL DESCRIPTION (continued)

Figure 4

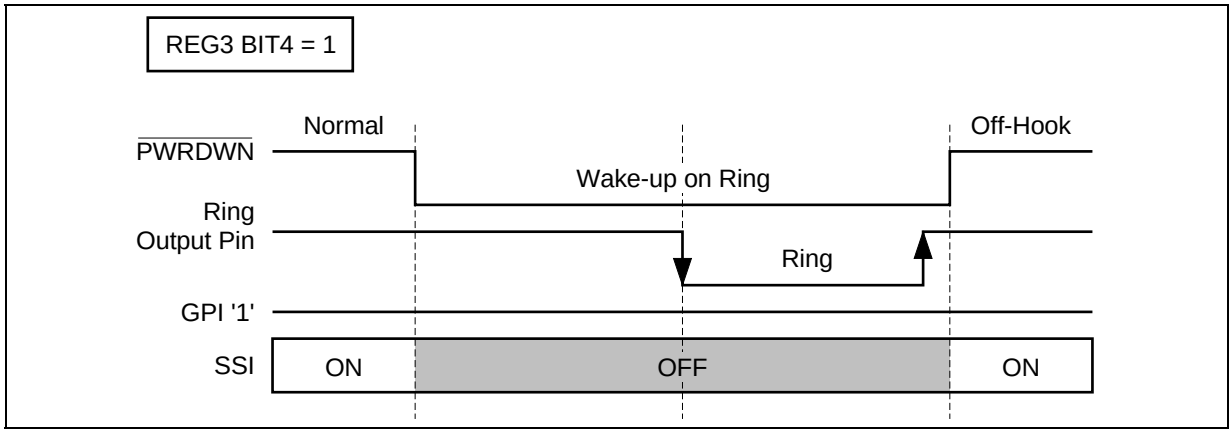
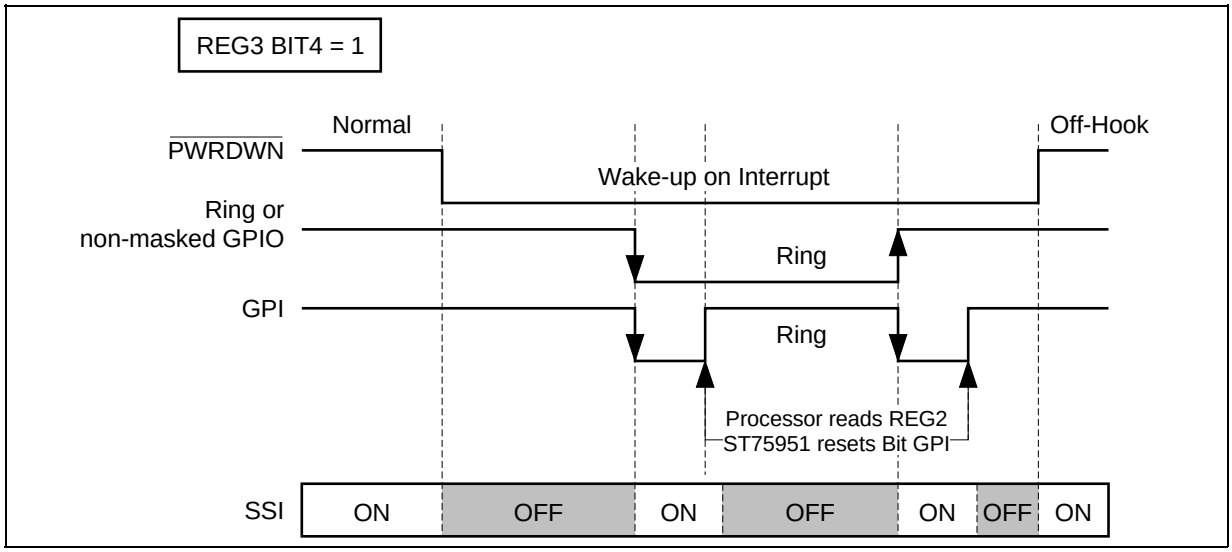


Figure 5



5 - Mode of Operation

Thanks to MCM and M/$\overline{S}$ programmation pins we can get the following configuration.

Configuration 1 : MCM = M/$\overline{S}$ = '1'.

ST75951 is in master mode and we have :
FS = F_Q / (M x Q x OVER). FS is an output. (see Figure 6).

Configuration 2 : MCM = '1', M/$\overline{S}$ = ' 0 '.

ST75951 is in slave mode and the processor provides FS = (R x SCLK) OVER. FS is an input (see Figure 7).

Configuration 3 : MCM = '0', M/$\overline{S}$ = '1'.

ST75951 is in master mode and we have :
FS = F_Q / (OVER). FS is an output (see Figure 8).

Configuration 4 : MCM = '0', M/$\overline{S}$ = ' 0 '.

The configuration 4 is equivalent to configuration 3 but the processor generates the FS and control the phase.

ST75951 is in slave mode and the processor provides FS = (R x SCLK)/OVER. FS is an input (see Figure 9).

Configuration 5 : Master codec 1 : MCM = '0', M/$\overline{S}$ = ' 1 '. Slave codec 2 : MCM = '0', M/$\overline{S}$ = ' 0 '.

This is a dual codec application running on the same SSI. The master codec has his data in timeslot 0 (bit 0 to bit15) and the slave codec has his data in timeslot 1 (bit 16 to bit 31) thanks to the programmation of TS (see Figure 10).

FUNCTIONAL DESCRIPTION (continued)

Figure 6

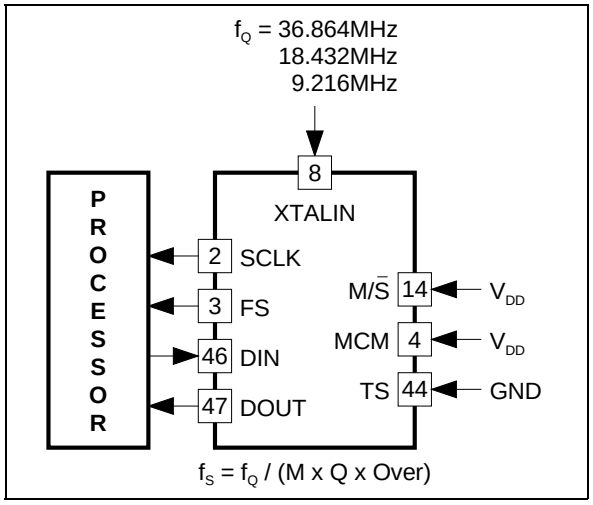


Figure 7

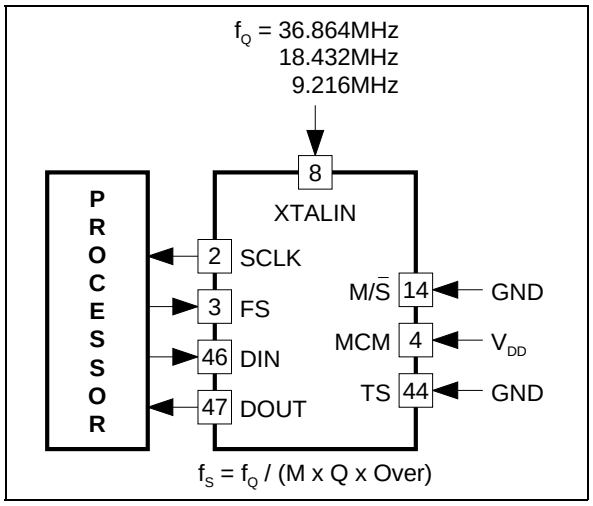


Figure 8

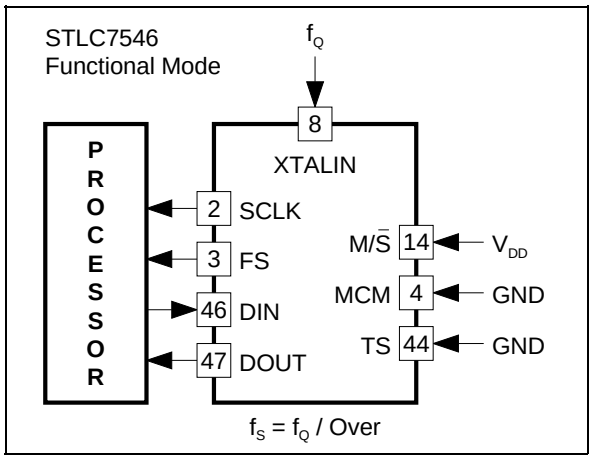


Figure 9

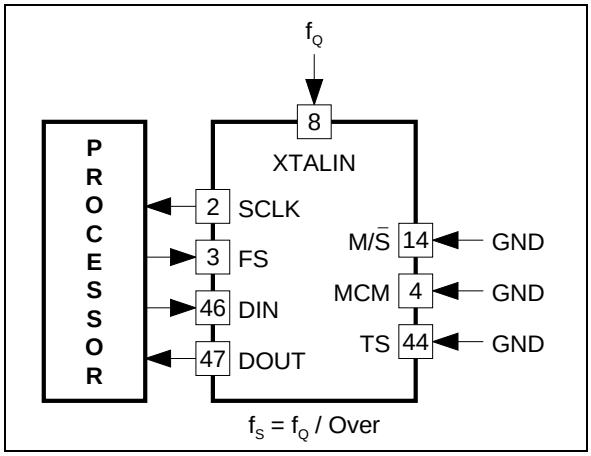
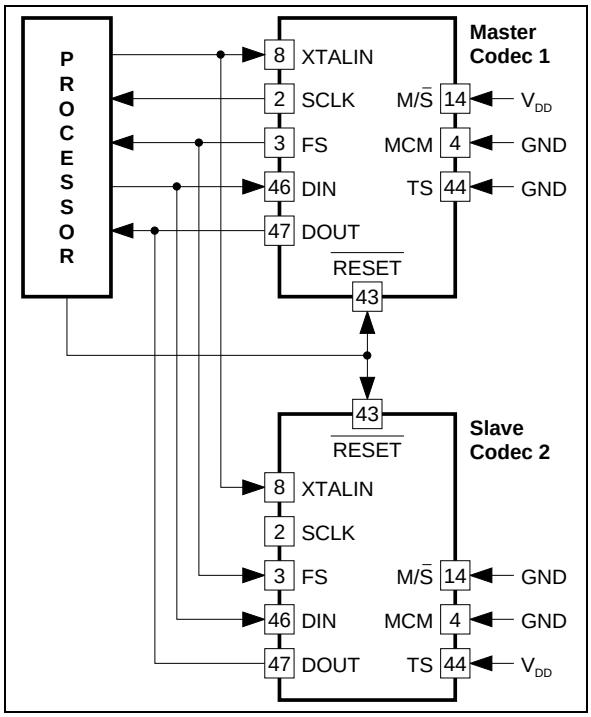


Figure 10



6 - General Purpose Input / Output

ST75951 features 4 GPIO. The GPIO0..3 are traditional inputs/outputs programmed and set thanks to the control register 1 (mask, input/output) and control register 2 (output value, static or modulated).

GPIO0 output is dedicated to output F0/N clocks instead of a static '1' if bit 6 in control register 2 is set. GPIO3 is dedicated to output F0 clock instead of a static '1' if bit 10 in control register 2 is set (see Figure 11 and 12).

FUNCTIONAL DESCRIPTION (continued)

Figure 11 : GPIO0 When bit6 = '1' in REG2

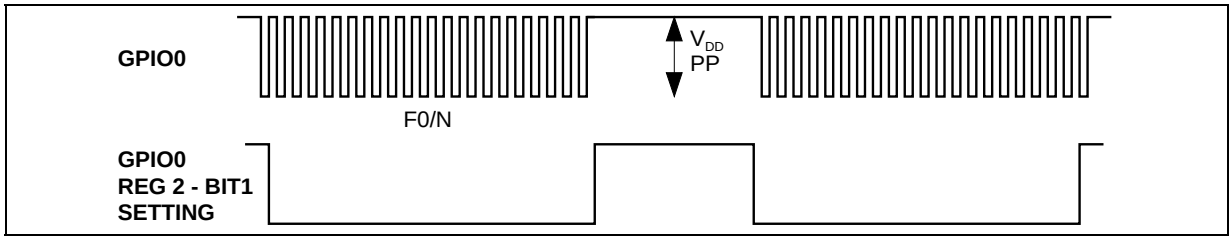
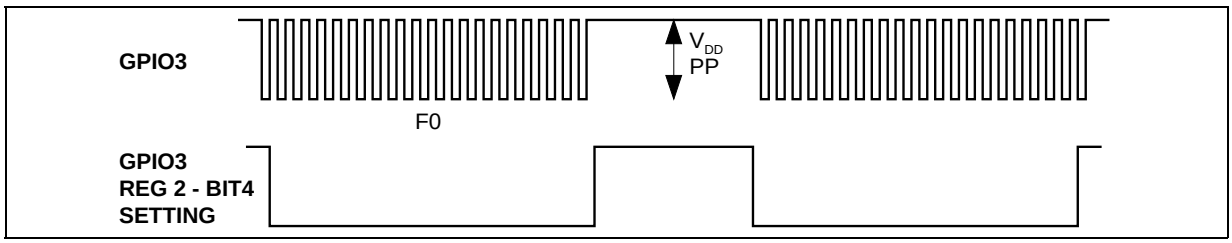


Figure 12 : GPIO3 When bit10 = '1' in REG2



GPIO1 and GPIO2 are dedicated input and control CLID and OFF-HOOK function respectively if the control input Pin HM is set to '1'.

Table 2

HM	GPIO1	GPIO2	Function
1	0	0	ON-HOOK
1	0	1	OFF-HOOK
1	1	0	CLID
1	1	1	SPECIAL
HM	**CL**	**OH**	**Function**
0	0	0	ON-HOOK
0	0	1	OFF-HOOK
0	1	0	CLID
0	1	1	SPECIAL

CL, OH : Bit 2, 3 Reg 3.

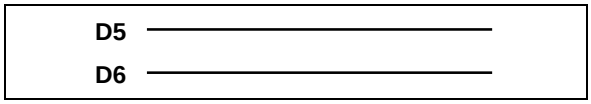
Depending of the setting of the Mask bit in control register 1, any change of non-masked GPIO can generate an interrupt to the processor thanks to GPI (General purpose Interrupt).

7 - Operating Modes

Three operating modes controlled either by the GPIO1 and 2 or by the control register 3 are implemented :

- ON-HOOK,
- OFF-HOOK,
- CLID (Caller ID).

Figure 13



7.1 - ON-HOOK

During ON-HOOK state no signal is sent by D5, D6.

D5 = D6 = V_{DD}.

Ring

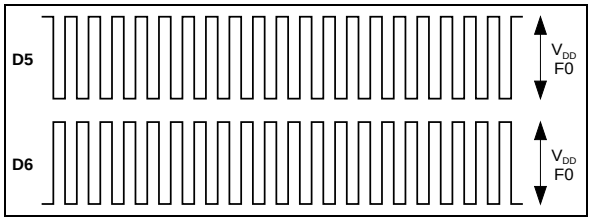
When in ON-HOOK state, the ST952 sends a 1MHz differential signal on D3, D4 when it receives an incoming ringing signal from Tip/Ring.

ST75951 will output on RING Pin the image of the ring signal (RING Pin is also duplicated in the read register 2 bit 5) (see Figure 15).

7.2 - OFF-HOOK

Depending on Pin HM status (see Table 2), 2 possibilities are offered to control the device to go in OFF-HOOK state.

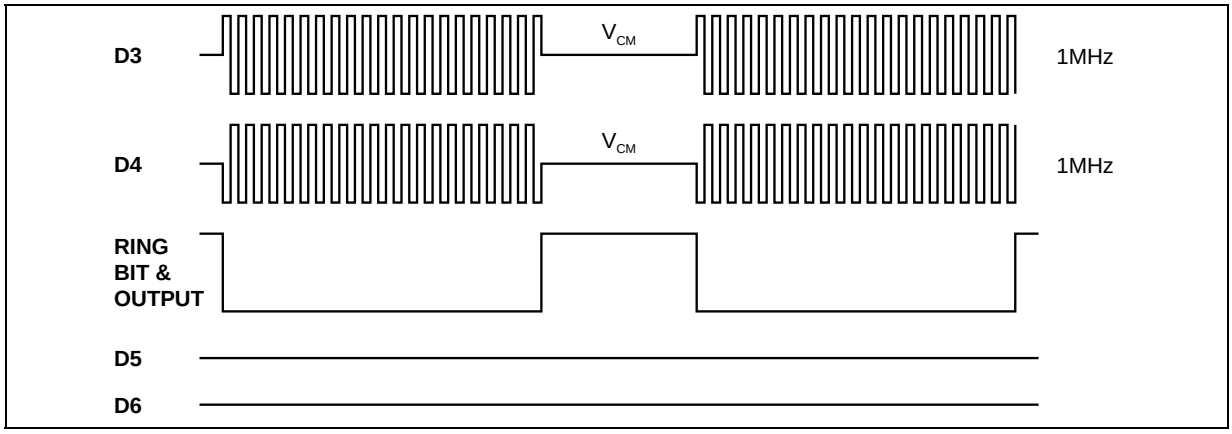
Figure 14



D5 and D6 send F0 clock in opposite phase to ST952.

FUNCTIONAL DESCRIPTION (continued)

Figure 15



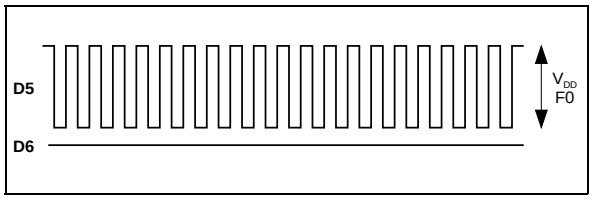
D5 = D6 = V_{DD}.

7.3 - Caller ID

Depending on Pin HM status (see Table 2), 2 possibilities are offered to control the device to go in caller ID state.

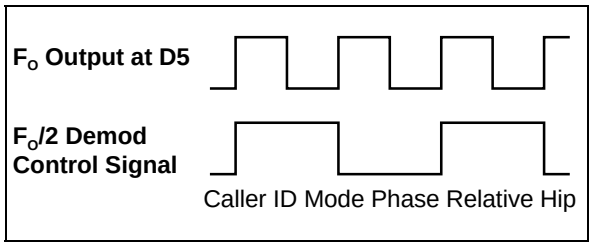
F0 clock is send to D5, in caller ID mode the modulation frequency of ST952 is equal to F0/2, so the demodulation on the receive signal at D3, D4 is at F0/2 in caller ID mode.

Figure 16



D6 = V_{DD}.

Figure 17



8 - Phone Line Monitoring Features

This chipset is intended to be used for a wide range of application such as modem, answering machine, telephony on PC, so because the home PSTN phone line will be shared by several terminals, information concerning the line status has to be sent to the host.

As long as there is an alerting signal at D3, D4 Pins, the ADC converter is saturated and outputs 7FFF or 8000 at DOUT Pin.

8.1 - Line In Use Checking

Before going OFF-HOOK the modem software can check that the line is free by setting the CLID mode and check that the RING Pin/bit output a low pulse. When in CLID mode if the line is free the ST952 will output a F0/2, $5V_{PP}$ differential signal on D3, D4 (see Figure 18).

8.2 - Digital Phone Line or Over Loop Current Limit Detect

When portable modem plug into digital line, it will cause over loop current during modem off-hook state.

The modem controller should know this condition and go onhook to avoid the DAA being damaged. ST952 when OFF-HOOK will determine if the loop current exceeds the current limit or not (160mA).

If we have overcurrent ST952 will continuously output a low level on RING output Pin.

FUNCTIONAL DESCRIPTION (continued)

Figure 18

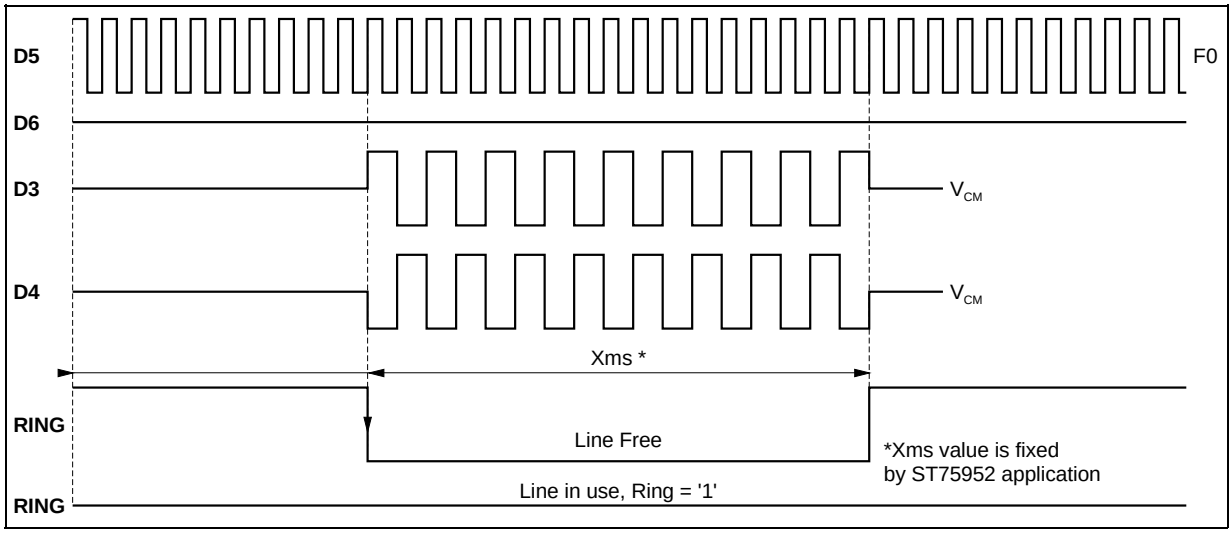
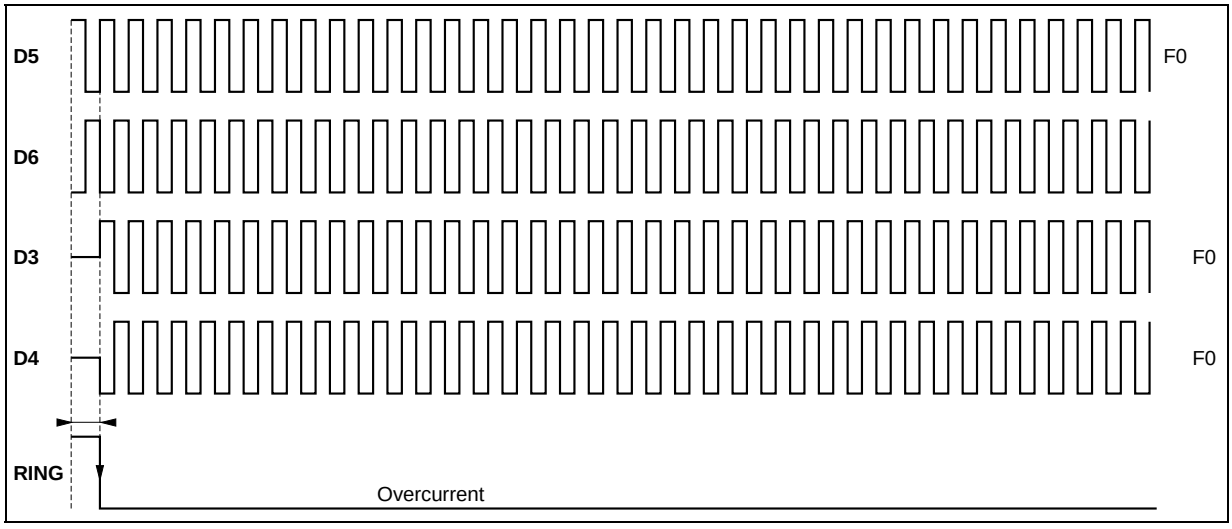


Figure 19

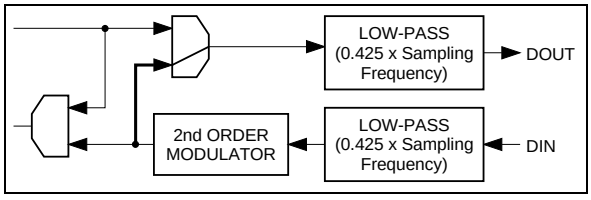


9 - Analog / Digital Loop Back Test

By programming bit 9,8 = ' 01' of control register 3, we can set ST75951 in 'local analog loop back' (see Figure 20).

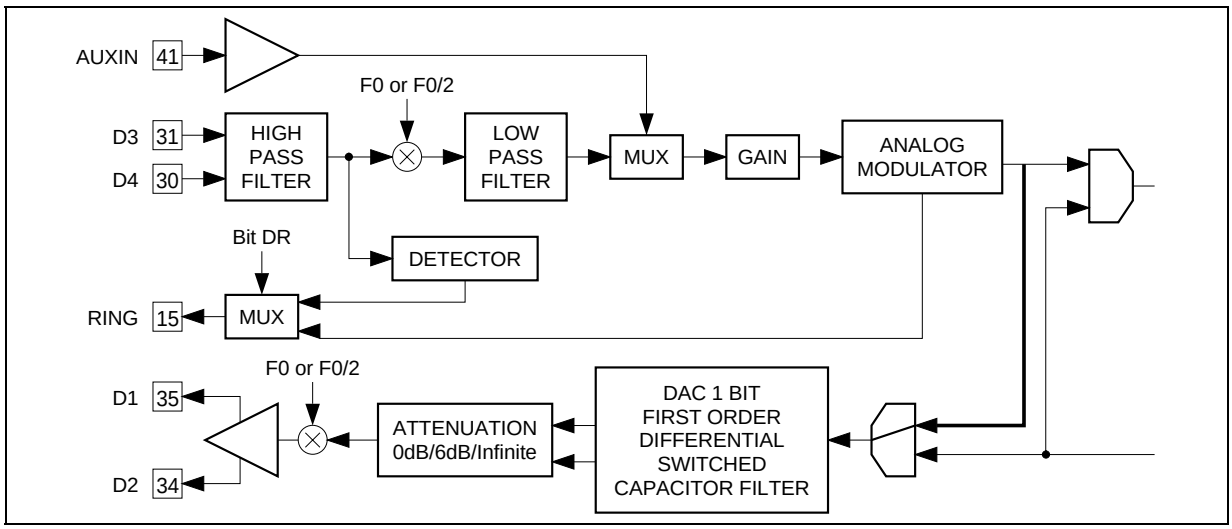
By programming bit 9, 8 =' 10' of control register 3, we can set ST75951 in 'local digital loop back' (see Figure 21).

Figure 20



FUNCTIONAL DESCRIPTION (continued)

Figure 21



10 - Host Interface

Table 3

HC1	HC0	LSB	2nd FS	Mode Description
0	0	0	no	Software mode, data transfer only
0	0	1	yes	Software mode, data xfer + control xfer
0	1	x	no	Hardware mode, data transfer only
1	x	x	yes	Hardware mode, data + control transfer

The host interface is a Serial Synchronous Interface (FS, SCLK, DOUT, DIN).
Two modes of serial transfer are available and are selected via pins HC0 and HC1.

First mode is a software mode control (15 bits transmit data and 16 bits receive data). In this mode ST75951 is completely controlled through the SSI, the access of control register is done by managing the LSB of the transmit data word.

Second mode is a hardware mode control (16bits data transmit and receive). In this mode the access of control register is done via dynamic setting of Pins HC0 and HC1 (see Table 3).

The bit 15 of the control word is used to do a read only or a read and write of control register (bit 15 = 1 Read only, bit 15 = 0 Read & Write).

11 - Control Registers

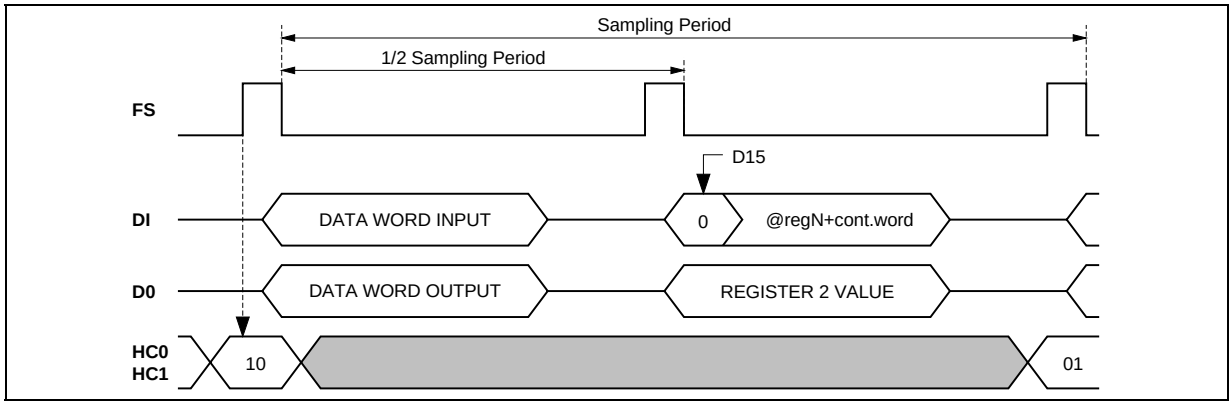
This section defines how to handle the 4 registers implemented in ST75951.

11.1 - Write / Read Operation (D15 = 0)

This is a one sampling frequency period duration operation, where the 16-bit word sent from the host on DIN, contains the write qualifier, the address register and the data field.

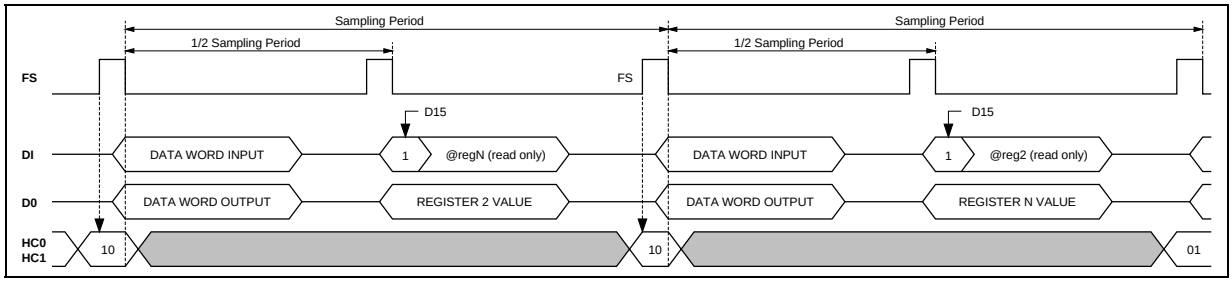
Contemporaly ST75951 ouptuts on DOUT the register 2 value (GPIO) (see Figure 22).

Figure 22 : WRITE REG n , READ default REG 2



FUNCTIONAL DESCRIPTION (continued)

Figure 23



11.2 - Read Operation (Register n) (D15 = 1)

This is a two sampling frequency period duration operation, where a first 16 bit word sent from the host on DIN, contains the read qualifier and the address register (register n).

Contemporaly ST75951 ouptuts on DOUT the register 2 (GPIO) while the address field is decoded.

Then a second read operation with the default address (register 2) is sent to the device. At that time ST75951 outputs on DOUT the register n value (see Figure 23, 24 and 25).

Figure 24

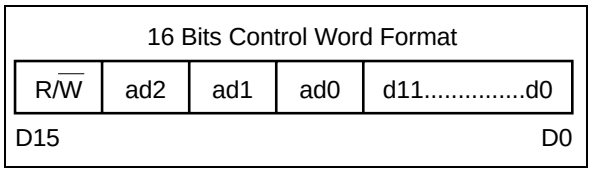
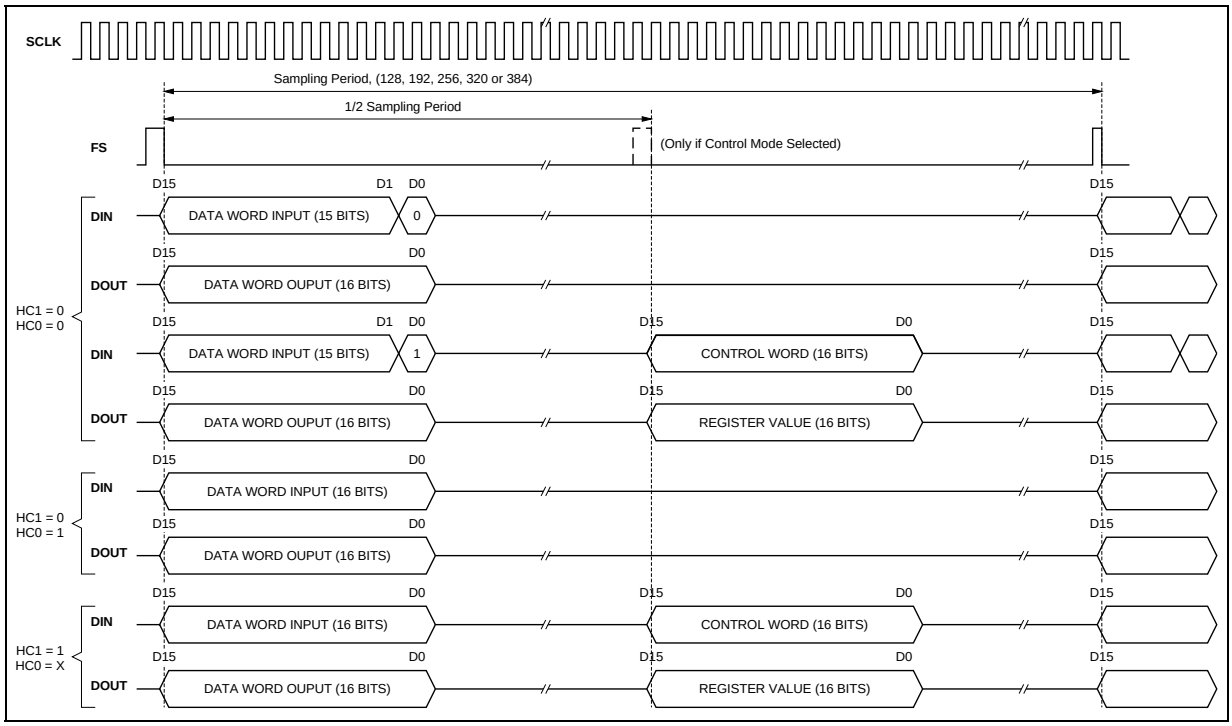


Figure 25



FUNCTIONAL DESCRIPTION (continued)

Table 4 : Control Register 0 : AFE Setting

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function
	0	0	0											0		Main Receive input (INI)
	0	0	0											1		Auxil. Receive input
	0	0	0										0			0dB Receive Gain (INI)
	0	0	0										1			+6dB Receive Gain
	0	0	0							0	0	0				OVER = 320 (INI)
	0	0	0							0	0	1				OVER = 384
	0	0	0							1	0	1				OVER = 128
	0	0	0							1	1	0				OVER = 192
	0	0	0							1	1	1				OVER = 256
	0	0	0					0	0							- Infin. attenuation XMIT (INI)
	0	0	0					0	1							+2dB gain XMIT
	0	0	0					1	0							6dB attenuation XMIT
	0	0	0					1	1							0dB gain XMIT
	0	0	0				0									M = 1
	0	0	0				1									M = 2 (INI)
	0	0	0	0	0	0										Q = 3
	0	0	0	0	0	1										Q = 6 (INI)
	0	0	0	0	1	0										Q = 7
	0	0	0	0	1	1										Q = 8
	0	0	0	1	0	0										Q = 4.5
	0	0	0	1	0	1										Q = 5.5
	0	0	0	1	1	0										Q = 6.5
	0	0	0	1	1	1										Q = 7.5

Table 5 : Control Register 1 : GPIO Setting, Ring Bit

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function
	0	0	1								Di3	Di2	Di1	Di0		DIR. '0' = (Inp INI), 1 = Out
	0	0	1		MR	M3	M2	M1	M0							MASK for INT. GPI '0' masked (INI), '1' unmasked
										DR						Digital Ring '1' on, '0' off (INI)

Table 6 : Control Register 2 : GPIO / RING Output Setting

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function
	0	1	0								G3	G2	G1	G0		GPIOx output setting, read input
	0	1	0							RG						Read only, Ring
	0	1	0		S											GPIO3 '0' In static Value (INI) if set GPIO3 modulated at F0
	0	1	0				x	x	0							GPIO0 In static Value (INI)
	0	1	0				0	0	1							GPIO0 Modulate at F0
	0	1	0				0	1	1							GPIO0 Modul. at F0/2
	0	1	0				1	0	1							GPIO0 Modul. at F0/4
	0	1	0				1	1	1							GPIO0 Modul. at F0/8

Note : GPI is in "high" state, any change on one Gx or RG non-masked put GPI in "low" state, one read on this register (@010) put GPI in "hight" state.

FUNCTIONAL DESCRIPTION (continued)

Table 7 : Control Register 3 : Clock / configuration setting

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function
	0	1	1									OH	CL			Software value (HM = 0)
	0	1	1								0					Normal operation (INI)
	0	1	1								1					PowerDown with wake-up on ring or non-masked GPIO
	0	1	1							0						Transmit modulated (INI)
	0	1	1							1						Transmit not modulated
	0	1	1					0	0							SCLK = MCLK (R = 1)
	0	1	1					0	1							SCLK = MCLK/2 (R = 2) (INI)
	0	1	1					1	0							SCLK = MCLK/4 (R = 4)
	0	1	1					1	1							Reserved
	0	1	1			0	0									Normal mode (INI)
	0	1	1			0	1									Analog loop back
	0	1	1			1	0									Digital loop back
	0	1	1			1	1									Reserved
	0	1	1	0	0											Normal mode (INI)
	0	1	1	0	1											Reserved
	0	1	1	1	0											TSTD1 Pin = PCLK output
	0	1	1	1	1											TSTD1 Pin = PCLK input

Below you'll find a table giving different programmation for achieving all common V.34 baud rate with ST75951 working with an external crystal f_Q = 36.864 MHz. The 8kHz could be used for voice processing and the 16kHz for the 56K (V.pcm).

Table 8

Baud Rate	F_S	Over	M	Q	F0
	16000	192	2	6	1536000
3429	13714.29	192	2	7	1316571
3000	12000	256	2	6	1536000
3490	10472.73	320	2	5.5	1675636
3429	10285.71	256	2	7	1316571
2400/3200	9600	320	2	6	1536000
3000	9000	256	2	8	1152000
2953	8861.54	320	2	6.5	1417846
2743	8228.57	320	2	7	1316571
	8000	384	2	6	1536000
2400	7200	320	2	8	1152000

In any cases attention must be paid to have F0 between 1MHz and 1.7 MHz , optimum value beeing 1.5MHz.

The modulator and demodulator frequency F0 = OVERSAMPLING FREQUENCY / 2.

When MCM = ' 0', we have OVERSAMPLING FREQUENCY = MCLK and F0 = MCLK / 2 SCLK = MCLK / R (see clock block diagram).

Table 9 : (eg : with R = 4)

f_S (kHz)	M	Q	Over	MCLK (MHz)	F0 (MKz)	SCLK (kHz)
8	X	X	384	3.072	1.536	768
9.6	X	X	320	3.072	1.536	768
9.6	X	X	256	2.4576	1.2288	614.4
16	X	X	192	3.072	1.536	768

ELECTRICAL SPECIFICATION

Unless otherwise noted, Electrical characteristics are specified over the operating range.
Typical value are given for V_{DD} = 3.3V, T_{AMB} = 25°C. Initial value MCLK external = 3.072MHz.

Absolute Maximum Rating (AGND = DGND = 0V, all voltages with respect to 0V)

Symbol	Parameter	Value	Unit
AV_{DD}	Analog Power Supply	-0.3, 6.0	V
DV_{DD}	Digital Power Supply	-0.3, 6.0	V
II	Input Current per Pin	-10, +10	mA
I_O	Output Current per Pin	-20, +20	mA
V_{IA}	Analog Input Voltage	-0.3, 6	V
V_{ID}	Digital Input Voltage	-0.3, 6	V
V_{IDGPIO}	Digital Input Voltage at GPIO	5.25	V
T_{oper}	Operating Temperature	0, +70	°C
T_{stg}	Storage Temperature	- 40, +125	°C
P_{tot}	Maximum Power Dissipation	200	mW

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Warning : Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Dc Characteristics (T_{amb} = 0 to 70°C unless otherwise specified)

Power Supply And Common Mode Voltage

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	2.7	3.3	5.25	V
I_{DVDD}	Digital Supply Current		6	8	mA
I_{AVDD}	Analog Supply Current		9	12	mA
I_{DLP}	Low Power mode (Hardware control $\overline{\text{PWRDWN}}$ Pin) @ 25°C		10		µA
$I_{DLP\ R}$	Low Power mode (Software control with wake-up on Ring) @ 25°C		30	100	µA
V_{CM}	Common Mode Voltage Output (see note 1)	AV_{DD}/2-5%		AV_{DD}/2+5%	V

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Note 1 : V_{CM} output voltage current must be DC (<10 µA) If dynamic load exists, the VCM output must be buffered or the performances of ADCs and DACs will be degraded.

Digital Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage	DV_{DD}-0.5			V
V_{IL}	Low Level Input Voltage	-0.3		0.5	V
V_{OH}	High Level Output Voltage (I_{LOAD} = +2mA)	DV_{DD}-0.5			V
V_{OL}	Low Level Output Voltage (I_{LOAD} = -2mA)			0.3	V
I_{LEAK}	Input Leakage Current	-1		1	µA
I_{XIN}	Input Leakage Current (XTALIN Pin when MCM = 1)	-25		25	µA

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ELECTRICAL SPECIFICATION (continued)

Analog Interface

(typical value are given for AV_{DD} = DV_{DD} = 3.3V, T_{amb} = 25°C. Measurement band = 0 to 0.425 x f_S)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{REF}	Differential reference voltage output V_{REF} = (V_{REFP} - V_{REFN})		1.18	1.25	1.32	V
$V_{DIFF\ IN}$	Differential Input Voltage [D3 - D4] ≤ 2 x V_{REF}			2.5		V_{PP}
$V_{ADO\ OUT}$	A/D Modulator Output DC Offset Voltage	See Figure 26	-50		50	mV
$V_{DIFF\ OUT}$	Differential Output Voltage [D1 - D2]	XMIT = 0dB XMIT= 2dB		2.5 3.2		V_{PP} V_{PP}
$V_{OFF\ OUT}$	Differential Output DC Offset Voltage	Input code = 0000h	-50		50	mV
R_{IN}	Input Resistance (D3, D4)		40			kΩ
R_{OUT}	Output Resistance (D1, D2)			4		kΩ
R_L	Load Resistance (D1, D2)		10			kΩ
C_L	Load Capacitance (D1, D2)				20	pF
Res	Converter Resolution	See Note 2	16			Bit
DNL	Differential Non Linearity	See Note 2	-0.9		0.9	Bit
GTX	Channel Gain at f_0 + 1kHz		-0.5		0.5	dB
Ripple	Ripple in Band	0 to 0.425 * f_S, see Notes 2 & 3		±0.2		dB
StopB	Stop Band Attenuation	$f_0 \pm 0.5 * f_S$		-70		dB
SNDR	Signal / Noise + Distortion at - 5dBr	XMIT = 0dB, see Note 1 XMIT = 2dB		80 74		dB dB
DR	Dynamic Range	f = 1kHz, XMIT ATTE = 0dB, see Note 1, Measured over the full 0 to Fs/2 with -20dBr input and extrapoled to full scale		85		dB
GRX	Receive Gain (Rx gain set to 0 dB)		-1	0	+1	dB
PSRR	Power supply rejection ratio	f = 1kHz, V_{AC} = 200mV_{PP}, see Note 1		40		dB

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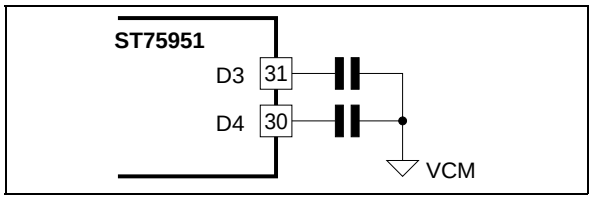
Notes : 1. These parameters are valid for transmit and receive channels.
2. This specification is guaranteed by characterization, not production testing.
3. Transmit channels measured in baseband without modulation.

Figure 26



75951-27.EPS

ELECTRICAL SPECIFICATION (continued)

Serial Channel Timing

(Reference level V_{IL} = 0.8V, V_{IH} = DV_{DD}-0.5V, Vol = 0.4V, V_{OH} = DV_{DD}-0.5V, V_{BUS} = 5V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
1	SCLK Period	300			ns
2	SCLK Width Low	150			ns
3	SCLK Width High	150			ns
4	SCLK Rise Time			10	ns
5	SCLK Fall Time			10	ns
6	FS Set-up	100			ns
7	FS Hold	100			ns
8	Din set-up	50			ns
9	Din Hold	0			ns
10	D_{OUT} Valid			20	ns
11	HC0, HC1 Set-up	20			ns
12	FS to SCLK Delay	0		50	ns

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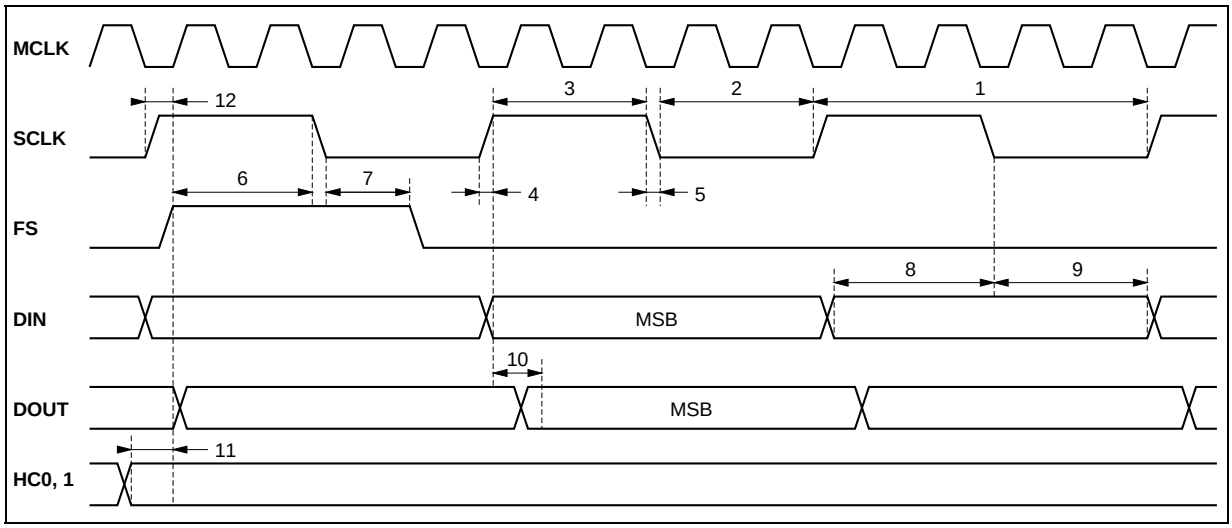
Figure 27 : Timing Diagram (R = 4)



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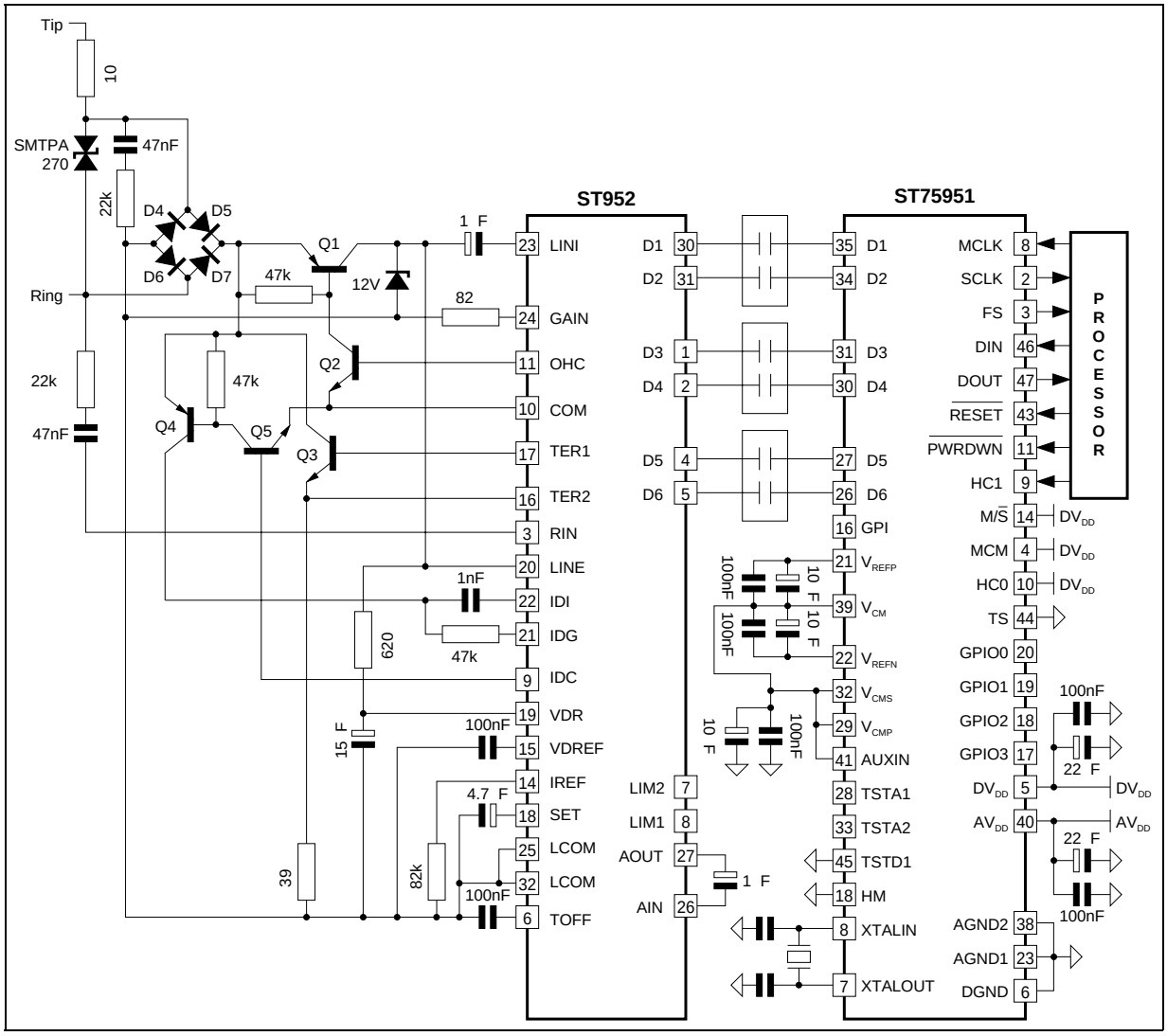
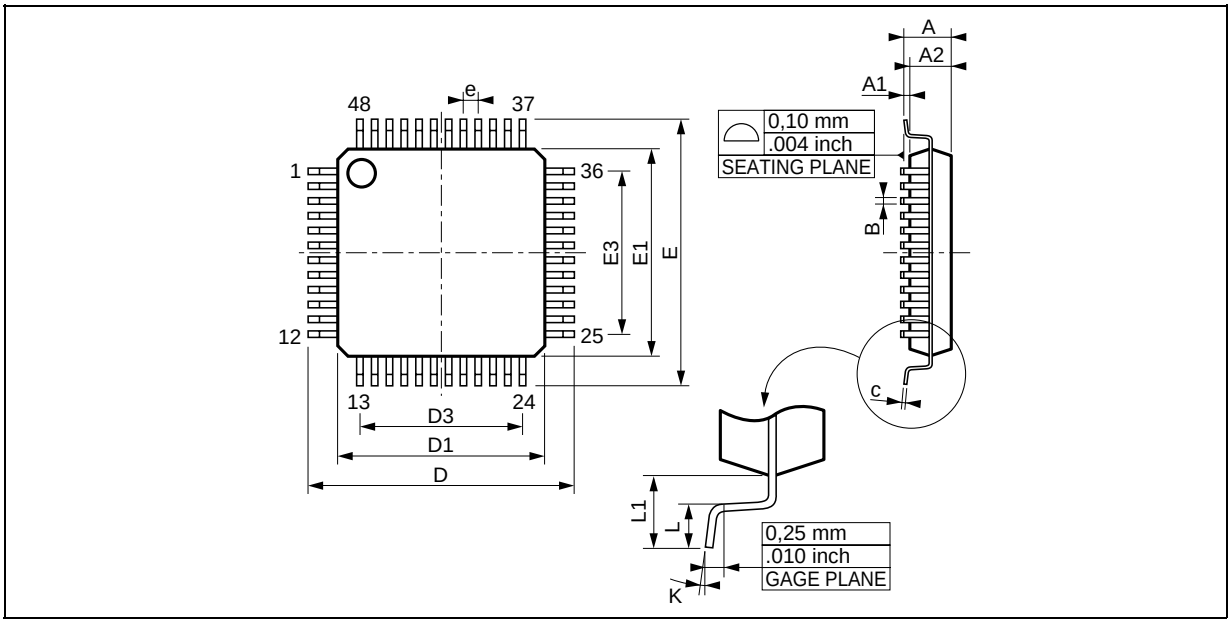
TYPICAL APPLICATION



PACKAGE MECHANICAL DATA

48 PINS - THIN PLASTIC QUAD FLAT PACK (TQFP)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
D3		5.50			0.216	
e		0.50			0.0197	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.50			0.216	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0^o (Min.), 7^o (Max.)					

5B.TBL