AS3932

3D Low Frequency Wakeup Receiver

General Description

The AS3932 is a 3-channel low power ASK receiver that is able to generate a wake-up upon detection of a data signal which uses a LF carrier frequency between 110 - 150 kHz. The integrated correlator can be used for detection of a programmable 16-bit wake-up pattern. The device can operate using one, two, or three active channels.

The AS3932 provides a digital RSSI value for each active channel, it supports a programmable data rate. The AS3932 offers a real-time clock (RTC), which is either derived from a crystal oscillator or the internal RC oscillator.

The programmable features of AS3932 enable to optimize its settings for achieving a longer distance while retaining a reliable wake-up generation. The sensitivity level of AS3932 can be adjusted in presence of a strong field or in noisy environments.

The device is available in 16-pin TSSOP and 16LD QFN (4×4) packages.

Ordering Information and *Content Guide* appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS3932, 3D Low Frequency Wakeup Receiver are listed below:

Figure 1:
Added Value of Using AS3932

| Benefits	Features
Enables low power active tags	3-channel ASK wake-up receiver
Selectable carrier frequency	Carrier frequency range 110 - 150 kHz
One, two, or three channel operation	1-D, 2-D, or 3-D wake-up pattern detection
Highly resistant to false wake-ups	16-bit programmable wake-up pattern
Improved immunity to false wake-ups	Supporting doubling of wake-up pattern
Allows frequency only detection	Wake-up without pattern detection selectable
Improved range with best-in-class sensitivity	Wake-up sensitivity 100µVRMS (typ.)
Adjustable range	Sensitivity level adjustable
Provides tracking of false wake-ups	False wake-up counter
Ensures wake-up in a noise environment	Periodical forced wake-up supported (1s – 2h)
Extended battery life	Current consumption in 3-channel listening mode 1.7µA (typ.)

| Benefits	Features
Flexible clock configuration	RTC based 32 kHz XTAL, RC-OSC, or external clock
Operates from a 3V battery	Operating supply range 2.4V – 3.6V (TA = 25°C)
Industrial temperature range	Operation temperature range -40°C to +85°C

Applications

The AS3932 is ideal for:

- Active RFID tags,
- Real-time location systems,
- Operator identification,
- Access control, and
- Wireless sensors.

Figure 2:
AS3932 Typical Application Diagram with Crystal Oscillator
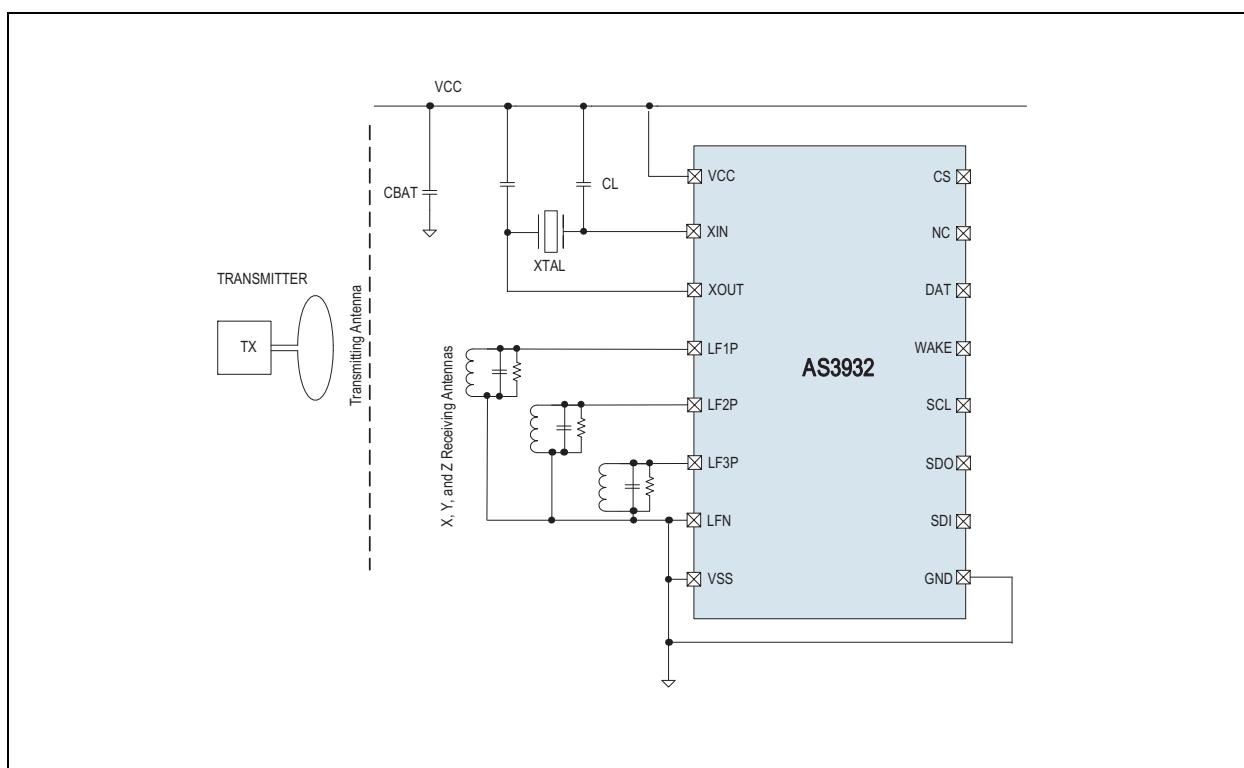
Figure 3:
**AS3932 Typical Application Diagram with RC Oscillator**
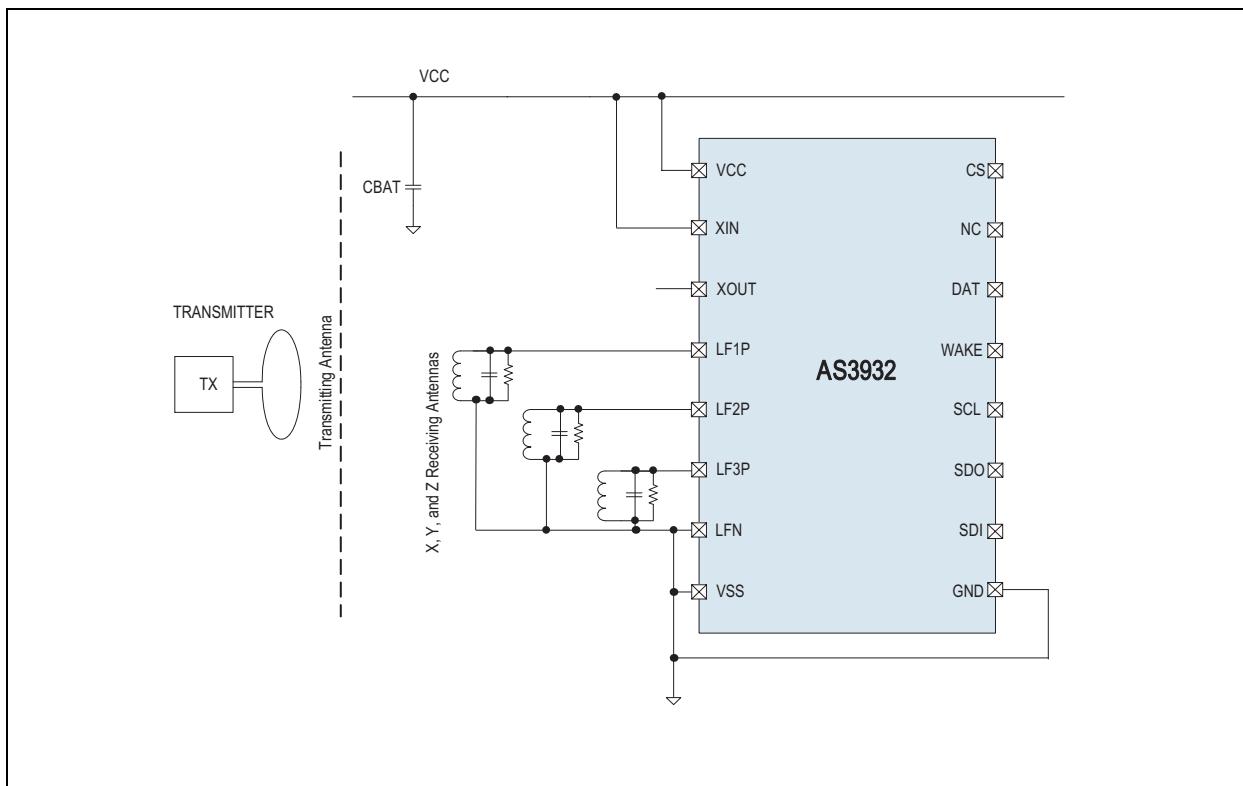
Figure 4:
AS3932 Typical Application Diagram with Clock from External Source
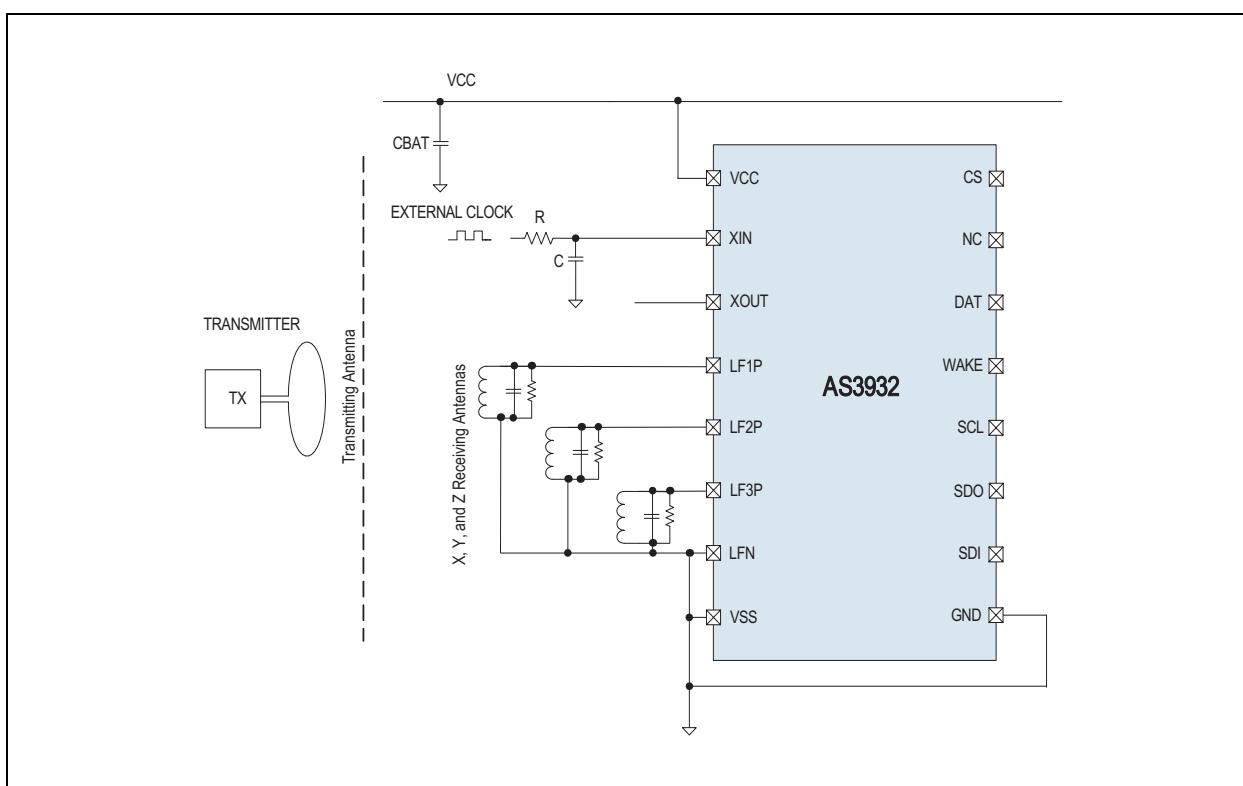
Pin Assignment

TSSOP Package

Figure 5:
Pin Assignments 16-pin TSSOP Package
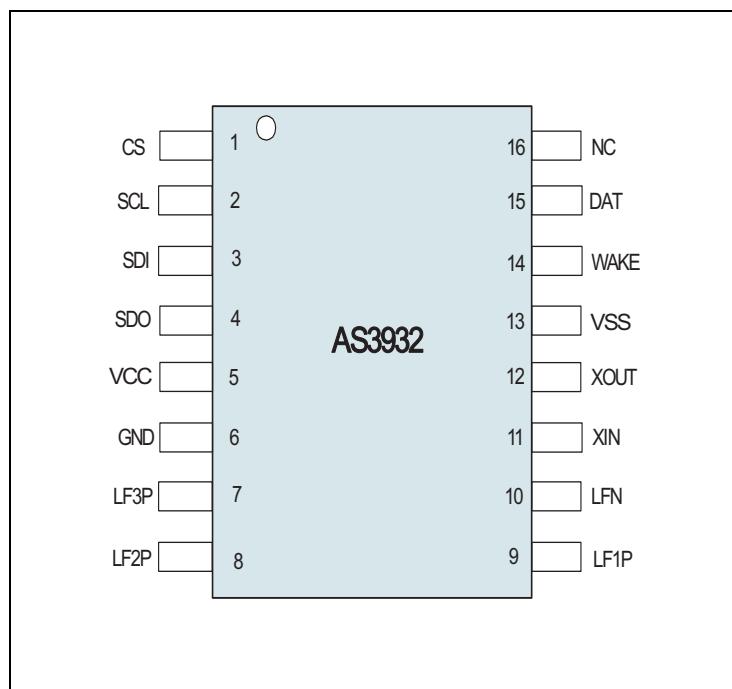
Pin Description

Figure 6:
Pin Descriptions 16-pin TSSOP Package

Pin Name	Pin Number	Pin Type	Description
CS	1	Digital input	Chip select
SCL	2		SDI interface clock
SDI	3		SDI data input
SDO	4	Digital output / tristate	SDI data output (tristate when CS is low)
VCC	5	Supply pad	Positive supply voltage
GND	6	Supply pad	Negative supply voltage

Pin Name	Pin Number	Pin Type	Description
LF3P	7	Analog I/O	Input antenna channel three
LF2P	8		Input antenna channel two
LF1P	9		Input antenna channel one
LFN	10		Common ground for antenna one, two and three
XIN	11		Crystal oscillator input
XOUT	12		Crystal oscillator output
V_{SS}	13	Supply pad	Substrate
WAKE	14	Digital output	Wake-up output IRQ
DAT	15		Data output
NC	16	-	Not connected

QFN Package

Figure 7:
Pin Assignments 16LD QFN (4×4) Package
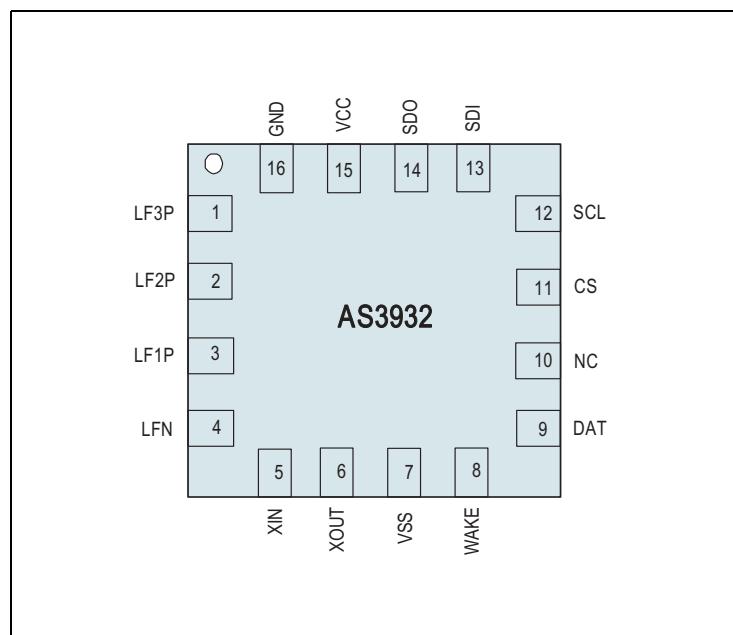
Pin Description

Figure 8:
Pin Descriptions 16LD QFN (4×4) Package

Pin Name	Pin Number	Pin Type	Description
LF3P	1	Analog I/O	Input antenna channel three
LF2P	2		Input antenna channel two
LF1P	3		Input antenna channel one
LFN	4		Common ground for antenna one, two and three
XIN	5		Crystal oscillator input
XOUT	6		Crystal oscillator output
V_{SS}	7	Supply pad	Substrate
WAKE	8	Digital output	Wake-up output IRQ
DAT	9		Data output
NC	10	-	Not connected
CS	11	Digital input	Chip select
SCL	12		SDI interface clock
SDI	13		SDI data input
SDO	14	Digital output / tristate	SDI data output (tristate when CS is low)
VCC	15	Supply pad	Positive supply voltage
GND	16	Supply pad	Negative supply voltage

Note(s) and/or Footnote(s):

1. The exposed pad has to be connected to ground.

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 9:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
Electrical Parameters					
V_{DD}	DC supply voltage	-0.5	5	V	
V_{IN}	Input pin voltage	-0.5	5	V	
I_{SOURCE}	Input current (latch up immunity)	-100	100	mA	Norm: Jedec 78
Electrostatic Discharge					
ESD	Electrostatic discharge	±2		kV	Norm: MIL 883 E method 3015 (HBM)
Continuous Power Dissipation					
P_t	Total power dissipation		0.07	mW	All supplies and outputs
Temperature Ranges and Storage Conditions					
T_{strg}	Storage temperature	-65	150	°C	
T_{body}	Package body temperature		260	°C	Norm: IPC/JEDEC J-STD-020 *The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices".*
RH_{NC}	Relative Humidity non-condensing	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a maximum floor life time of 168h

Electrical Characteristics

Figure 10:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Operating Conditions						
V_{DD}	Positive supply voltage		2.4		3.6	V
V_{SS}	Negative supply voltage		0		0	V
T_{AMB}	Ambient temperature		-40		85	°C
DC/AC Characteristics for Digital Inputs and Outputs						
CMOS Input						
V_{IH}	High level input voltage		0.58* V_{DD}	0.7* V_{DD}	0.83* V_{DD}	V
V_{IL}	Low level input voltage		0.125* V_{DD}	0.2* V_{DD}	0.3* V_{DD}	V
I_{LEAK}	Input leakage current				100	nA
CMOS Output						
V_{OH}	High level output voltage	With a load current of 1mA	V_{DD} - 0.4			V
V_{OL}	Low level output voltage	With a load current of 1mA			V_{SS} + 0.4	V
C_L	Capacitive load	For a clock frequency of 1 MHz			400	pF
Tristate CMOS Output						
V_{OH}	High level output voltage	With a load current of 1mA	V_{DD} - 0.4			V
V_{OL}	Low level output voltage	With a load current of 1mA			V_{SS} + 0.4	V
I_{OZ}	Tristate leakage current	To V_{DD} and V_{SS}			100	nA

Figure 11:
Electrical System Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input Characteristics						
R_{IN}	Input Impedance	In case no antenna damper is set (R1<4>=0)		2		MΩ
Fmin	Minimum Input Frequency			110		kHz
Fmax	Maximum Input Frequency			150		kHz
Current Consumption						
IPWD	Power Down Mode			400		nA
I1CHRC	Current Consumption in standard listening mode with one active channel and RC-oscillator as RTC			2.7		µA
I2CHRC	Current Consumption in standard listening mode with two active channels and RC-oscillator as RTC			4.2		µA
I3CHRC	Current Consumption in standard listening mode with three active channels and RC-oscillator as RTC			5.7	8.3	µA
I3CHSCRC	Current Consumption in scanning mode with three active channels and RC-oscillator as RTC			2.7		µA
I3CHOORC	Current Consumption in ON/ OFF mode with three active channels and RC-oscillator as RTC	11% Duty Cycle		1.7		µA
		50% Duty Cycle		3.45		
I3CHXT	Current Consumption in standard listening mode with three active channels and crystal oscillator as RTC			6.5	8.9	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IDATA	Current Consumption in Preamble detection / Pattern correlation / Data receiving mode (RC-oscillator)	With 125 kHz carrier frequency and 1kbpsdata-rate. No load on the output pins.		8.3	12	µA
Input Sensitivity						
SENS	Input Sensitivity on all channels	With 125 kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection		100		µVrms
Channel Settling Time						
TSAMP	Amplifier settling time			250		µs
Crystal Oscillator						
FXTAL	Frequency	Crystal dependent		32.768		kHz
TXTAL	Start-up Time	Crystal dependent			1	s
IXTAL	Current consumption			1		µA
External Clock Source						
IEXTCL	Current consumption			1		µA
RC Oscillator						
FRCNCAL	Frequency	If no calibration is performed	27	32.768	42	kHz
FRCCAL32	Frequency	If calibration with 32.768 kHz reference signal is performed	31	32.768	34.5	kHz
FRCCALMAX	Frequency	Maximum achievable frequency after calibration		35		kHz
FRCCALMIN	Frequency	Minimum achievable frequency after calibration		30		kHz
TRC	Start-up time	From RC enable (R1<0> = 0)			1	s
TCALRC	Calibration time				65	Periods of reference clock
IRC	Current consumption			200		nA

Typical Operating Characteristics

Figure 12:
**Sensitivity over Voltage and Temperature**
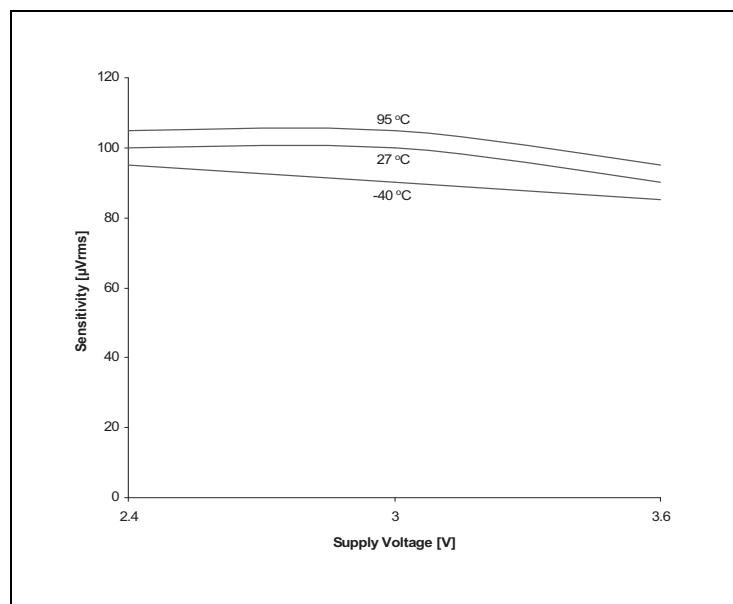
Figure 13:
Sensitivity over RSSI
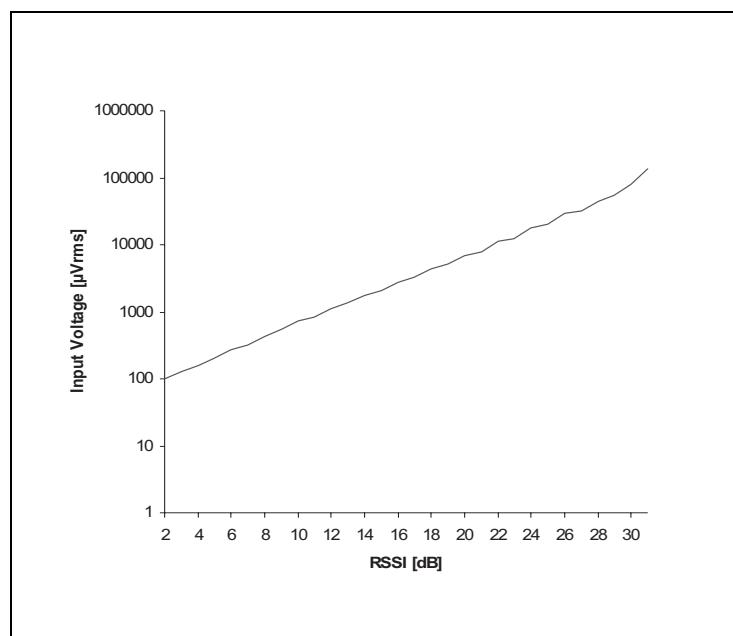
Figure 14:
RC-Osc Frequency over Voltage (calibr.)
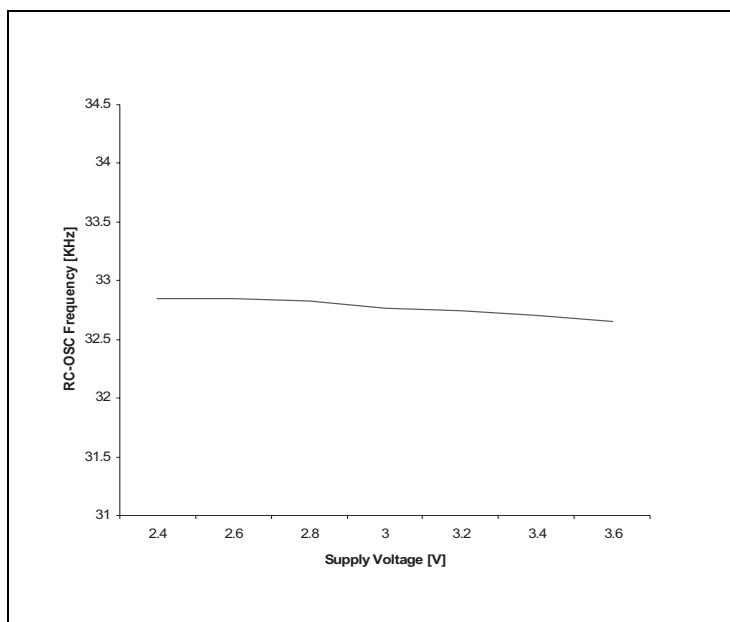
Figure 15:
**RC-Osc Frequency over Temperature (calibr.)**
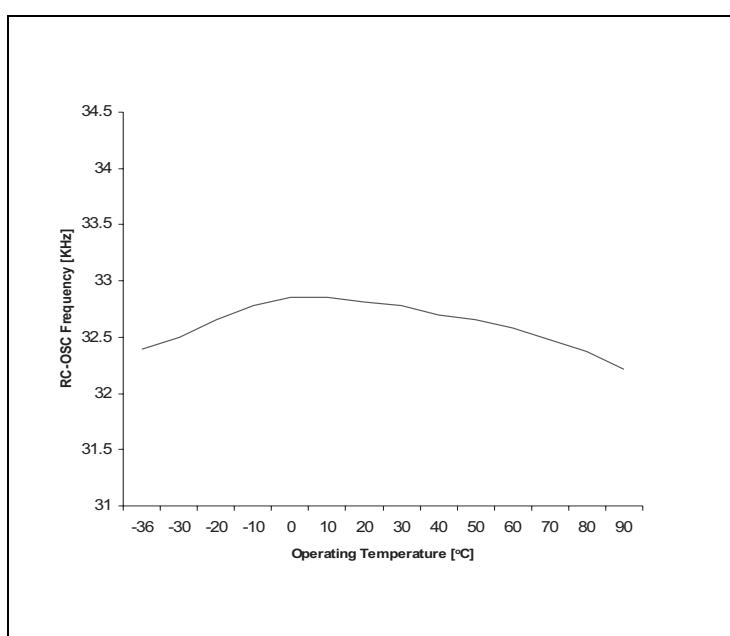
Detailed Description

The AS3932 is a three-dimensional low power low-frequency wake-up receiver. The AS3932 is capable to detect the presence of an inductive coupled carrier and extract the envelope of the ON-OFF-Keying (OOK) modulated carrier. If the detected pattern corresponds to the stored one a wake-up signal (IRQ) is risen up. The pattern correlation can be bypassed in which case the wake-up detection is based only on the frequency detection.

The AS3932 is made up by three independent receiving channels, one envelop detector, one data correlator, 8 programmable registers with the main logic and a real time clock.

The digital logic can be accessed by an SPI. The real time clock can be based on a crystal oscillator or on an internal RC one. If the internal RC oscillator is used, a calibration procedure can be performed to improve its accuracy.

Figure 16:
Block Diagram of LF Wake-up Receiver AS3932
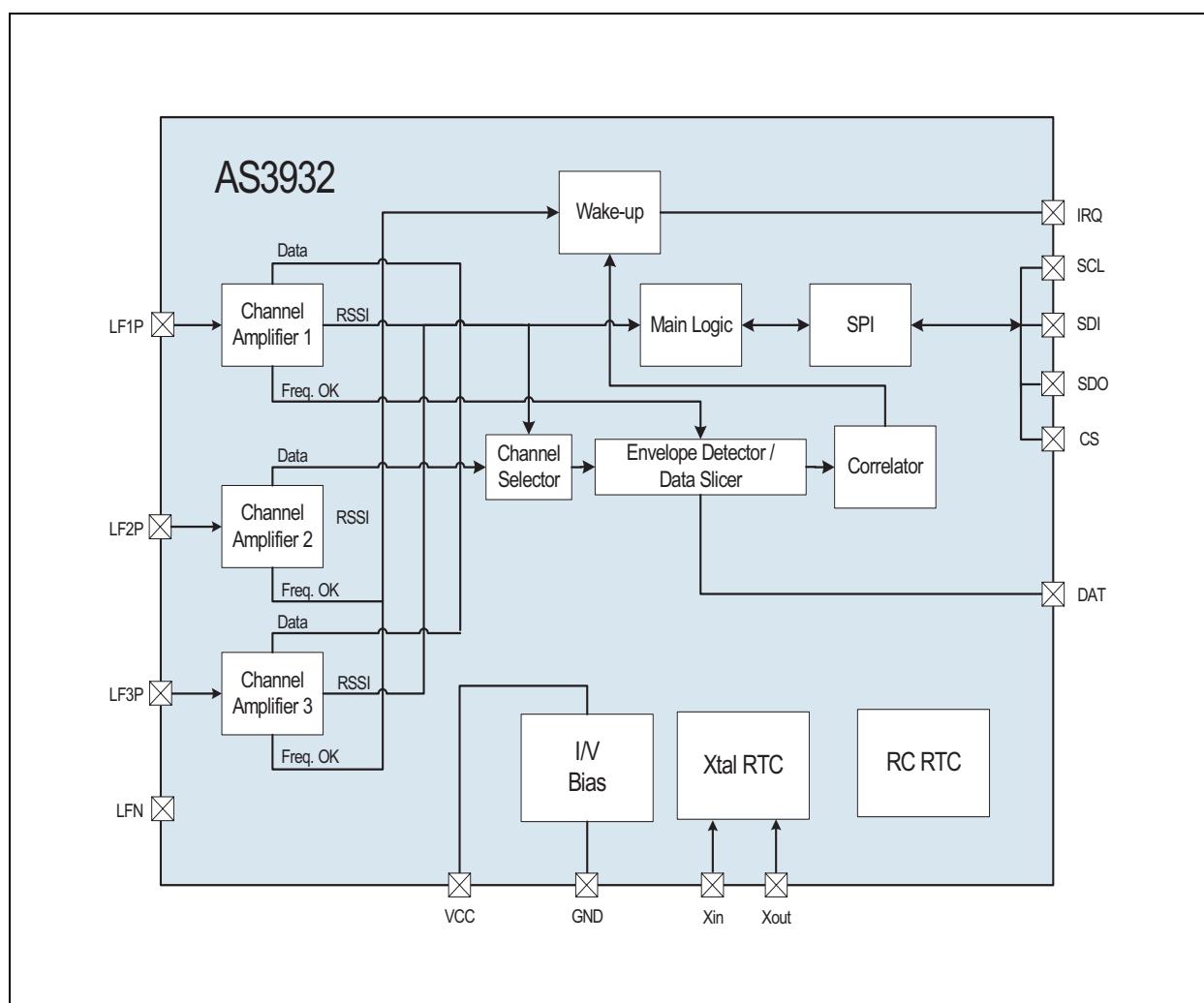
AS3932 needs the following external components:

- Power supply capacitor - CBAT - 100 nF.

- 32.768 kHz crystal with its two pulling capacitors - XTAL and CL - (it is possible to omit these components if the internal RC oscillator is used instead of the crystal oscillator).

- One, two, or three LC resonators according to the number of used channels.

In case the internal RC-oscillator is used (no crystal oscillator is mounted), the pin XIN has to be connected to the supply, while pin XOUT should stay floating. Application diagrams with and without crystal are shown in Figure 2 and Figure 3.

Operating Modes

Power Down Mode

In Power Down Mode AS3932 is completely switched OFF. The typical current consumption is 400 nA.

Listening Mode

In listening mode only the active channel amplifiers and the RTC are running. In this mode the system detects the presence of a carrier. In case the carrier is detected the RSSI can be displayed.

If the three dimensional detection is not required it is possible to deactivate one or more channels. In case only two channels are required the deactivated channel must be the number two, while if only one channel detection is needed the active channel must be the number one.

Inside this mode it is possible to distinguish the following three sub modes:

Standard Listening Mode. All channels are active at the same time.

Scanning Mode (Low Power Mode 1). All used channels are active, but only one per time slot, where the time slot T is defined as 1ms. Thus, if all three channels are active the procedure is as follows (see Figure 17): for the first millisecond only channel one is active while channel two and three are powered down; for the next millisecond only channel three is active while channel one and two are powered down; finally, channel two is active while the other two are deactivated. This channel rotation goes on until the presence of the carrier is detected by any of the channels; then immediately all three channels will become active at the same time. Now AS3932 can perform a simultaneous multidirectional evaluation (on all three channels) of the field and evaluate which channel has the strongest RSSI. The channel with the highest RSSI will be put through to the demodulator.

In this way it is possible to perform multidirectional monitoring of the field with a current consumption of a single channel, keeping the sensitivity as good as if all channels are active at the same time.

Figure 17:
Scanning Mode
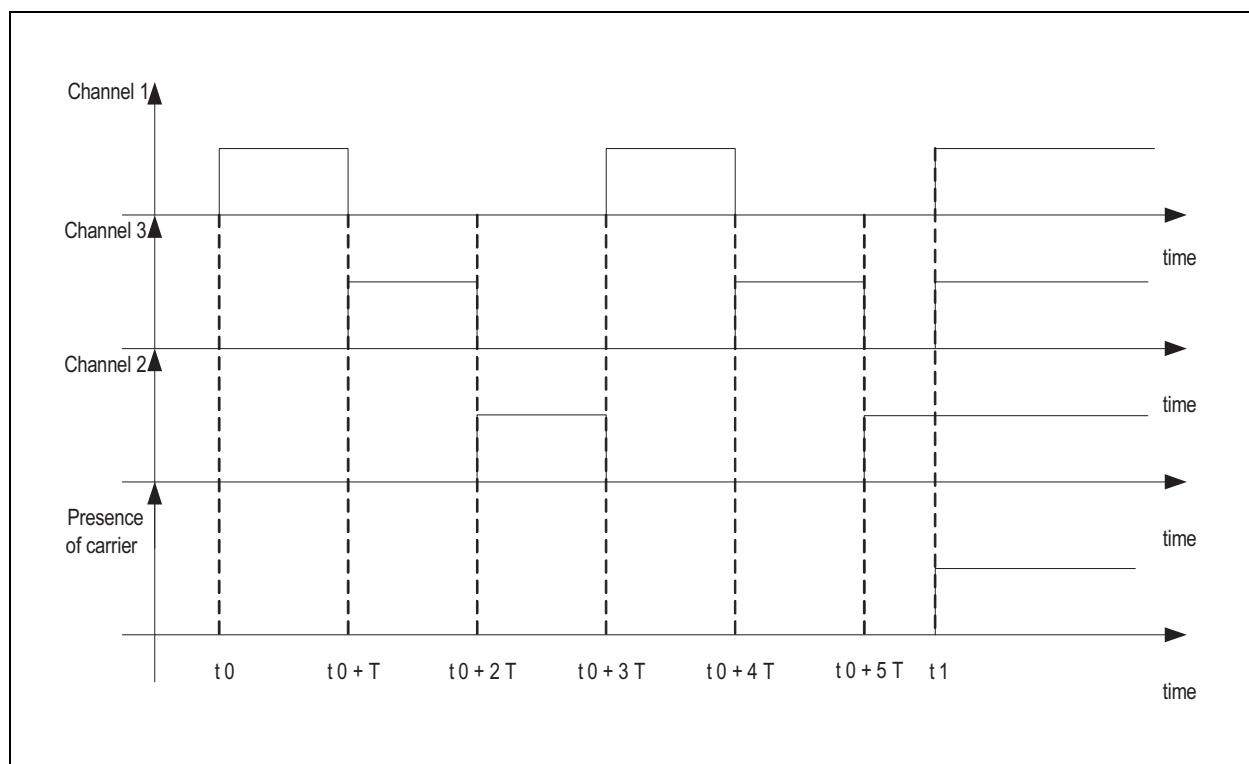
ON/OFF Mode (Low Power Mode 2). All active channels are ON at the same time but not for the whole time (time slot T is defined as 1ms). An ON-OFF duty-ratio is defined. This duty ratio is programmable see R4<7:6>.

**Figure 18:
ON/OFF Mode**
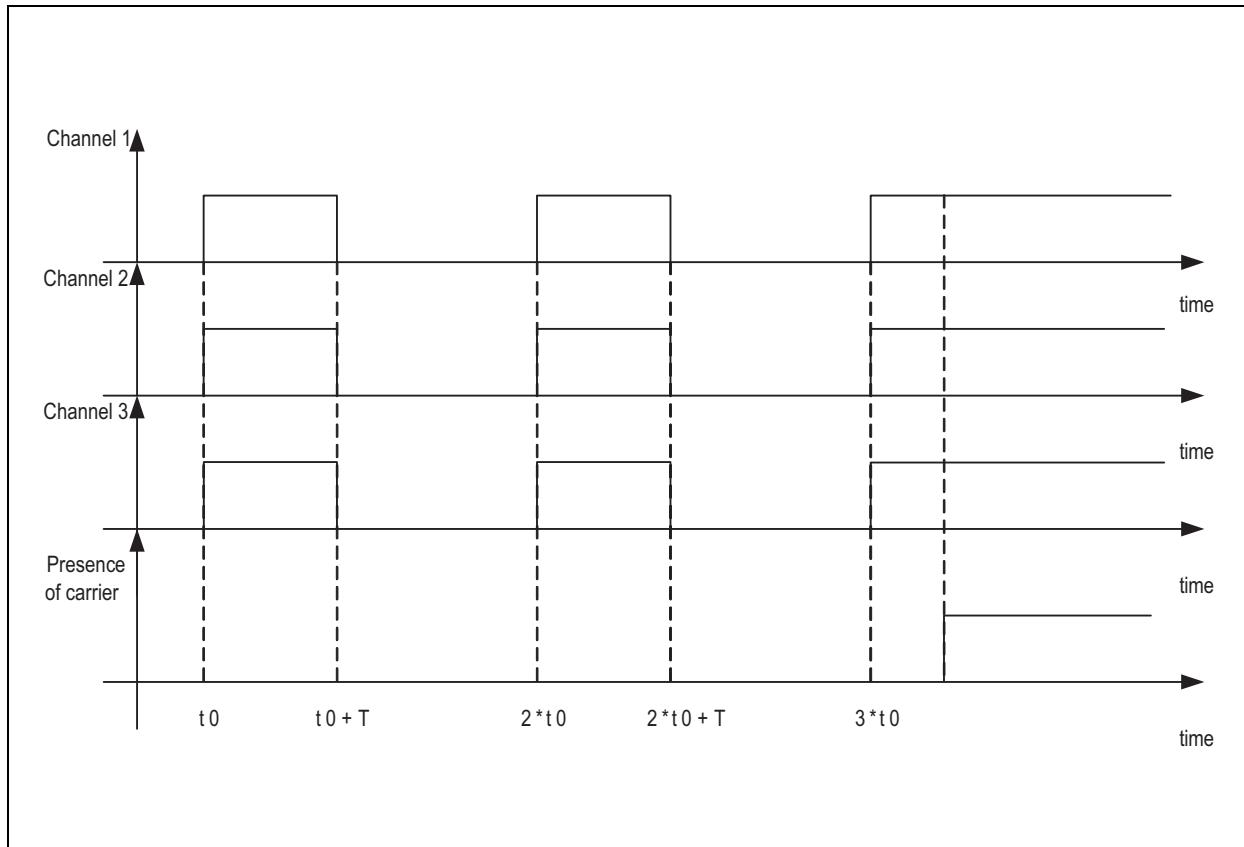
For each of these sub modes it is possible to enable a further feature called Artificial Wake-up. The Artificial Wake-up is a counter based on the used RTC. Three bits define a time window see R8<2:0>. If no activity is seen within this time window the chip will produce an interrupt on the WAKE pin that lasts 128µs. With this interrupt the microcontroller (µC) can get feedback on the surrounding environment (e.g. read the false wake-up register R13<7:0>) and/or take actions in order to change the setup.

Preamble Detection / Pattern Correlation

The preamble detection and pattern correlation are only considered for the wake-up when the data correlator function is enabled (see R1<1>). The correlator searches first for preamble frequency (constant frequency of Manchester clock defined according to bit-rate transmission, see Figure 37) and then for data pattern.

If the pattern is matched the wake-up interrupt is displayed on the WAKE output and the chip goes in Data receiving mode. If the pattern fails the internal wake-up (on all active channels) is terminated and no IRQ is produced.

Data Receiving

After a successful wake-up the chip enters the data receiving mode. In this mode the chip can be retained a normal OOK receiver. The received data are streamed out on the pin DAT. It is possible to put the chip back to listening mode either with a direct command (CLEAR_WAKE (see Figure 25)) or by using the timeout feature. This feature automatically sets the chip back to listening mode after a certain time R7<7:5>.

System and Block Specification

Register Table

Figure 19:
Register Table

	7	6	5	4	3	2	1	0
R0	n.a.		ON_OFF	MUX_123	EN_A2	EN_A3	EN_A1	PWD
R1	ABS_HY	AGC_TLIM	AGC_UD	ATT_ON		EN_PAT2	EN_WPAT	EN_RTC
R2	S_ABSH	W_PAT_T<1:0>		Reserved			S_WU1<1:0>	
R3	HY_20m	HY_POS	FS_SLC<2:0>			FS_ENV<2:0>		
R4	T_OFF<1:0>		R_VAL<1:0>		GR<3:0>			
R5	TS2<7:0>							
R6	TS1<7:0>							
R7	T_OUT<2:0>			T_HBIT<4:0>				
R8	n.a					T_AUTO<2:0>		
R9	n.a	Reserved						
R10	n.a			RSSI1<4:0>				
R11	n.a			RSSI3<4:0>				
R12	n.a			RSSI2<4:0>				
R13	F_WAKE							

Register Table Description and Default Values

Figure 20:
Default Values of Registers

Register	Name	Type	Default Value	Description
R0<5>	ON_OFF	R/W	0	ON/OFF operation mode. (Duty-cycle defined in the register R4<7:6>
R0<4>	MUX_123	R/W	0	Scan mode enable
R0<3>	EN_A2	R/W	1	Channel 2 enable
R0<2>	EN_A3	R/W	1	Channel 3 enable
R0<1>	EN_A1	R/W	1	Channel 1 enable
R0<0>	PWD	R/W	0	Power down
R1<7>	ABS_HY	R/W	0	Data slicer absolute reference
R1<6>	AGC_TLIM	R/W	0	AGC acting only on the first carrier burst
R1<5>	AGC_UD	R/W	1	AGC operating in both direction (up-down)
R1<4>	ATT_ON	R/W	0	Antenna damper enable
R1<2>	EN_PAT2	R/W	0	Double wake-up pattern correlation
R1<1>	EN_WPAT	R/W	1	Data correlation enable
R1<0>	EN_RTC	R/W	1	Crystal oscillator enable
R2<7>	S_ABSH	R/W	0	Data slicer threshold reduction
R2<6:5>	W_PAT	R/W	00	Pattern correlation tolerance (see Figure 38)
R2<4:2>	Reserved		000	Reserved
R2<1:0>	S_WU1	R/W	00	Tolerance setting for the stage wake-up (see Figure 32)
R3<7>	HY_20m	R/W	0	Data slicer hysteresis if HY_20m = 0 then comparator hysteresis = 40mV if HY_20m = 1 then comparator hysteresis = 20mV
R3<6>	HY_POS	R/W	0	Data slicer hysteresis on both edges (HY_POS = 0 → hysteresis on both edges; HY_POS = 1 → hysteresis only on positive edges)
R3<5:3>	FS_SCL	R/W	100	Data slicer time constant (see Figure 36)
R3<2:0>	FS_ENV	R/W	000	Envelop detector time constant (see Figure 35)

Register	Name	Type	Default Value	Description	
R4<7:6>	T_OFF	R/W	00	OFF time in ON/OFF operation mode	
				T_OFF=00	1ms
				T_OFF=01	2ms
				T_OFF=10	4ms
				T_OFF=11	8ms
R4<5:4>	D_RES	R/W	01	Antenna damping resistor (see Figure 34)	
R4<3:0>	GR	R/W	0000	Gain reduction (see Figure 33)	
R5<7:0>	TS2	R/W	01101001	2nd Byte of wake-up pattern	
R6<7:0>	TS1	R/W	10010110	1st Byte of wake-up pattern	
R7<7:5>	T_OUT	R/W	000	Automatic time-out (see Figure 39)	
R7<4:0>	T_HBIT	R/W	01011	Bit rate definition (see Figure 37)	
R8<2:0>	T_AUTO	R/W	000	Artificial wake-up	
				T_AUTO=000	No artificial wake-up
				T_AUTO=001	1 sec
				T_AUTO=010	5 sec
				T_AUTO=011	20 sec
				T_AUTO=100	2 min
				T_AUTO=101	15min
				T_AUTO=110	1 hour
				T_AUTO=111	2 hour
R9<6:0>	Reserved		000000	Reserved	
R10<4:0>	RSSI1	R		RSSI channel 1	
R11<4:0>	RSSI2	R		RSSI channel 2	
R12<4:0>	RSSI3	R		RSSI channel 3	
R13<7:0>	F_WAK	R		False wake-up register	

Serial Data Interface (SDI)

This 4-wires interface is used by the Microcontroller (μC) to program the AS3932. The maximum clock frequency of the SDI is 2MHz.

Figure 21:
Serial Data Interface (SDI) Pins

Name	Signal	Signal Level	Description
CS	Digital Input with pull down	CMOS	Chip Select
SDI	Digital Input with pull down	CMOS	Serial Data input for writing registers, data to transmit and/or writing addresses to select readable register
SDO	Digital Output	CMOS	Serial Data output for received data or read value of selected registers
SCLK	Digital Input with pull down	CMOS	Clock for serial data read and write

Note(s): SDO is set to tristate if CS is low. In this way more than one device can communicate on the same SDO bus.

SDI Command Structure. To program the SDI the CS signal has to go high. A SDI command is made up by a two bytes serial command and the data is sampled on the falling edge of SCLK. The Figure 22 shows how the command looks like, from the MSB (B15) to LSB (B0). The command stream has to be sent to the SDI from the MSB (B15) to the LSB (B0).

Figure 22:
SDI Command Structure

Mode		Register Address / Direct Command						Register Data						
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B3	B2	B1	B0

The first two bits (B15 and B14) define the operating mode. There are three modes available (write, read, direct command) plus one spare (not used), as shown in Figure 23.

Figure 23:
SDI Command Structure

B15	B14	Mode
0	0	WRITE
0	1	READ
1	0	NOT ALLOWED
1	1	DIRECT COMMAND

In case a write or read command happens the next 6 bits (B13 to B8) define the register address which has to be written respectively read, as shown in Figure 24.

Figure 24:
SDI Command Structure

B13	B12	B11	B10	B9	B8	Read/Write Register
0	0	0	0	0	0	R0
0	0	0	0	0	1	R1
0	0	0	0	1	0	R2
0	0	0	0	1	1	R3
0	0	0	1	0	0	R4
0	0	0	1	0	1	R5
0	0	0	1	1	0	R6
0	0	0	1	1	1	R7
0	0	1	0	0	0	R8
0	0	1	0	0	1	R9
0	0	1	0	1	0	R10
0	0	1	0	1	1	R11
0	0	1	1	0	0	R12
0	0	1	1	0	1	R13

The last 8 bits are the data that has to be written respectively read. A CS toggle high-low-high terminates the command mode.

If a direct command is sent (B15-B14=11) the bits from B13 to B8 defines the direct command while the last 8 bits are omitted. The Figure 25 shows all possible direct commands:

Figure 25:
List of Direct Commands

COMMAND_MODE	B13	B12	B11	B10	B9	B8
clear_wake	0	0	0	0	0	0
reset_RSSI	0	0	0	0	0	1
trim_osc	0	0	0	0	1	0
clear_false	0	0	0	0	1	1
preset_default	0	0	0	1	0	0

All direct commands are explained below:

- clear_wake: clears the wake state of the chip. In case the chip has woken up (WAKE pin is high) the chip is set back to listening mode.
- reset_RSSI: resets the RSSI measurement.
- trim_osc: starts the trimming procedure of the internal RC oscillator (see Figure 46).
- clear_false: resets the false wake-up register (R13<7:0>=00).
- preset_default: sets all register in the default mode, as shown in Figure 20.

Writing of Data to Addressable Registers (WRITE Mode). The SDI is sampled at the falling edge of SCLK (as shown in the following diagrams).

A CS toggling high-low-high indicates the end of the WRITE command after register has been written. The following example shows a write command.

Figure 26:
Writing of a Single Byte (falling edge sampling)
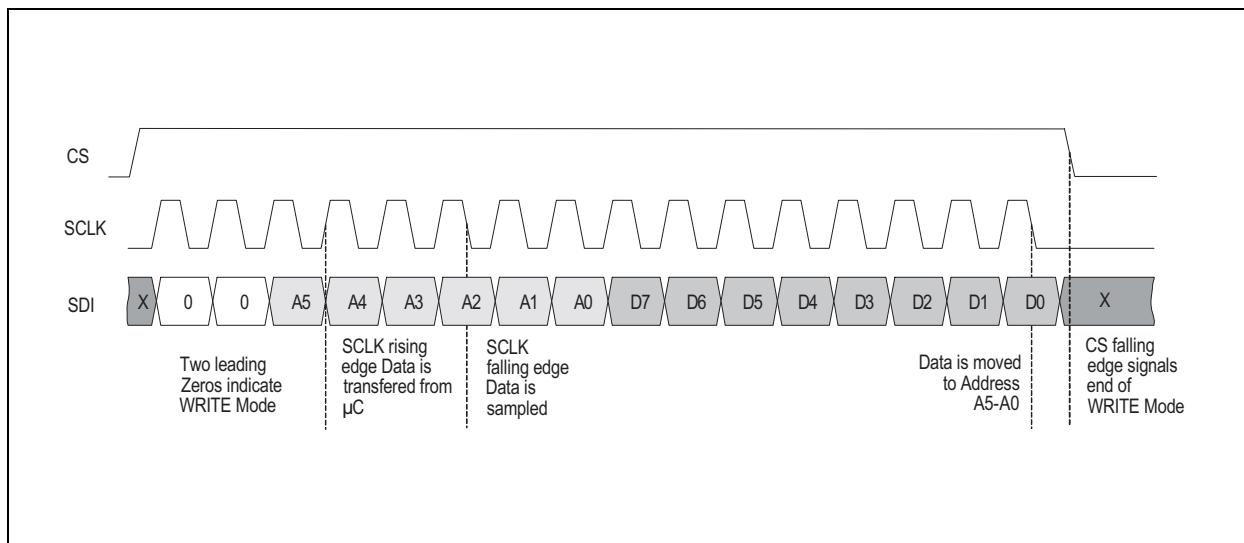
Figure 27:
**Writing of Register Data with Auto-incrementing Address**
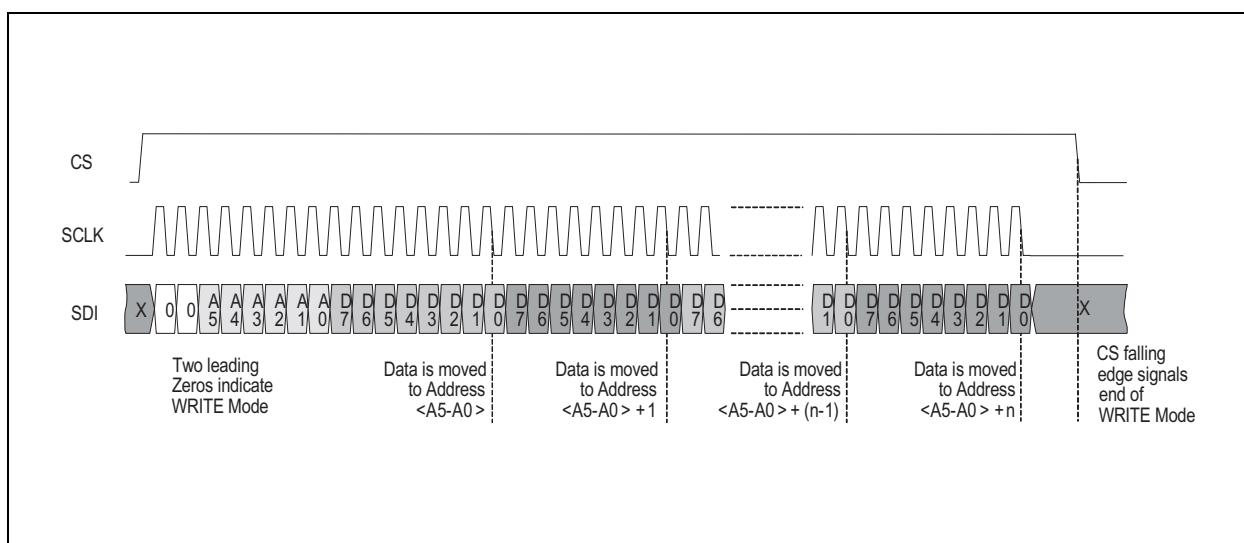
Reading of Data from Addressable Registers (READ Mode)
Once the address has been sent through SDI, the data can be fed through the SDO pin out to the microcontroller.

A CS LOW toggling high-low-high has to be performed after finishing the read mode session, in order to indicate the end of the READ command and prepare the Interface to the next command control Byte.

To transfer bytes from consecutive addresses, SDI master has to keep the CS signal high and the SCLK clock has to be active as long as data need to be read.

Figure 28:
Reading of Single Register Byte
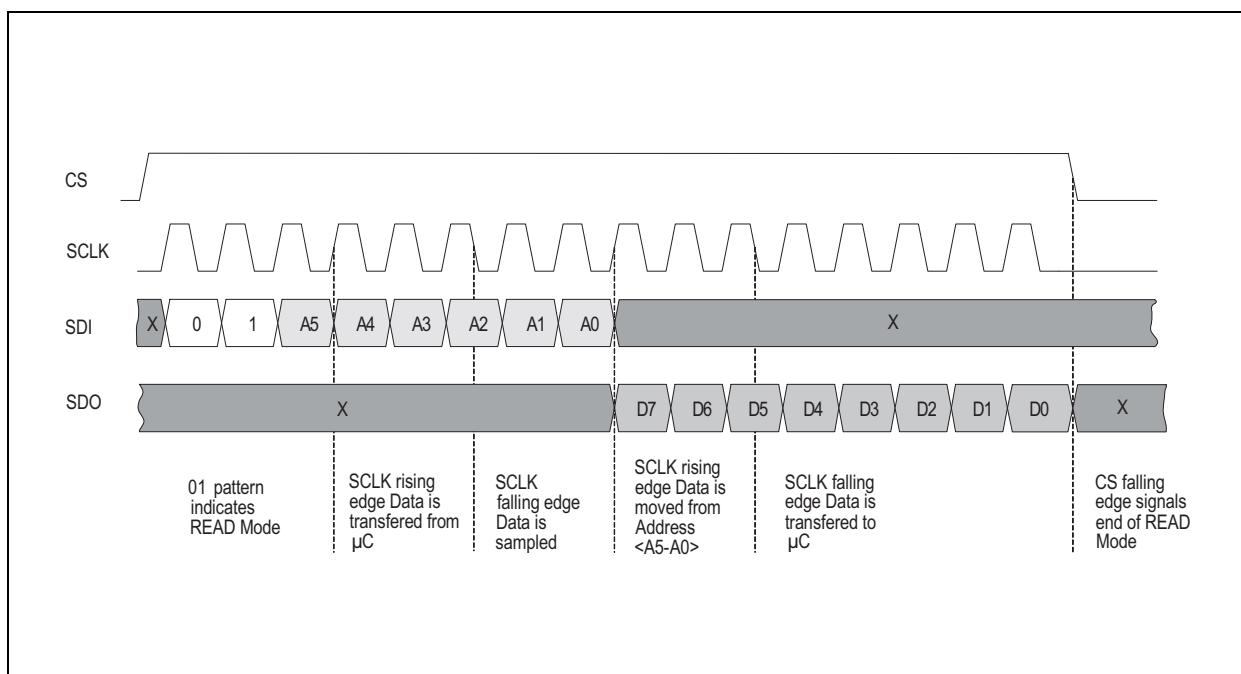
**Figure 29:**
Send Direct COMMAND Byte
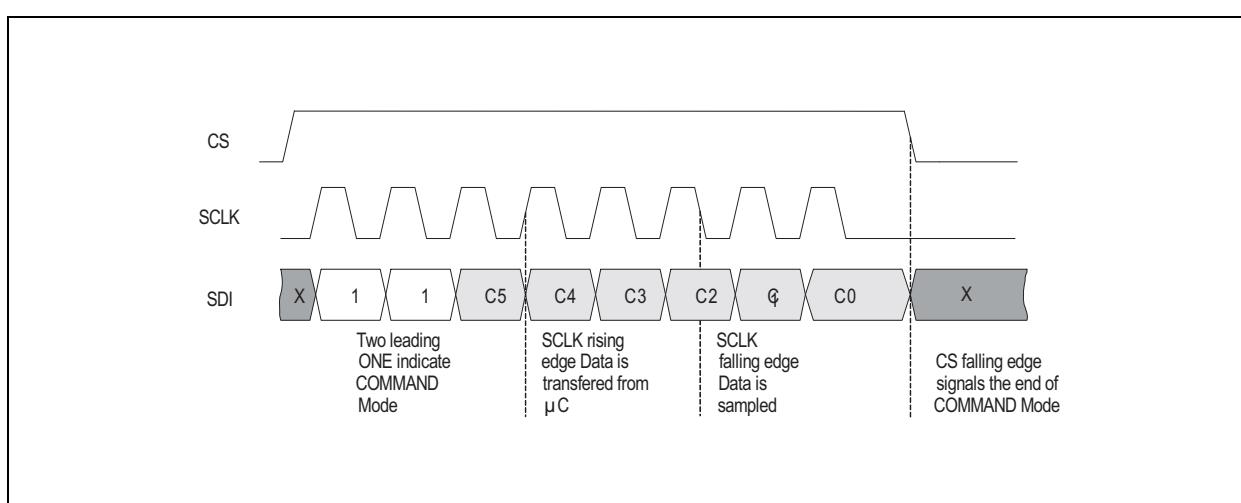
SDI Timing

Figure 30:
SDI Timing Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TCSCLK	Time CS to Sampling Data		500			ns
TDCLK	Time Data to Sampling Data		300			ns
THCL	SCLK High Time		200			ns
TCLK	SCLK period		500			ns
TCLKCS	Time Sampling Data to CS down		500			ns
TCST	CS Toggling time		500			ns

Figure 31:
SDI Timing Diagram
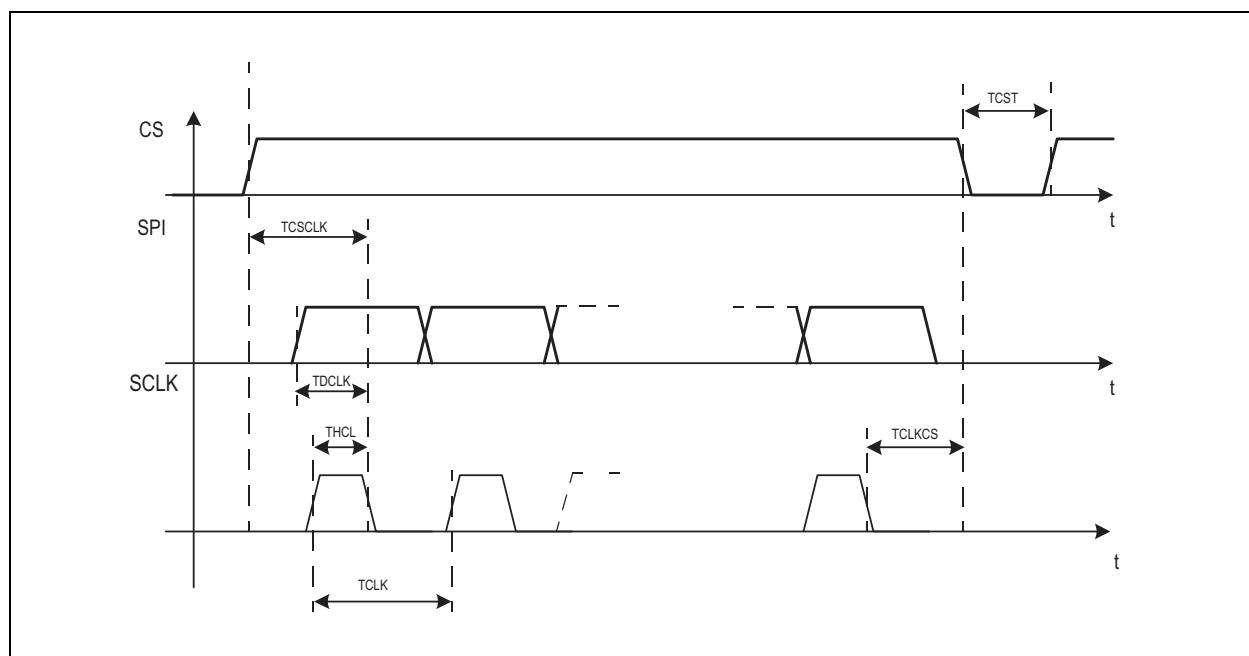
Channel Amplifier and Frequency Detector

Each of the 3 channels consists of a variable gain amplifier, an automatic gain control and a frequency detector. The latter detects the presence of a carrier. As soon as the carrier is detected the AGC is enabled, the gain of the VGA is reduced and set to the right value and the RSSI can be displayed.

It is possible to enable/disable individual channels, in case not all three channels are needed. This enables to reduce the current consumption by 1.5 µA (typ.) per channel.

Frequency Detector / AGC

The frequency detection uses the RTC as time base. In case the internal RC oscillator is used as RTC, it must be calibrated, but the calibration is guaranteed for a 32.768 kHz crystal oscillator only. The frequency detection criteria can be tighter or more relaxed according to the setup described in R2<1:0> (see Figure 32).

Figure 32:
Tolerance Settings for Wake-up

R2<1>	R2<0>	Tolerance
0	0	relaxed
0	1	tighter (medium)
1	0	stringent
1	1	reserved

The AGC can operate in two modes:

- AGC down only (R1<5>=0)
- AGC up and down (R1<5>=1)

As soon as the AGC starts to operate, the gain in the VGA is set to maximum. If the AGC down only mode is selected, the AGC can only decrease the gain. Since the RSSI is directly derived from the VGA gain, the system holds the RSSI peak.

When the AGC up and down mode is selected, the RSSI can follow the input signal strength variation in both directions.

Regardless which AGC operation mode is used, the AGC needs maximum 35 carrier periods to settle.

The RSSI is available for all 3 channels at the same time and it is stored in 3 registers (R10<4:0>, R11<4:0>, R12<4:0>)

Both AGC modes (only down or down and up) can also operate with time limitation. This option allows AGC operation only in time slot of 256µs following the internal wake-up. Then the AGC (RSSI) is frozen till the wake-up or RSSI reset occurs.

The RSSI is reset either with the direct command 'clear_wakeup' or 'reset_RSSI'. The 'reset_RSSI' command resets only the AGC setting but does not terminate wake-up condition. This means that if the signal is still present the new AGC setting (RSSI) will appear not later than 300μs (35 LF carrier periods) after the command was received. The AGC setting is reset if for duration of 3 Manchester half symbols no carrier is detected. If the wake-up IRQ is cleared the chip will go back to listening mode.

In case the maximum amplification at the beginning is a drawback (e.g. in noisy environment) it is possible to set a smaller starting gain on the amplifier, according to the Figure 33. In this way it is possible to reduce the false frequency detection.

Figure 33:
Bit Setting of Gain Reduction

R4<3>	R4<2>	R4<1>	R4<0>	Gain Reduction
0	0	0	0	No gain reduction
0	0	0	1	n.a.
0	0	1	0 or 1	n.a.
0	1	0	0 or 1	-4dB
0	1	1	0 or 1	-8dB
1	0	0	0 or 1	-12dB
1	0	1	0 or 1	-16dB
1	1	0	0 or 1	-20dB
1	1	1	0 or 1	-24dB

Antenna Damper

The antenna damper allows the chip to deal with higher field strength, it is enabled by register R1<4>. It consists of shunt resistors which degrade the quality factor of the resonator by reducing the signal at the input of the amplifier. In this way the resonator sees a smaller parallel resistance (in the band of interest) which degrades its quality factor in order to increase the linear range of the channel amplifier (the amplifier doesn't saturate in presence of bigger signals). Figure 34 shows the bit setup.

Figure 34:
Antenna Damper Bit Setup

R4<5>	R4<4>	Shunt Resistor (parallel to the resonator at 125 kHz)
0	0	1 kΩ
0	1	3 kΩ
1	0	9 kΩ
1	1	27 kΩ

Channel Selector / Demodulator / Data Slicer

When at least one of three gain channel enters initial wake-up state the channel selector makes a decision which gain channel to connect to the envelope detector. If only one channel is in wake-up state the selection is obvious. If more than one channel enters wake-up state in 256µs following the first active channel the channel with highest RSSI value is selected. The output signal (amplified LF carrier) of selected channel is connected to the input of the demodulator.

The performance of the demodulator can be optimized according to bit rate and preamble length as described in Figure 35 and Figure 36.

Figure 35:
Bit Setup for the Envelop Detector for Different Symbol Rate

R3<2>	R3<1>	R3<0>	Symbol Rate [Manchester symbols/s]
0	0	0	4096
0	0	1	2184
0	1	0	1490
0	1	1	1130
1	0	0	910
1	0	1	762
1	1	0	655
1	1	1	512

If the bit rate gets higher the time constant in the envelop detector must be set to a smaller value. This means that higher noise is injected because of the wider band. The next table is a rough indication of how the envelop detector looks like for different bit rates. By using proper data slicer settings it is possible to improve the noise immunity paying the penalty of a longer preamble. In fact if the data slicer has a bigger time constant it is possible to reject more noise, but every time a transmission occurs, the data slicer need time to settle. This settling time will influence the length of the preamble. Figure 36 gives a correlation between data slicer setup and minimum required preamble length.

Figure 36:
Bit Setup for the Data Slicer for Different Preamble Length

R3<5>	R3<4>	R3<3>	Minimum Preamble Length [ms]
0	0	0	0.8
0	0	1	1.15
0	1	0	1.55
0	1	1	1.9
1	0	0	2.3
1	0	1	2.65
1	1	0	3
1	1	1	3.5

Note(s): These times are minimum required, but it is recommended to prolong the preamble.

The comparator of the data slicer can work only with positive or with symmetrical threshold (R3<6>). In addition the threshold can be 20 or 40 mV (R3<7>).

In case the length of the preamble is an issue the data slicer can also work with an absolute threshold (R1<7>). In this case the bits R3<2:0> would not influence the performance. It is even possible to reduce the absolute threshold in case the environment is not particularly noisy (R2<7>).

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Correlator

After frequency detection the data correlation is only performed if the correlator is enabled (R1<1>=1).

The data correlation consists of checking the presence of a preamble (ON/OFF modulated carrier) followed by a certain pattern.

After the frequency detection the correlator waits 16 bits (see bit rate definition in Figure 37) and if no preamble is detected the chip is set back to listening mode and the false wake-up register (R13<7:0>) is incremented by one.

To get started with the pattern correlation the correlator needs to detect at least 4 bits of the preamble (ON/OFF modulated carrier).

The bit duration is defined in the register R7<4:0> according to the Figure 37 as function of the Real Time Clock (RTC) periods.

Figure 37:
Bit Rate Setup

R7<4>	R7<3>	R7<2>	R7<1>	R7<0>	Bit Duration in RTC Clock Periods	Bit Rate (bits/s)	Symbol Rate (Manchester symbols/s)
0	0	0	1	1	4	8192	4096
0	0	1	0	0	5	6552	3276
0	0	1	0	1	6	5460	2730
0	0	1	1	0	7	4680	2340
0	0	1	1	1	8	4096	2048
0	1	0	0	0	9	3640	1820
0	1	0	0	1	10	3276	1638
0	1	0	1	0	11	2978	1489
0	1	0	1	1	12	2730	1365
0	1	1	0	0	13	2520	1260
0	1	1	0	1	14	2340	1170
0	1	1	1	0	15	2184	1092
0	1	1	1	1	16	2048	1024
1	0	0	0	0	17	1926	963
1	0	0	0	1	18	1820	910
1	0	0	1	0	19	1724	862
1	0	0	1	1	20	1638	819

R7<4>	R7<3>	R7<2>	R7<1>	R7<0>	Bit Duration in RTC Clock Periods	Bit Rate (bits/s)	Symbol Rate (Manchester symbols/s)
1	0	1	0	0	21	1560	780
1	0	1	0	1	22	1488	744
1	0	1	1	0	23	1424	712
1	0	1	1	1	24	1364	682
1	1	0	0	0	25	1310	655
1	1	0	0	1	26	1260	630
1	1	0	1	0	27	1212	606
1	1	0	1	1	28	1170	585
1	1	1	0	0	29	1128	564
1	1	1	0	1	30	1092	546
1	1	1	1	0	31	1056	528
1	1	1	1	1	32	1024	512

If the preamble is detected correctly the correlator keeps searching for a data pattern. The duration of the preamble plus the pattern should not be longer than 40 bits (see bit rate definition in Figure 37). The data pattern can be defined by the user and consists of two bytes which are stored in the registers R5<7:0> and R6<7:0>. The two bytes define the pattern consisting of 16 half bit periods. This means the pattern and the bit period can be selected by the user. The only limitation is that the pattern (in combination with preamble) must obey Manchester coding and timing. It must be noted that according to Manchester coding a down-to-up bit transition represents a symbol "0", while a transition up-to-down represents a symbol "1". If the default code is used (96 [hex]) the binary code is (10 01 01 10 01 10 10 01). MSB has to be transmitted first.

The user can also select (R1<2>) if single or double data pattern is used for wake-up. In case double pattern detection is set, the same pattern has to be repeated 2 times.

Additionally it is possible to set the number of allowed missing zero bits (not symbols) in the received bitstream (R2<6:5>), as shown in the Figure 38.

Figure 38:
Allowed Pattern Detection Errors

R2<6>	R2<5>	Maximum Allowed Error in the Pattern Detection
0	0	No error allowed
0	1	1 missed zero
1	0	2 missed zeros
1	1	3 missed zeros

If the pattern matches the wake-up, interrupt is displayed on the WAKE output.

If the pattern detection fails, the internal wake-up (on all active channels) is terminated with no signal sent to MCU and the false wake-up register will be incremented (R13<7:0>).

Wake-up Protocol - Carrier Frequency 125 kHz

The wake-up state is terminated with the direct command 'clear_wake' Figure 25. This command terminates the MCU activity. The termination can also be automatic in case there is no response from MCU. The time out for automatic termination is set in a register R7<7:5>, as shown in the Figure 39.

Figure 39:
Timeout Setup

R7<7>	R7<6>	R7<5>	Time Out
0	0	0	0 sec
0	0	1	50 msec
0	1	0	100 msec
0	1	1	150 msec
1	0	0	200 msec
1	0	1	250 msec
1	1	0	300 msec
1	1	1	350 msec

Without Pattern Detection

Figure 40:
Wake-up Protocol Overview without Pattern Detection (only carrier frequency detection)
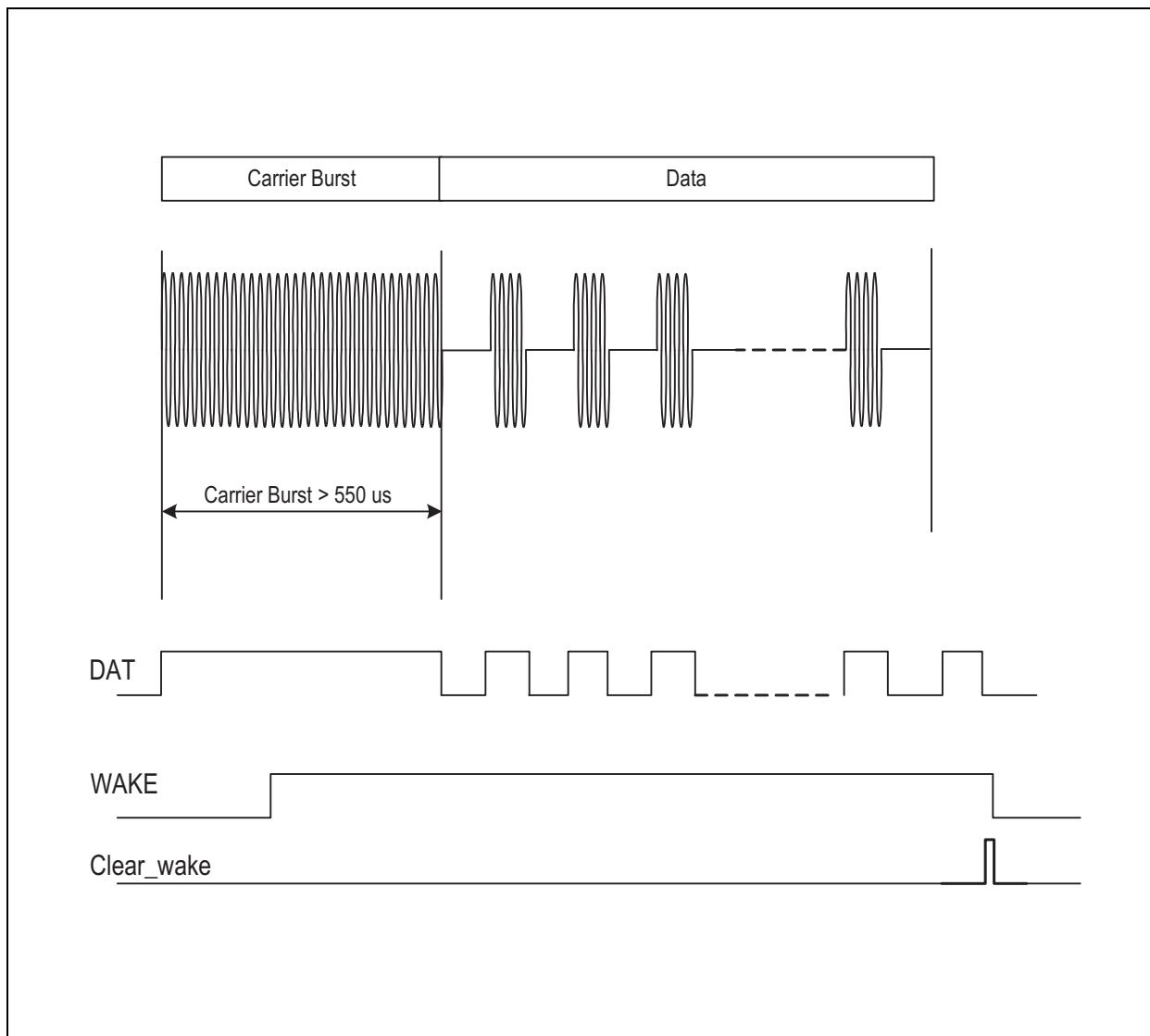
In case the data correlation is disabled (R1<1>=0) the AS3932 wakes up upon detection of the carrier frequency only as shown in Figure 40. In order to ensure that AS3932 wakes up the carrier burst has to last longer than 550 µs. To set AS3932 back to listening mode there are two possibilities: either the microcontroller sends the direct command clear_wake via SDI or the time out option is used (R7<7:5>). In case the latter is chosen, AS3932 is automatically set to listening mode after the time defined in T_OUT (R7<7:5>), counting starts at the low-to-high WAKE edge on the WAKE pin.

Single Pattern Detection

The Figure 41 shows the wake-up protocol in case the pattern correlation is enabled (R1<1>=1) for a 125 kHz carrier frequency. The initial carrier burst has to be longer than 550 µs and can last maximum 16 bits (see bit rate definition in Figure 37). If the ON/OFF mode is used (R1<5>=1), the minimum value of the maximum carrier burst duration is limited to 10 ms. This is summarized in Figure 42. In case the carrier burst is too long the internal wake-up will be set back to low and the false wake-up counter (R13<7:0>) will be incremented by one. The carrier burst must be followed by a preamble (0101... modulated carrier with a bit duration defined in Figure 37) and the wake-up pattern stored in the registers R5<7:0> and R6<7:0>. The preamble must have at least 4 bits and the preamble duration together with the pattern should not be longer than 40 bits. If the wake-up pattern is correct, the signal on the WAKE pin goes high one bit after the end of the pattern and the data transmission can get started. To set the chip back to listening mode the direct command clear_wake, as well as the time out option (R7<7:5>) can be used.

Figure 41:
Wake-up Protocol Overview with Single Pattern Detection
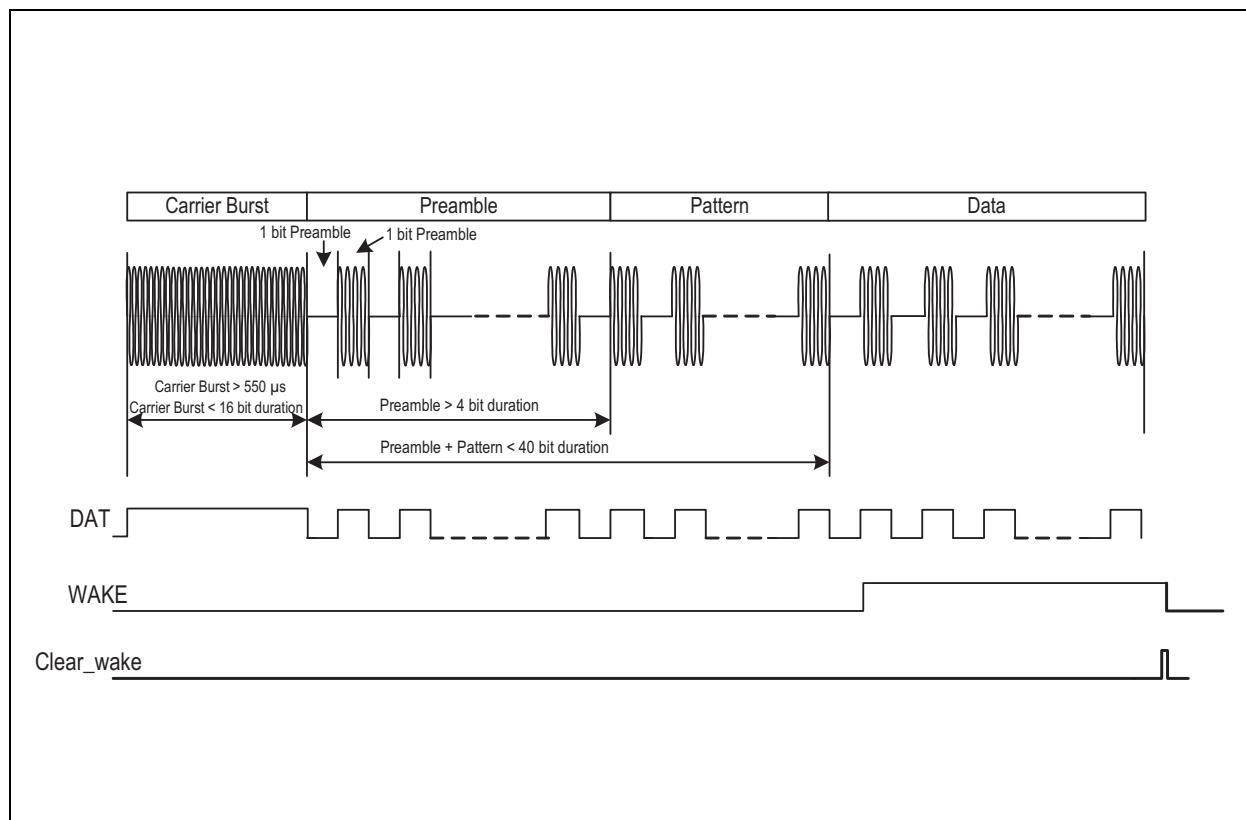
Figure 42:

Preamble Requirements in Standard Mode, Scanning Mode and ON/OFF Mode

Bit Rate (bits/s)	Maximum Duration of The Carrier Burst in Standard Mode and Scanning Mode (ms)	Maximum Duration of the Carrier Burst in ON/OFF Mode (ms)
8192	1.95	10
6552	2.44	10
5460	2.93	10
4680	3.41	10
4096	3.90	10
3640	4.39	10
3276	4.88	10
2978	5.37	10
2730	5.86	10
2520	6.34	10
2340	6.83	10
2184	7.32	10
2048	7.81	10
1926	8.30	10
1820	8.79	10
1724	9.28	10
1638	9.76	10
1560	10.25	10.25
1488	10.75	10.75
1424	11.23	11.23
1364	11.73	11.73
1310	12.21	12.21
1260	12.69	12.69
1212	13.20	13.20
1170	13.67	13.67
1128	14.18	14.18
1092	14.65	14.65

Bit Rate (bits/s)	Maximum Duration of The Carrier Burst in Standard Mode and Scanning Mode (ms)	Maximum Duration of the Carrier Burst in ON/OFF Mode (ms)
1056	15.15	15.15
1024	15.62	15.62

False Wake-up Register

The wake-up strategy in the AS3932 is based on 2 steps:

1. Frequency Detection: in this phase the frequency of the received signal is checked.

2. Pattern Correlation: here the pattern is demodulated and checked whether it corresponds to the valid one.

If there is a disturber or noise capable to overcome the first step (frequency detection) without producing a valid pattern, then a false wake-up call happens.Each time this event is recognized a counter is incremented by one and the respective counter value is stored in a memory cell (false wake-up register). Thus, the microcontroller can periodically look at the false wake-up register, to get a feeling how noisy the surrounding environment is and can then react accordingly (e.g. reducing the gain of the LNA during frequency detection, set the AS3932 temporarily to power down etc.), as shown in the Figure 43. The false wake-up counter is a useful tool to quickly adapt the system to any changes in the noise environment and thus avoid false wake-up events.

Most wake-up receivers have to deal with environments that can rapidly change. By periodically monitoring the number of false wake-up events it is possible to adapt the system setup to the actual characteristics of the environment and enables a better use of the full flexibility of AS3932.

Figure 43:
Concept of the False Wake-up Register Together With the System
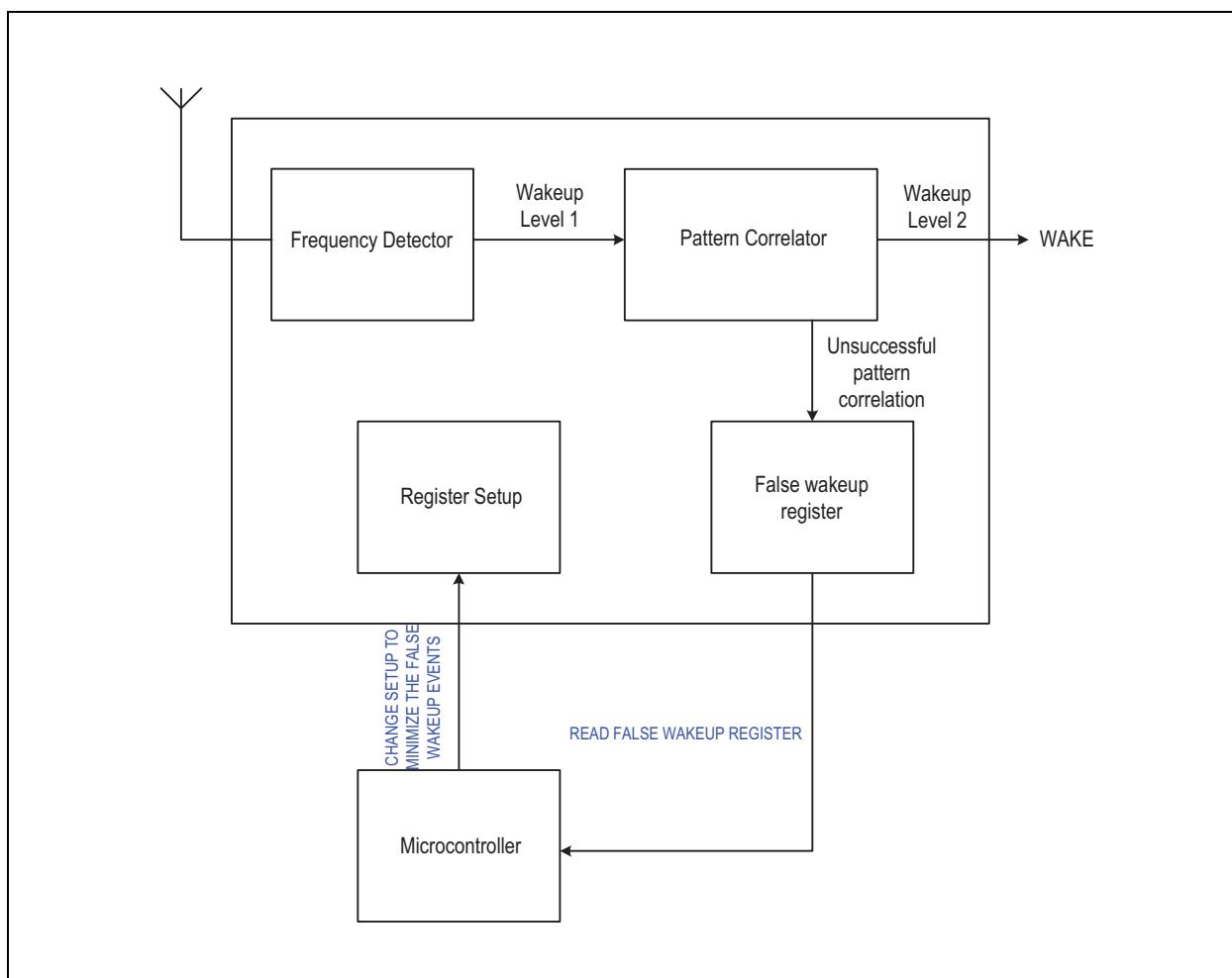
Real Time Clock (RTC)

The RTC can be based on a crystal oscillator (R1<0>=1), the internal RC-oscillator (R1<0>=0), or an external clock source (R1<0>=1). The crystal oscillator has higher precision of the frequency with higher current consumption and needs three external components (crystal plus two capacitors). The RC-oscillator is completely integrated and can be calibrated if a reference signal is available for a very short time to improve the frequency accuracy. The calibration gets started with the trim_osc direct command. Since no non-volatile memory is available the calibration must be done every time after the RCO is turned OFF. The RCO is turned OFF when the chip is in power down mode, a POR happened, or the crystal oscillator is enabled.

Since the RTC defines the time base of the frequency detection, the selected frequency (frequency of the crystal oscillator or the reference frequency used for calibration of the RC oscillator) should be about one forth of the carrier frequency:

(EQ1) $F_{RTC} \sim F_{CAR} * 0.25$

Where: F_{CAR} is the carrier frequency and F_{RTC} is the RTC frequency.

The third option for the RTC is the use of an external clock source, which must be applied directly to the XIN pin (XOUT floating).

Crystal Oscillator

Figure 44:
Characteristics of XTAL

Symbol	Parameter	Conditions	Min	Max	Typ	Units
	Crystal accuracy (initial)	Overall accuracy			±120	p.p.m.
	Crystal motional resistance				60	KΩ
	Frequency			32.768		kHz
	Contribution of the oscillator to the frequency error			±5		p.p.m
	Start-up Time	Crystal dependent		1		s
	Duty cycle		45	50	55	%
	Current consumption			1		μA

RC-Oscillator

Figure 45:
Characteristics of RCO

Symbol	Parameter	Conditions	Min	Max	Typ	Units
	Frequency	If no calibration is performed	27	32.768	42	kHz
		If calibration is performed	31	32.768	34.5	kHz
	Calibration time	Periods of reference clock			65	cycles
	Current consumption			200		nA

To trim the RC-Oscillator, set the chip select (CS) to high before sending the direct command trim_osc over SDI. Then 65 digital clock cycles of the reference clock (e.g. 32.768 kHz) have to be sent on the clock bus (SCLK), as shown in Figure 46. After that the signal on the chip select (CS) has to be pulled down.

The calibration is effective after the 65th reference clock edge and it will be stored in a volatile memory. In case the RC-oscillator is switched OFF or a power-on-reset happens (e.g. battery change) the calibration has to be repeated.

Figure 46:
RC-Oscillator Calibration via SDI
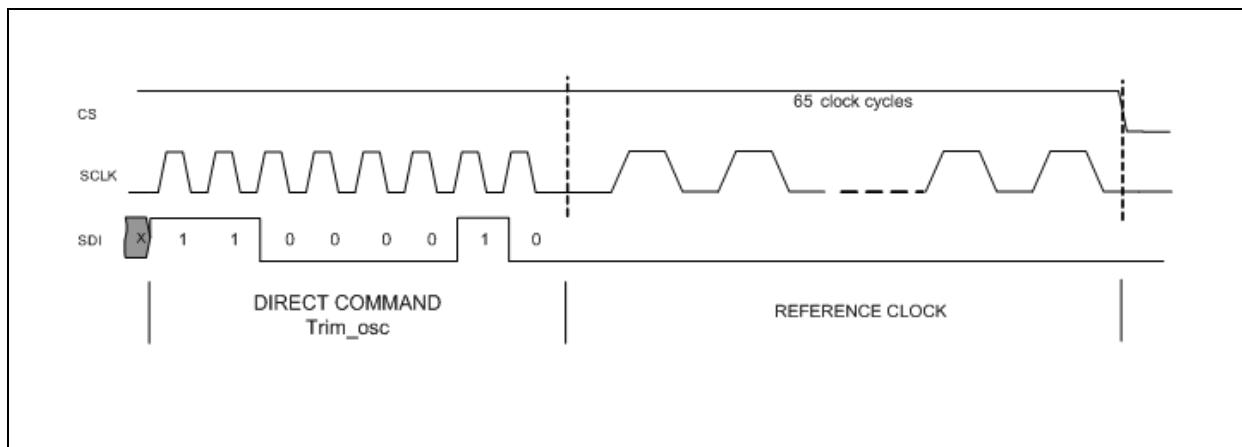
External Clock Source

To clock the AS3932 with an external signal the crystal oscillator has to be enabled (R1<0>=1). As shown in the Figure 4 the clock must be applied on the pin XIN while the pin XOUT must stay floating. The RC time constant has to be 15µs with a tolerance of ±10% (e.g. R=680 kΩ and C=22pF). In the Figure 47 the clock characteristics are summarized.

Figure 47:
Characteristics of External Clock

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vl	Low level		0		$0.1 * V_{DD}$	V
Vh	High level		$0.9 * V_{DD}$		V_{DD}	V
Tr	Rise-time				3	µs
Tf	Fall-time				3	µs
T = RC	RC Time constant		13.5	15	16.5	µs

Note(s): In power down mode the external clock has to be set to VDD.

Channel Selection in Scanning Mode and ON/OFF Mode

In case only 2 channels are active and one of the Low Power modes is enabled, then the channels 1 and 3 have to be active. If the chip works in ON-OFF mode and only one channel is active then the active channel has to be the channel 1.

Both Low Power modes are not allowed to be enabled at the same time.

Package Drawings & Markings

The product is available in a 16-pin TSSOP package.

Figure 48:
Drawings and Dimensions (TSSOP)

Symbol	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	5.00	5.10
E	-	6.40BSC	-
E1	4.30	4.40	4.50
e	-	0.65BSC	-
L	0.45	0.60	0.75
L1	-	1.00REF	-

Symbol	Min	Nom	Max
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ1	0°	-	8°
θ2	-	12REF	-
θ3	-	12REF	-
aaa	-	0.10	-
bbb	-	0.10	-
ccc	-	0.05	-
ddd	-	0.20	-
N		16	

Green

RoHS
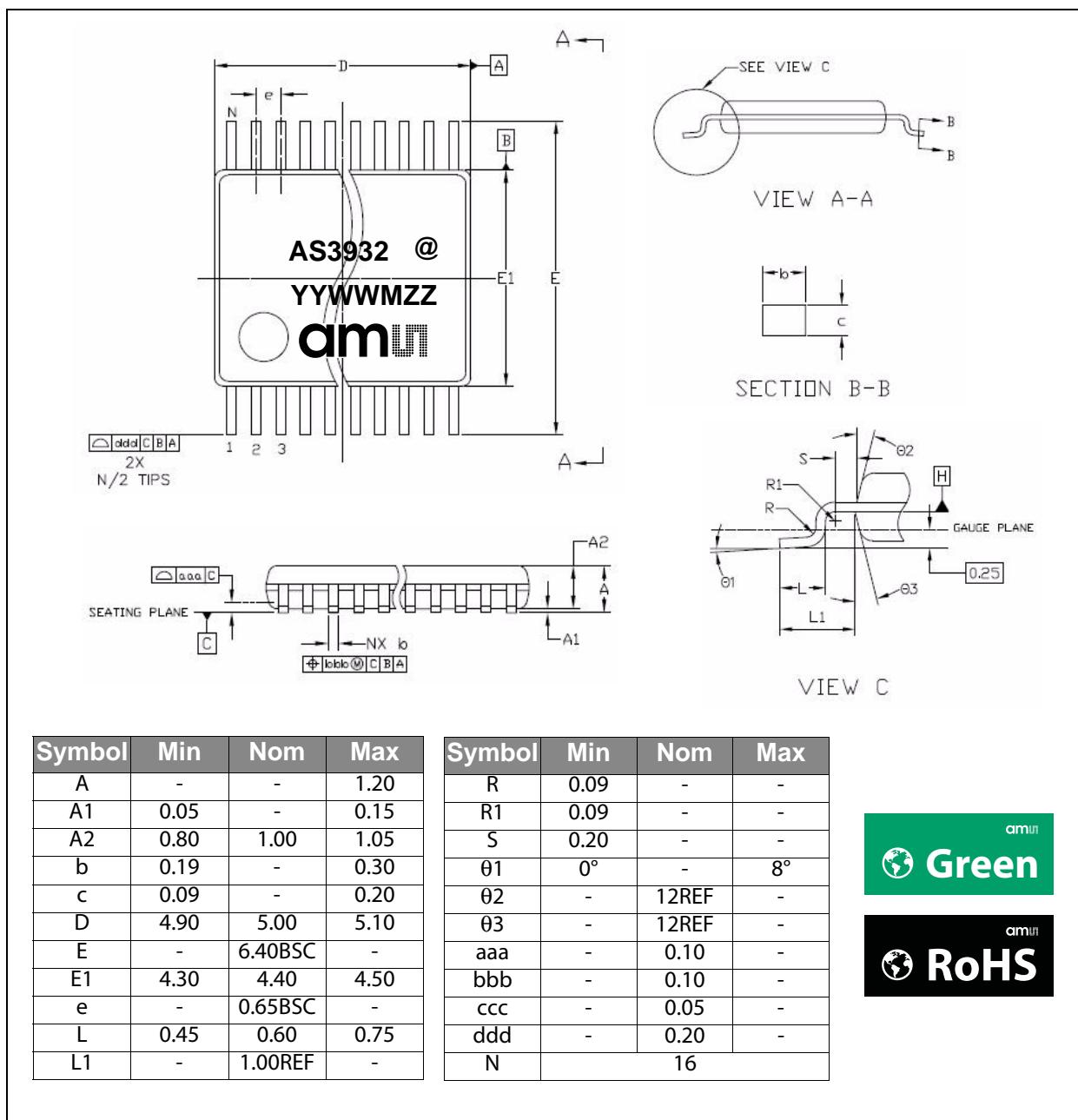
Note(s) and/or Footnote(s):

1. Dimensions and tolerancing conform to ASME Y14.5M-1994.

2. All dimensions are in millimeters. Angles are in degrees.

Figure 49:
Marking: YYWWMZZ

YY	WW	M	ZZ	@
Year (i.e. 10 for 2010)	Manufacturing Week	Assembly plant identifier	Assembly traceability code	Sublot identifier

The product is available in a 16LD QFN (4×4) package.

Figure 50:
Drawings and Dimensions (QFN)

REF.	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20 REF	
L	0.35	0.40	0.45
L1	0	-	0.15
b	0.25	0.30	0.35
D		4.00 BSC	
E		4.00 BSC	
e		0.65 BSC	
D2	2.30	2.40	2.50
E2	2.30	2.40	2.50
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		16	
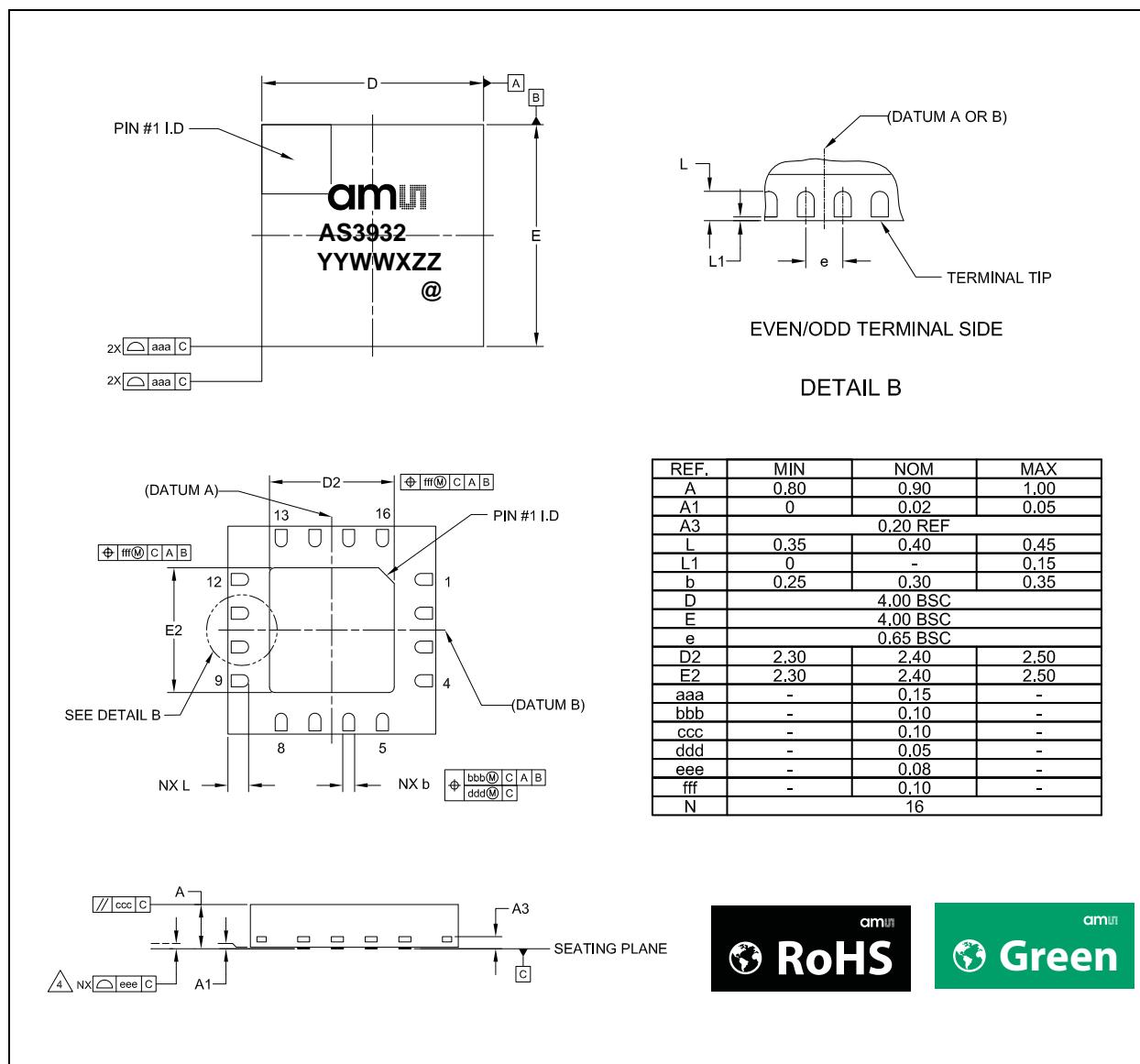
Note(s) and/or Footnote(s):

1. Dimensioning and tolerancing conform to *ASME Y14.5M-1994*.

2. All dimensions are in millimeters. Angles are in degrees.

3. Dimension b applies to metallized terminal and is measured between 0.25mm and 0.30mm from terminal tip. Dimension L1 represents terminal full back from package edge up to 0.15mm is acceptable.

4. Coplanarity applies to the exposed heat slug as well as the terminal.

5. Radius on terminal is optional.

6. N is the total number of terminals.

Figure 51:
Marking: YYWWXZZ

YY	WW	X	ZZ	@
Year (i.e. 10 for 2010)	Manufacturing Week	Assembly plant identifier	Assembly traceability code	Sublot identifier

Ordering & Contact Information

The devices are available as the standard products shown in Figure 52.

Figure 52:
Ordering Information

Ordering Code	Type	Marking	Delivery Form[1]	Delivery Quantity
AS3932-BTST	16-pin TSSOP	AS3932	7 inches Tape & Reel	1000 pcs
AS3932-BQFT	16LD QFN (4×4)	AS3932	7 inches Tape & Reel	1000 pcs

Note(s) and/or Footnote(s):

1. Dry Pack Sensitivity Level =3 according to IPC/JEDEC J-STD-033A for full reels.

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Headquarters
ams AG
Tobelbaderstrasse 30
8141 Unterpremstaetten
Austria, Europe

Tel: +43 (0) 3136 500 0

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

Changes from 1.7 (2013-Jun-18) to current revision 1-83 (2015-Mar-02)	Page
1.7 (2013-Jun-18) to 1-82 (2014-Nov-05)	
Content was converted to latest **ams** design	
Added benefits to Key Features	1
Added TRC (start-up time) parameter in Figure 11	9
Updated text under Detailed Description section	13
Updated Figure 30	25
1-82 (2014-Nov-05) to 1-83 (2015-Mar-02)	
Updated Figure 50 (QFN (4×4) package)	43

Note(s) and/or Footnote(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.

2. Correction of typographical errors is not explicitly mentioned.

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