

SN54LS640 THRU SN54LS642, SN54LS644, SN54LS645  
 SN74LS640 THRU SN74LS642, SN74LS644, SN74LS645  
 OCTAL BUS TRANSCEIVERS

SDLS189 - APRIL 1979 - REVISED MARCH 1988

- **SN74LS64X-1 Versions Rated at  $I_{OL}$  of 48 mA**
- **Bi-directional Bus Transceivers in High-Density 20-Pin Packages**
- **Hysteresis at Bus Inputs Improves Noise Margins**
- **Choice of True or Inverting Logic**
- **Choice of 3-State or Open-Collector Outputs**

DEVICE	OUTPUT	LOGIC
'LS640	3-State	Inverting
'LS641	Open-Collector	True
'LS642	Open-Collector	Inverting
'LS644	Open-Collector	True and inverting
'LS645	3-State	True

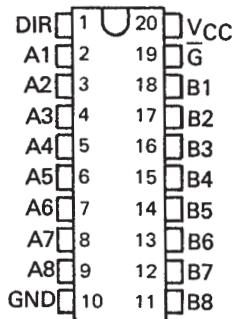
### description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G) can be used to disable the device so the buses are effectively isolated.

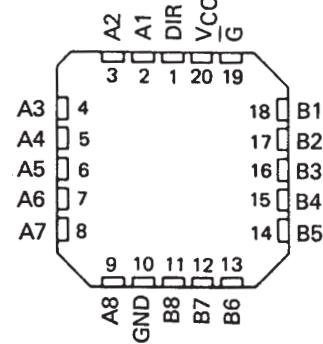
The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum  $I_{OL}$  is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54LS' . . . J PACKAGE  
 SN74LS' . . . DW OR N PACKAGE  
 (TOP VIEW)



SN54LS' . . . FK PACKAGE  
 (TOP VIEW)



### FUNCTION TABLE

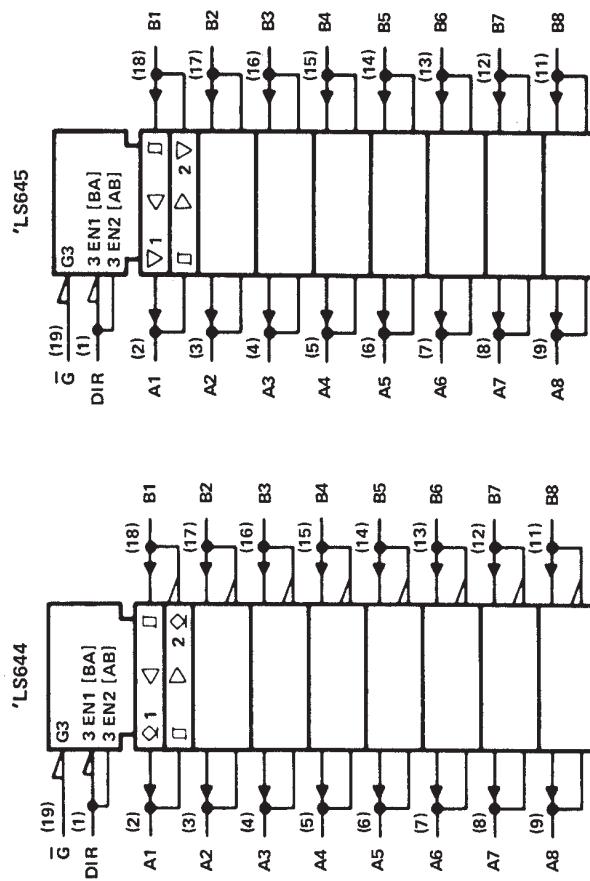
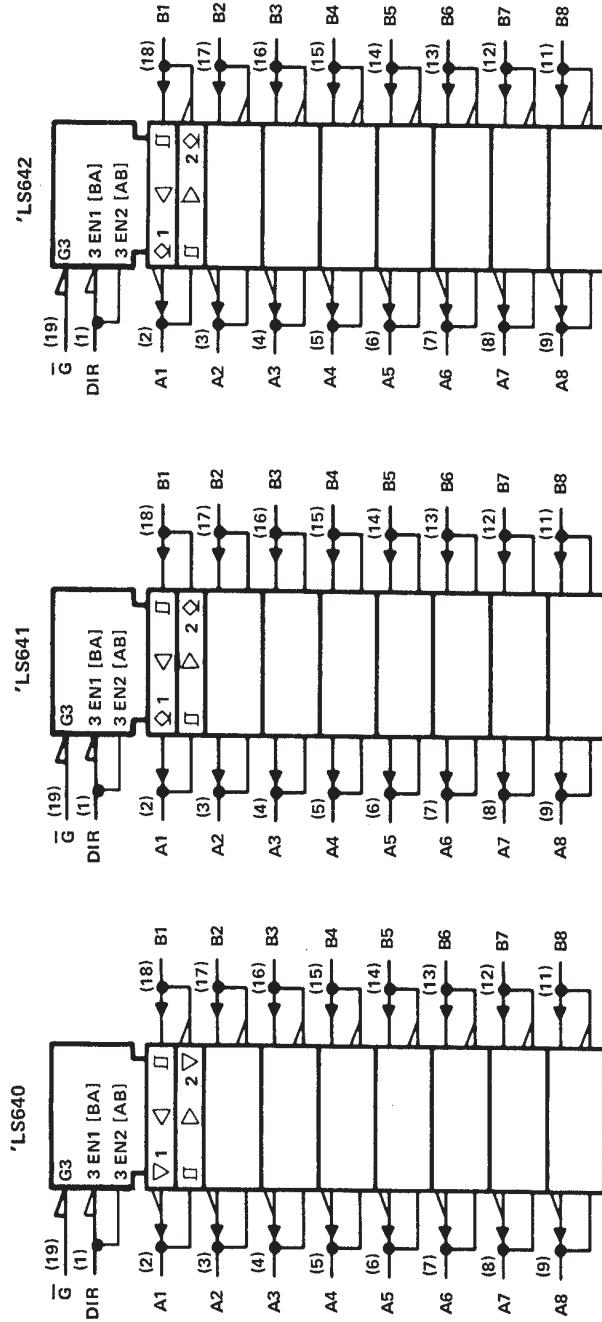
CONTROL INPUTS	OPERATION		
	'LS640 'LS642	'LS641 'LS645	'LS644
L L	B data to A bus	B data to A bus	B data to A bus
L H	A data to B bus	A data to B bus	$\bar{A}$ data to B bus
H X	Isolation	Isolation	Isolation

H = high level, L = low level, X = irrelevant

**SN54LS640 THRU SN54LS642, SN54LS644, SN54LS645  
SN74LS640 THRU SN74LS642, SN74LS644, SN74LS645  
OCTAL BUS TRANSCEIVRS**

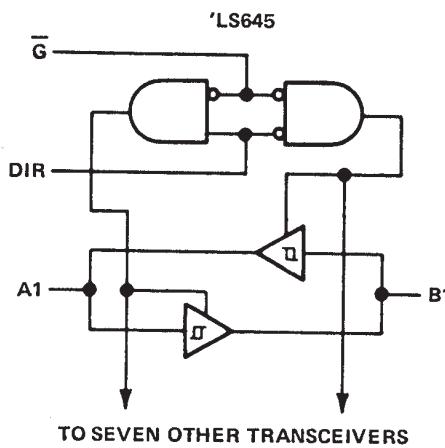
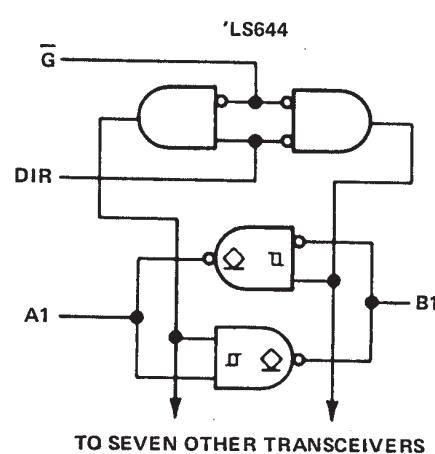
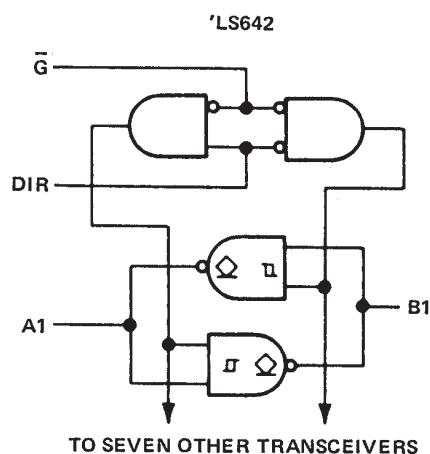
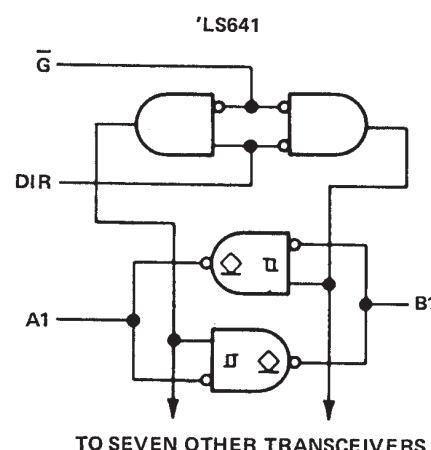
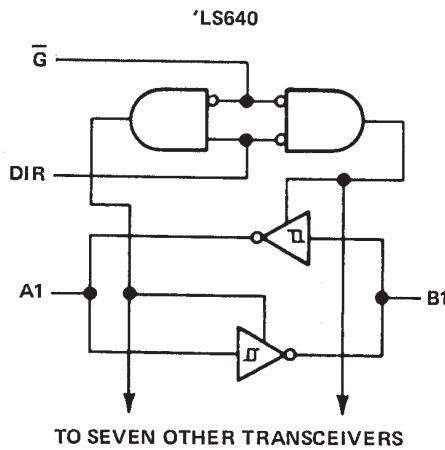
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**logic symbols<sup>†</sup>**



<sup>†</sup> These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for DW, J, and N packages.

logic diagrams (positive logic)



SN54LS640, SN54LS645

SN74LS640, SN74LS645

## OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . .	7 V
Input voltage: All inputs . . . . .	7 V
I/O ports . . . . .	5.5 V
Operating free-air temperature range: SN54LS640, SN54LS645 . . . . .	-55 °C to 125 °C
SN74LS640, SN74LS645 . . . . .	0 °C to 70 °C
Storage temperature range . . . . .	-65 °C to 150 °C

NOTE 1: Voltage values are with respect to network ground terminal.

### recommended operating conditions

PARAMETER	SN54LS640			SN74LS640			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.5			0.6	V
$I_{OH}$ High-level output current			-12			-15	mA
$I_{OL}$ Low-level output current			12			24	mA
						48 <sup>†</sup>	
$T_A$ Operating free-air temperature	-55	125	0	0	70	70	°C

<sup>†</sup>The 48-mA limit applies for the SN74LS640-1 and SN74LS645-1 only.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>‡</sup>			SN54LS640			SN74LS640			UNIT
	MIN	TYP <sup>§</sup>	MAX	MIN	TYP <sup>§</sup>	MAX	MIN	TYP <sup>§</sup>	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}$ , $I_I = -18 \text{ mA}$				-1.5			-1.5		V
Hysteresis ( $V_{T+} - V_{T-}$ )	$V_{CC} = \text{MIN}$ ,	A or B input		0.1	0.4		0.2	0.4		V
$V_{OH}$	$V_{CC} = \text{MIN}$ , $V_{IL} = \text{MAX}$	$I_{OH} = -3 \text{ mA}$	2.4	3.4		2.4	3.4			
		$I_{OH} = \text{MAX}$	2			2				
$V_{OL}$	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = \text{MAX}$	$I_{OL} = 12 \text{ mA}$	0.25	0.4		0.25	0.4			V
		$I_{OL} = 24 \text{ mA}$				0.35	0.5			
		$I_{OL} = 48 \text{ mA}^{\#}$				0.4	0.5			
$I_{OZH}$	$V_{CC} = \text{MAX}$ , $\bar{G}$ at 2 V,	$V_O = 2.7 \text{ V}$		20			20			μA
$I_{OZL}$	$V_{CC} = \text{MAX}$ , $\bar{G}$ at 2 V,	$V_O = 0.4 \text{ V}$		-0.4			-0.4			mA
$I_I$	A or B	$V_{CC} = \text{MAX}$	$V_I = 5.5 \text{ V}$		0.1		0.1			mA
	DIR or $\bar{G}$		$V_I = 7 \text{ V}$		0.1		0.1			
$I_{IH}$		$V_{CC} = \text{MAX}$ , $V_{IH} = 2.7 \text{ V}$		20			20			μA
$I_{IL}$		$V_{CC} = \text{MAX}$ , $V_{IL} = 0.4 \text{ V}$		-0.4			-0.4			mA
$I_{OS}$ <sup>¶</sup>		$V_{CC} = \text{MAX}$		-40	-225		-40	-225		mA
$I_{CC}$	Outputs high				48	70	48	70		mA
	Outputs low	$V_{CC} = \text{MAX}$ , Outputs open			62	90	62	90		
	Outputs at Hi-Z				64	95	64	95		

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup>All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25 \text{ °C}$ .

<sup>¶</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

<sup>#</sup>The 48-mA condition applies for the SN74LS640-1 and SN74LS645-1 only.



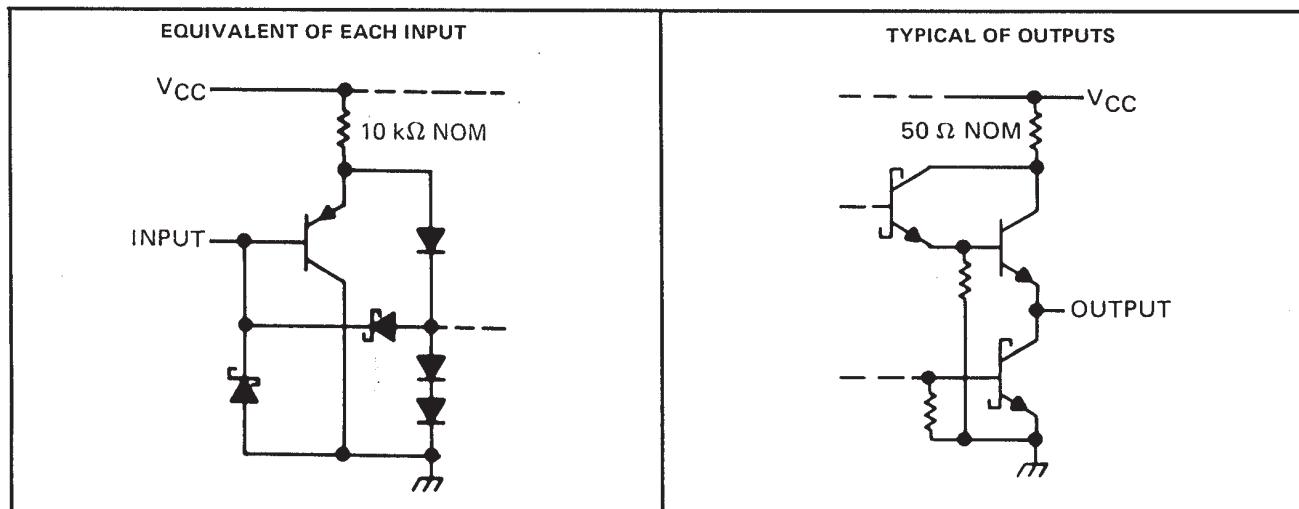
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switching characteristics,  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS640, 'LS640-1			'LS645, 'LS645-1			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH}$	A	B	$C_L = 45 \text{ pF}$ , $R_L = 667 \Omega$ , See Note 2	6	10	15	8	15	15	ns
	B	A		6	10	15	8	15	15	
$t_{PHL}$	A	B		8	15	15	11	15	15	ns
	B	A		8	15	15	11	15	15	
$t_{PZL}$	NOT	A	$C_L = 45 \text{ pF}$ , $R_L = 667 \Omega$ , See Note 2	31	40	40	31	40	40	ns
	NOT	B		31	40	40	31	40	40	
$t_{PZH}$	NOT	A		23	40	40	26	40	40	ns
	NOT	B		23	40	40	26	40	40	
$t_{PLZ}$	NOT	A	$C_L = 5 \text{ pF}$ , $R_L = 667 \Omega$ , See Note 2	15	25	25	15	25	25	ns
	NOT	B		15	25	25	15	25	25	
$t_{PHZ}$	NOT	A	$C_L = 5 \text{ pF}$ , $R_L = 667 \Omega$ , See Note 2	15	25	25	15	25	25	ns
	NOT	B		15	25	25	15	25	25	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



SN54LS640, SN54LS645

SN74LS640, SN74LS645

## OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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### TYPICAL CHARACTERISTICS

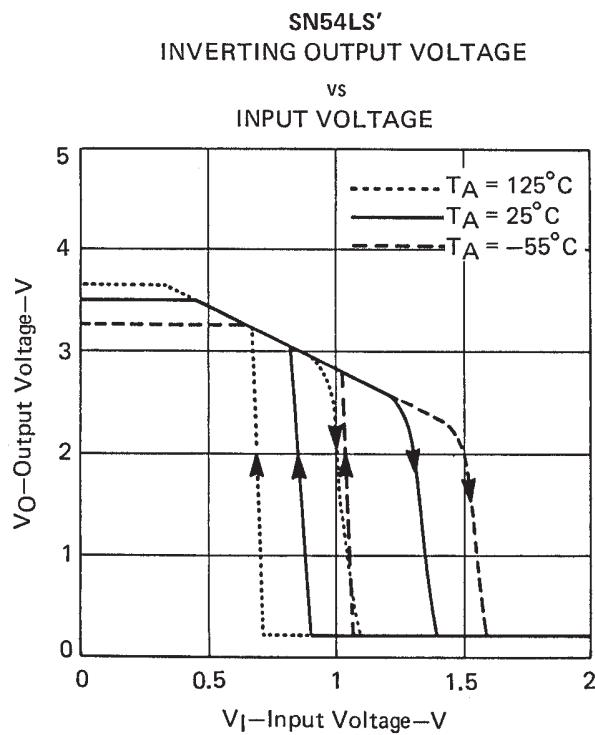


FIGURE 1

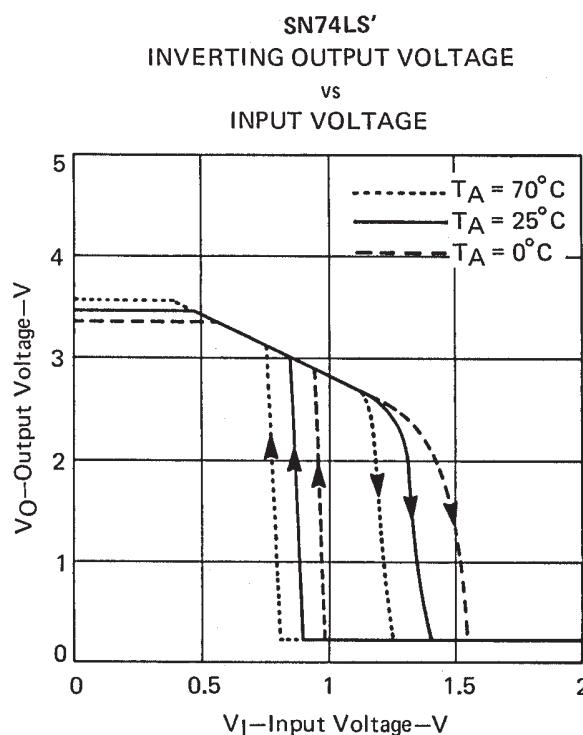


FIGURE 2

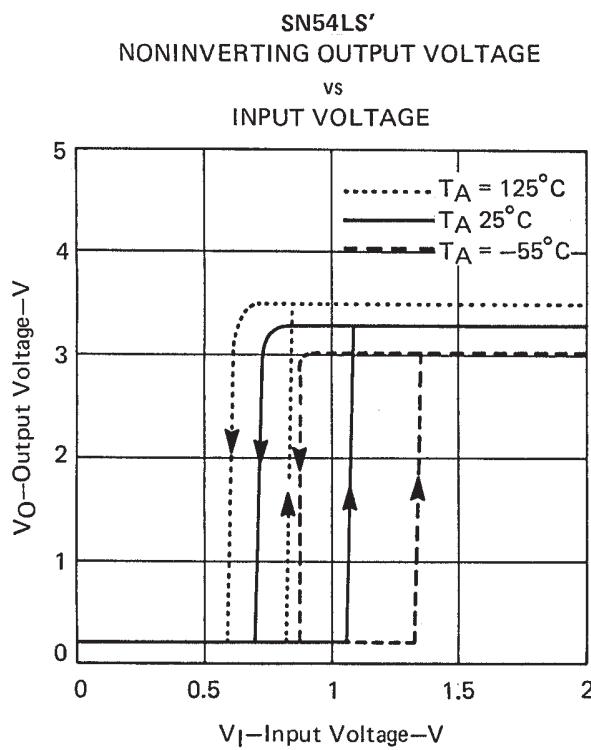


FIGURE 3

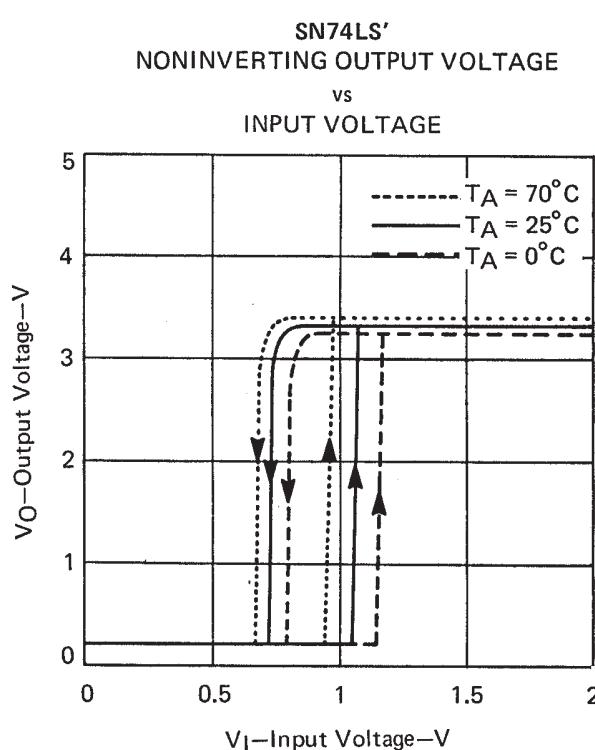


FIGURE 4

**SN54LS641, SN54LS642, SN54LS644  
SN74LS641, SN74LS642, SN74LS644  
OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage: All inputs and I/O ports .....	7 V
Operating free-air temperature range: SN54LS641, SN54LS642, SN54LS644 .....	- 55°C to 125°C
SN74LS641, SN74LS642, SN74LS644 .....	0°C to 70°C
Storage temperature range .....	- 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

**recommended operating conditions**

PARAMETER	SN54LS641			SN74LS641			UNIT	
	SN54LS642			SN74LS642				
	MIN	NOM	MAX	MIN	NOM	MAX		
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	V	
$V_{IH}$ High-level input voltage	2			2			V	
$V_{IL}$ Low-level input voltage			0.5			0.6	V	
$V_{OH}$ High-level output voltage			5.5			5.5	V	
$I_{OL}$ Low-level output current			12			24	mA	
						48§		
$T_A$ Operating free-air temperature	- 55		125	0		70	°C	

§ The 48 mA limit applies for the SN74LS641-1, SN74LS642-1, and SN74LS644-1 only.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	SN54LS641			SN74LS641			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}$ , $I_I = - 18 \text{ mA}$			- 1.5			- 1.5	V
Hysteresis ( $V_{T+} - V_{T-}$ )	$V_{CC} = \text{MIN}$ , A or B input	0.1	0.4		0.2	0.4		V
$I_{OH}$	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = \text{MAX}$ , $V_{OH} = 5.5 \text{ V}$			0.1			0.1	mA
$V_{OL}$	$V_{CC} = \text{MIN}$ , $I_{OL} = 12 \text{ mA}$ $V_{IH} = 2 \text{ V}$ , $V_{IL} = \text{MAX}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 48 \text{ mA}§$	0.25	0.4		0.25	0.4		V
$I_I$	$V_{CC} = \text{MAX}$ , A or B DIR or $\overline{G}$	0.1			0.35	0.5		
$I_{IH}$		0.1			0.4	0.5		
$I_{IL}$	$V_{CC} = \text{MAX}$ , $V_I = 2.7 \text{ V}$	20			20			$\mu\text{A}$
$I_{IC}$	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$	- 0.4			- 0.4			mA
$I_{CC}$	Outputs high			48	70		48	70
	Outputs low			62	90		62	90
	Outputs at Hi-Z			64	95		64	95

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ The 48 mA condition applies for the SN74LS641-1, SN74LS642-1, and SN74LS644-1 only.

SN54LS641, SN54LS642, SN54LS644  
 SN74LS641, SN74LS642, SN74LS644  
**OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS**

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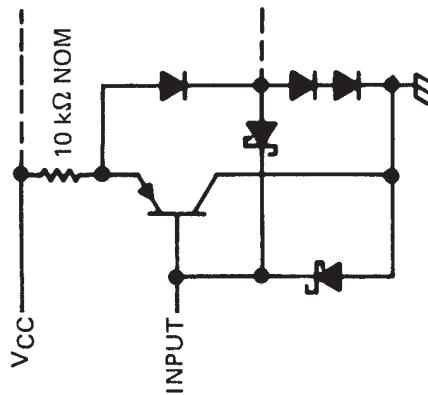
switching characteristics at  $V_{CC} = 5\text{ V}$ ,  $TA = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS			'LS641, 'LS641-1			'LS642, 'LS642-1			'LS644, 'LS644-1			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH}$ low-to-high-level output	A	B				17	25		19	25		17	25		ns
$t_{PLH}$ high-to-low-level output	B	A				17	25		19	25		19	25		ns
$t_{PHL}$ propagation delay time,	A	B	$C_L = 45\text{ pF}$ ,			16	25		14	25		14	25		ns
$t_{PHL}$ from low level	B	A				16	25		14	25		16	25		ns
$t_{PLH}$ output disable time	$\bar{G}, \text{DIR}$	A	$R_L = 667\text{ }\Omega$ ,			23	40		26	40		26	40		ns
$t_{PLH}$ from high level	$\bar{G}, \text{DIR}$	B				25	40		28	40		25	40		ns
Output enable time	$\bar{G}, \text{DIR}$	A				34	50		43	60		43	60		ns
$t_{PHL}$ from high level	$\bar{G}, \text{DIR}$	B				37	50		39	60		37	50		ns

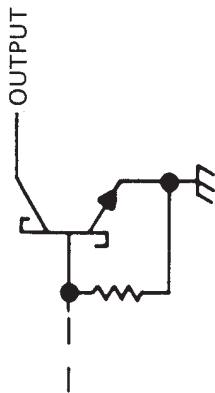
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF OUTPUTS



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
84161012A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84161012A SNJ54LS 640FK
8416101RA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8416101RA SNJ54LS640J
SN54LS640J	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS640J
SN54LS640J.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS640J
SN54LS645J	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS645J
SN54LS645J.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS645J
SN74LS640-1DW	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	0 to 70	LS640-1
SN74LS640-1N	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS640-1N
SN74LS640-1N.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS640-1N
SN74LS640-1NSR	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS640-1
SN74LS640-1NSR.A	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS640-1
SN74LS640DW	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	0 to 70	LS640
SN74LS640DWR	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS640
SN74LS640DWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS640
SN74LS640DWR.B	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS640
SN74LS640N	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS640N
SN74LS640N.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS640N
SN74LS640NSR	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS640
SN74LS640NSR.A	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS640
SN74LS641-1DW	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	0 to 70	LS641-1
SN74LS641-1DWR	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS641-1
SN74LS641-1DWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS641-1
SN74LS641-1N	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS641-1N
SN74LS641-1N.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS641-1N
SN74LS641DW	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	0 to 70	LS641
SN74LS641N	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS641N
SN74LS641N.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS641N

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74LS641NSR</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS641
<a href="#">SN74LS641NSR.A</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS641
<a href="#">SN74LS642-1DW</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS642-1
<a href="#">SN74LS642-1DW.A</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS642-1
<a href="#">SN74LS642-1N</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS642-1N
<a href="#">SN74LS642-1N.A</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS642-1N
<a href="#">SN74LS642DW</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS642
<a href="#">SN74LS642DW.A</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS642
<a href="#">SN74LS642N</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS642N
<a href="#">SN74LS642N.A</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS642N
<a href="#">SN74LS642NSR</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS642
<a href="#">SN74LS642NSR.A</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS642
<a href="#">SN74LS645-1DW</a>	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	0 to 70	LS645-1
<a href="#">SN74LS645-1DWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS645-1
<a href="#">SN74LS645-1DWR.A</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS645-1
<a href="#">SN74LS645-1N</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS645-1N
<a href="#">SN74LS645-1N.A</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS645-1N
<a href="#">SN74LS645-1NSR</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS645-1
<a href="#">SN74LS645-1NSR.A</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS645-1
<a href="#">SN74LS645DW</a>	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	0 to 70	LS645
<a href="#">SN74LS645N</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS645N
<a href="#">SN74LS645N.A</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS645N
<a href="#">SN74LS645NSR</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS645
<a href="#">SN74LS645NSR.A</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS645
<a href="#">SNJ54LS640FK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84161012A SNJ54LS 640FK
<a href="#">SNJ54LS640FK.A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84161012A SNJ54LS 640FK
<a href="#">SNJ54LS640J</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8416101RA SNJ54LS640J

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54LS640J.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8416101RA SNJ54LS640J
<b>SNJ54LS645J</b>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS645J
SNJ54LS645J.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS645J

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF SN54LS640, SN54LS645, SN74LS640, SN74LS645 :

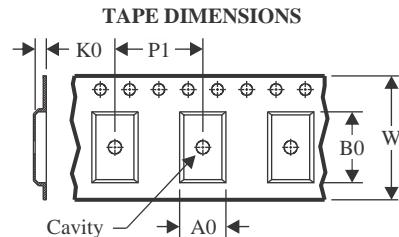
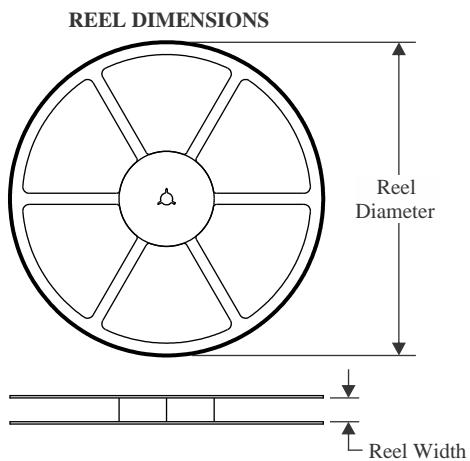
- Catalog : [SN74LS640](#), [SN74LS645](#)

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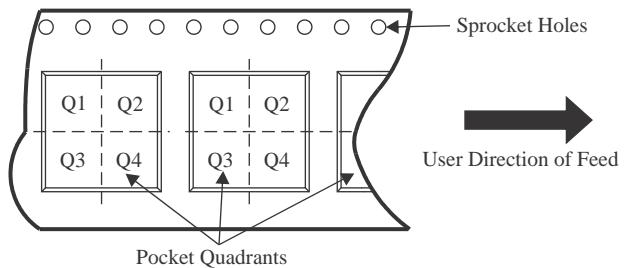
- Military : [SN54LS640](#), [SN54LS645](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


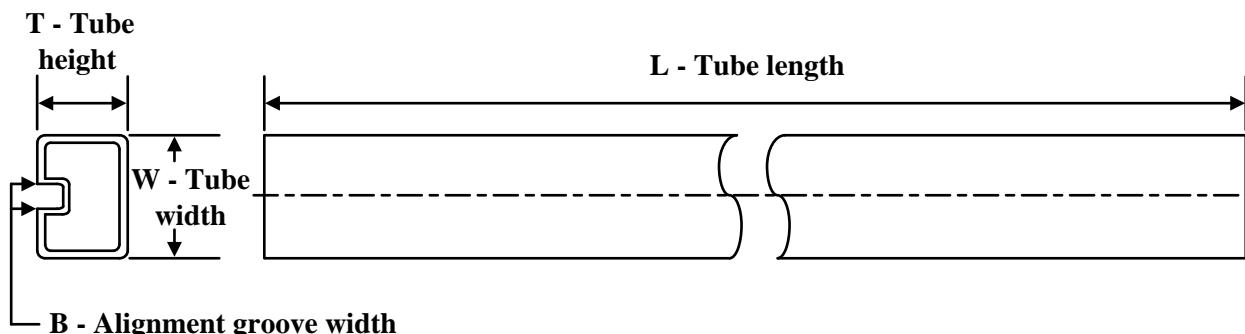
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS640-1NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LS640DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS640NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LS641-1DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS641NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LS642NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LS645-1DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS645-1NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LS645NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS640-1NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LS640DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LS640NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LS641-1DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LS641NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LS642NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LS645-1DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LS645-1NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LS645NSR	SOP	NS	20	2000	356.0	356.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
84161012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74LS640-1N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS640-1N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS640N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS640N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS641-1N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS641-1N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS641N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS641N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS642-1DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS642-1DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS642-1N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS642-1N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS642DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS642DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS642N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS642N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS645-1N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS645-1N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS645N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS645N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54LS640FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS640FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



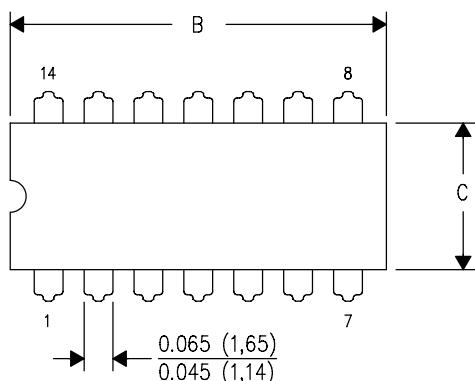
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

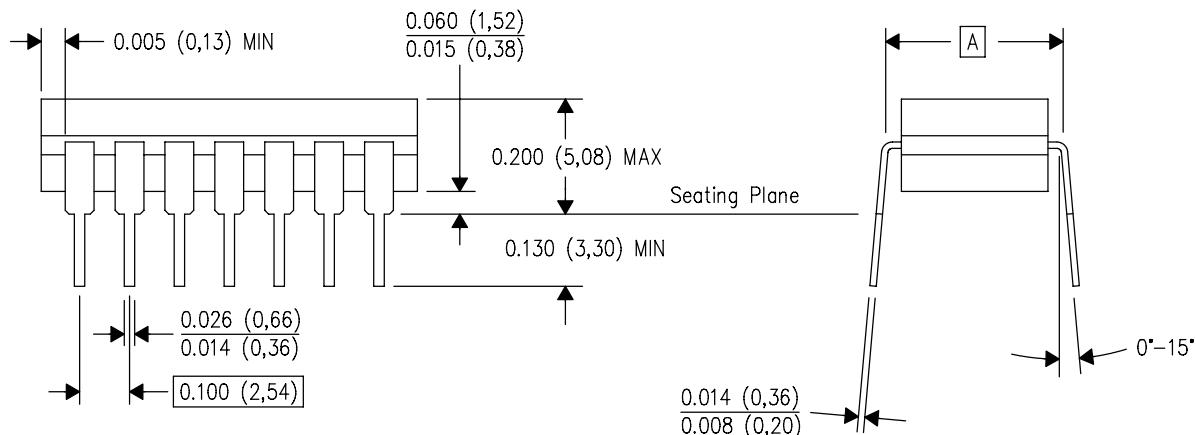
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# GENERIC PACKAGE VIEW

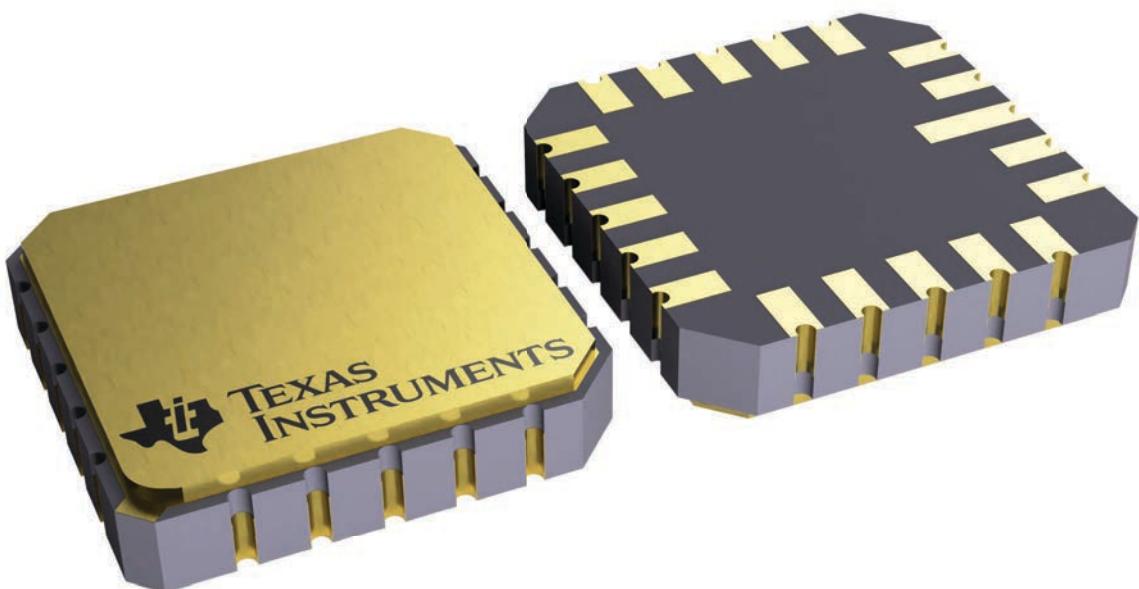
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



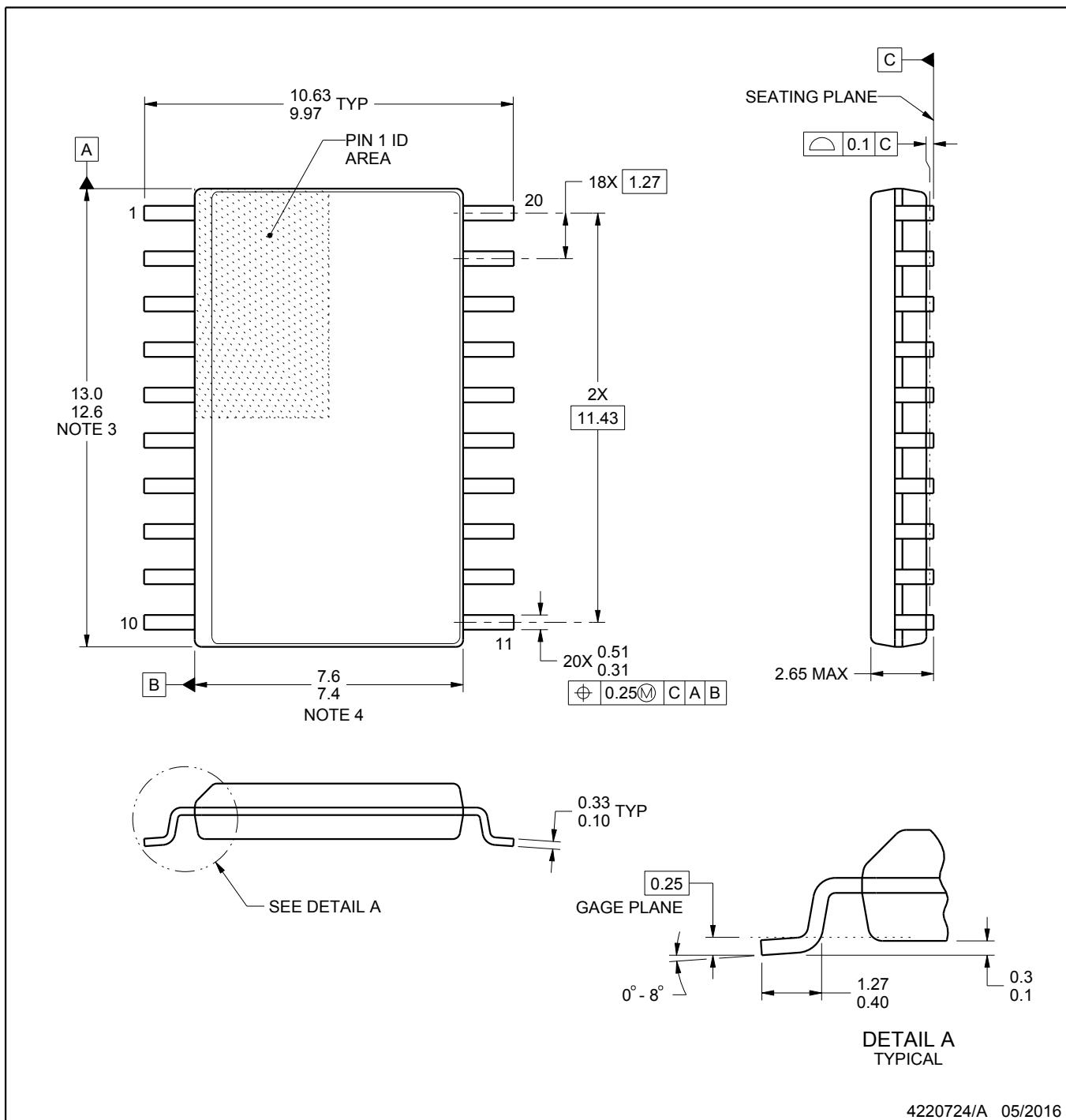
# PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



## NOTES:

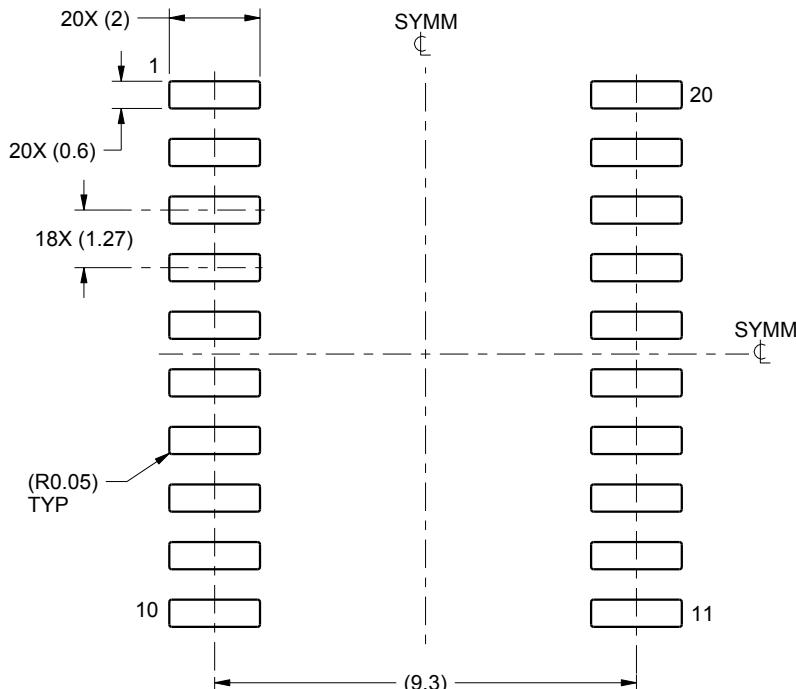
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

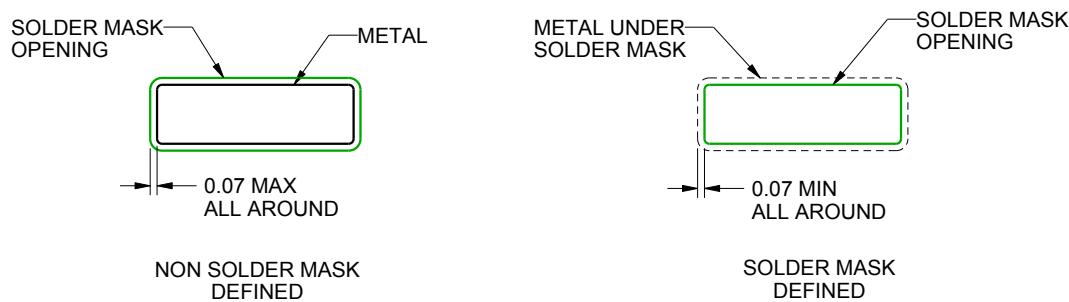
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

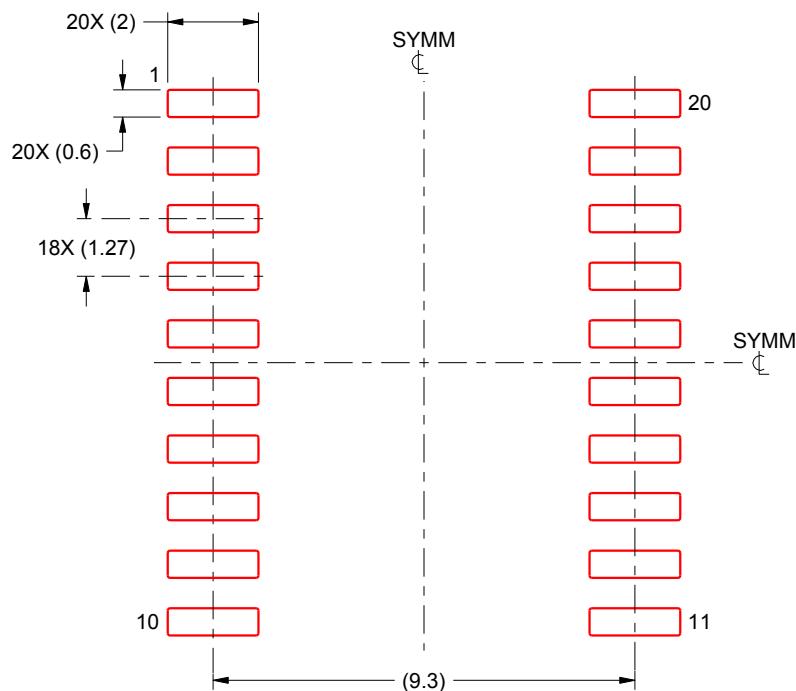
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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