RFD14N05L, RFD14N05LSM, RFP14N05L

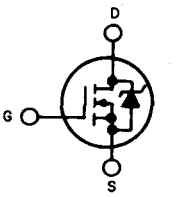
File Number **2246**

N-Channel Logic-Level Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

14 A, 50 V
$r_{DS}(on)$: 0.1 Ω

Features
- *Design optimized for 5-volt gate drive*
- *Can be driven directly from QMOS, NMOS, TTL circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



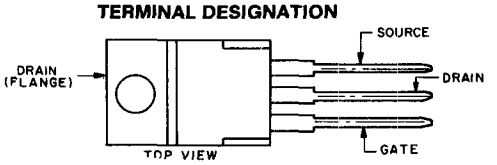
92CS-42658

TERMINAL DIAGRAM

The RFD14N05L, RFD14N05LSM, and RFP14N05L n-channel logic-level power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use with logic-level (5 volt) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor-relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate-oxide design which provides fully rated conductance at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

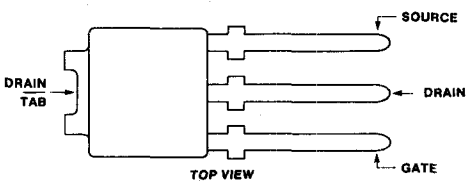
The RFD14N05L is supplied in the JEDEC TO-251 plastic package and the RFD14N05LSM is supplied in the JEDEC TO-252 surface-mount plastic package. The RFP14N05L is supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION

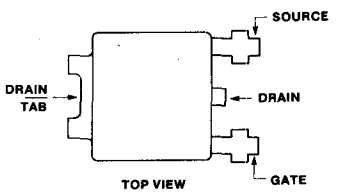


JEDEC TO-220AB

TERMINAL DESIGNATION



JEDEC TO-251AA



JEDEC TO-252AA

92CS-43478

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C=25°C):

DRAIN-SOURCE VOLTAGE, V_{DSS}	50 V
DRAIN-GATE VOLTAGE, R_{GS}=1 MΩ, V_{DGR}	50 V
GATE-SOURCE VOLTAGE, V_{GS}	±10 V
DRAIN CURRENT:	
RMS Continuous, I_D	14 A
Pulsed, I_{DM}	35 A
SINGLE PULSE AVALANCHE ENERGY RATING, E_{AS}	100 mj
AVALANCHE CURRENT, I_{AS}	14 A
POWER DISSIPATION, P_T:	
At T_C=25°C	40 W
Derate above T_C=25°C	0.32 W/°C
OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	-55 to +150°C

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C) = 25° C Unless Otherwise Specified.

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V		50	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA		1	2	
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V		—	1	μA
		T_C = 150° C		—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V		—	100	nA
Static Drain-Source On-Resistance	$r_{DS}(on)$	I_D = 14 A, V_{GS} = 5 V		—	0.1	Ω
		I_D = 14 A, V_{GS} = 4 V		—	0.12	
Turn-On Time	t(on)	V_{DD} = 25 V, I_D = 7 A		—	60	ns
Turn-On Delay Time	$t_d(on)$	I_{g1} = I_{g2} = 0.4 A		—	13 (typ.)	
Rise Time	t_r	V_{GS}(clamp) +5 V, -0.6 V		—	24 (typ.)	
Turn-Off Delay Time	$t_d(off)$	R_L = 3.57 Ω		—	42 (typ.)	
Fall Time	t_f	(See Figs. 10 & 11)		—	16 (typ.)	
Turn-Off Time	t(off)			—	100	
Total Gate Charge	Q_g(total)	V_{DD} = 40 V	V_{GS} = 0-10 V	—	40	nC
Gate Charge at 5 V	$Q_g(5)$	I_D = 14 A	V_{GS} = 0-5 V	—	25	
Threshold Gate Charge	$Q_g(th)$	R_L = 2.86 Ω	V_{GS} = 0-1 V	—	1.5	
Plateau Voltage	V(plateau)	I_D = 14 A, V_{DS} = 15 V		—	4	V
Turn-Off Energy Loss Per Cycle	E_{off}	V_{DD} = 25 V, I_D = 7 A, L = 0.2 μH, R_L = 3.57 Ω, I_{g1} = I_{g2} = 0.2 A, V_{GS}(clamp) +5 V, -0.6 V		—	14	μJ
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			—	3.125	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	TO-251 & TO-252		—	100	
		TO-220		—	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 14 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 14 A, dI_F/d_t = 100 A/μs	—	125	ns

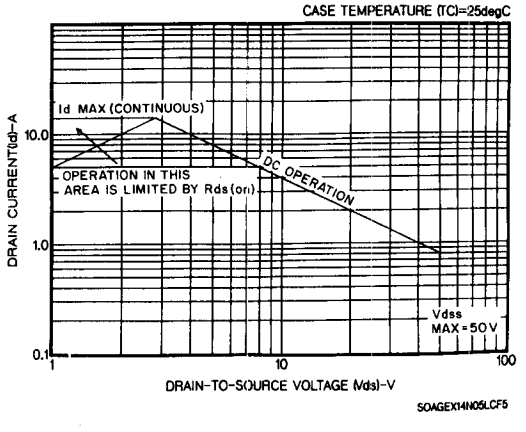


Fig. 1 - Safe-operating-area curve. (Curves must be derated linearly with increase in case temperature.)

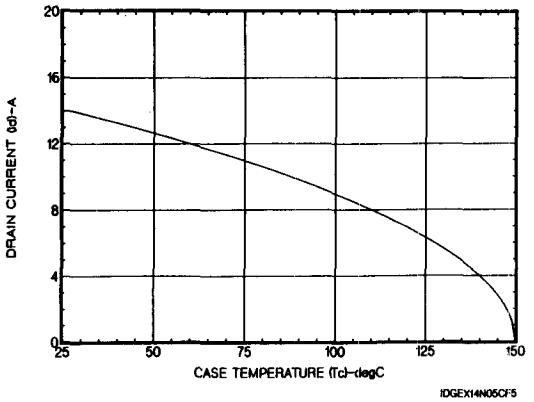


Fig. 2 - Maximum continuous drain current vs. temperature.

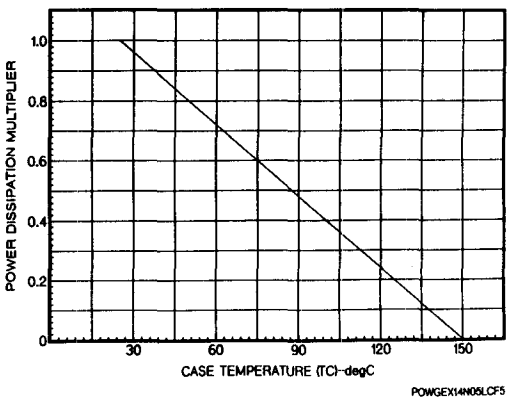


Fig. 3 - Normalized power dissipation vs. temperature derating curve.

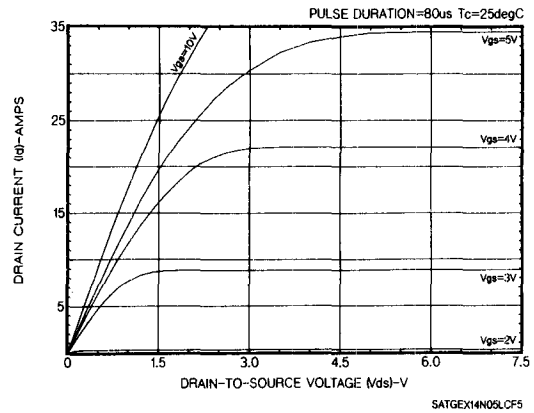


Fig. 4 - Typical saturation characteristics.

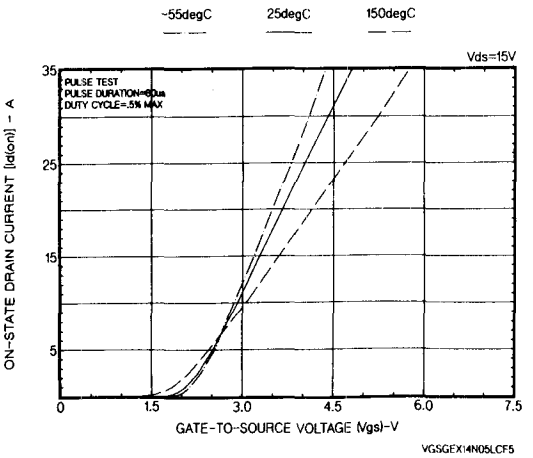


Fig. 5 - Typical transfer characteristics.

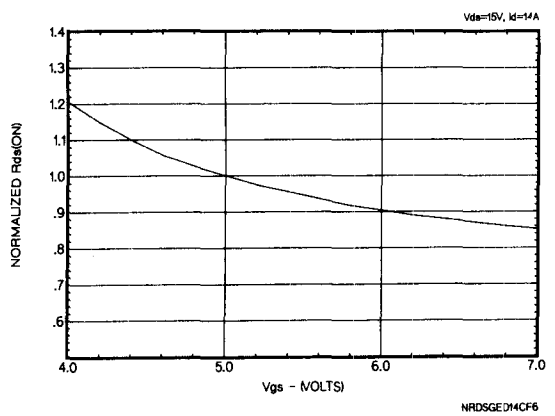


Fig. 6 - Normalized $r_{DS}(on)$ vs. V_{gs}.

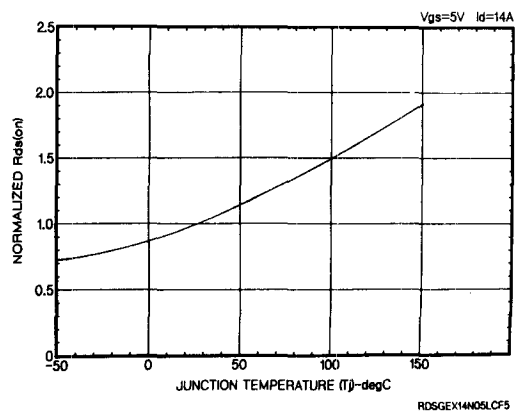


Fig. 7 - Normalized $r_{DS}(on)$ vs. junction temperature.

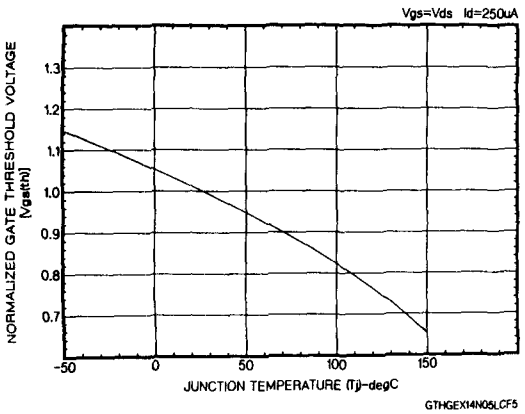


Fig. 8 - Gate threshold voltage vs. temperature.

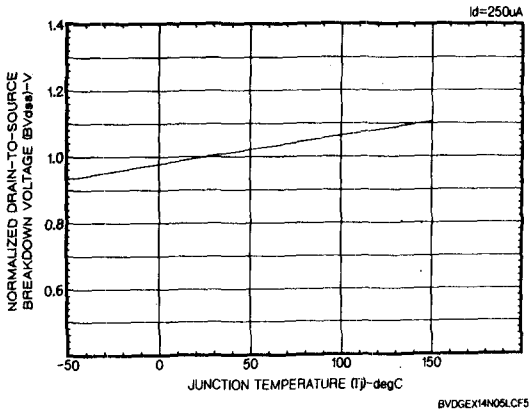


Fig. 9 - Drain source breakdown voltage vs. temperature.

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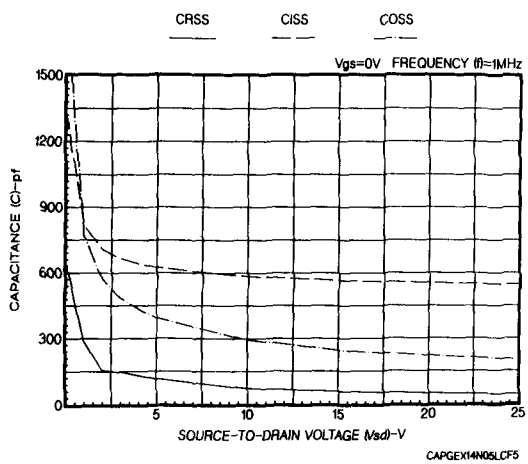

Fig. 10 - Typical capacitance vs. voltage.

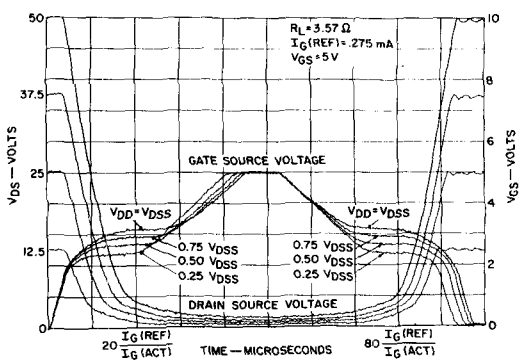

Fig. 11 - Normalized switching waveforms for constant gate current. (Refer to RCA application notes AN-7254 and AN7260.)

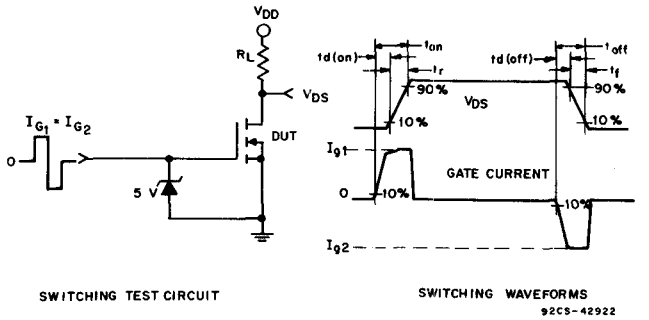

Fig. 12 - Resistive switching.

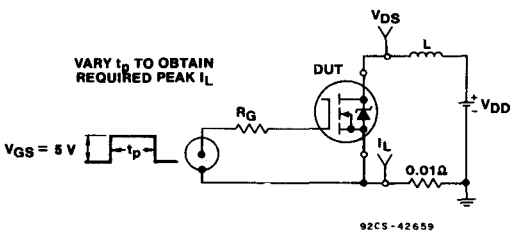

Fig. 13 - Unclamped energy test circuit.

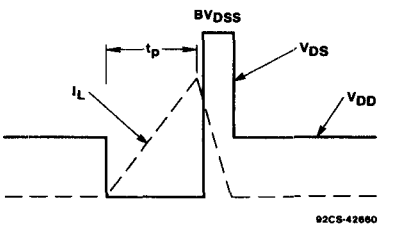

Fig. 14 - Unclamped energy waveforms.