ROHM

STRUCTURE	Silicon Monolithic Integrated Circuit
PRODUCT NAME	A serial control LED driver for car
TYPE	**BD8105FV**
FEATURES	• 12 bit serial control
	• Cascade connection support

●ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

PARAMETER	SYMBOL	LIMITS	UNIT
Power Supply Voltage	Vcc	7	V
Output Voltage	VDmax	35	V
Power Dissipation	Pd	1187*	mW
Operating Temperature Range	Topr	−40~+105	℃
Storage Temperature Range	Tstg	−55~+150	℃
Drive Current (DC)	IomaxD	50	mA
Drive Current (Pulse)	IomaxP	150**	mA
Junction Temperature	Tjmax	150	℃

* Pd decreased at 9.50mW/℃ for temperatures above Ta=25℃,mounted on 70×70×1.6mm Glass-epoxy PCB.
** Do not however exceed Pd. Time to impress≦200msec

●OPERATING CONDITION (Ta=−40~105℃)

PARAMETER	SYMBOL	LIMIT			UNIT
		Min	Typ	Max	
Power Supply Voltage	Vcc	4.5	5	5.5	V
Input Voltage	VIN	−0.3	−	Vcc	V
Drive Current	Io	−	20	40	mA

* The product described in this specification is a strategic product (and/or service) subject to COCOM regulations. It should not be exported without authorization from the appropriate government.

* This product is not designed for protection against radioactive rays.

* Status of this document
  The Japanese version of this document is the formal specification.
  A customer may use this translation version only for a reference to help reading the formal version.
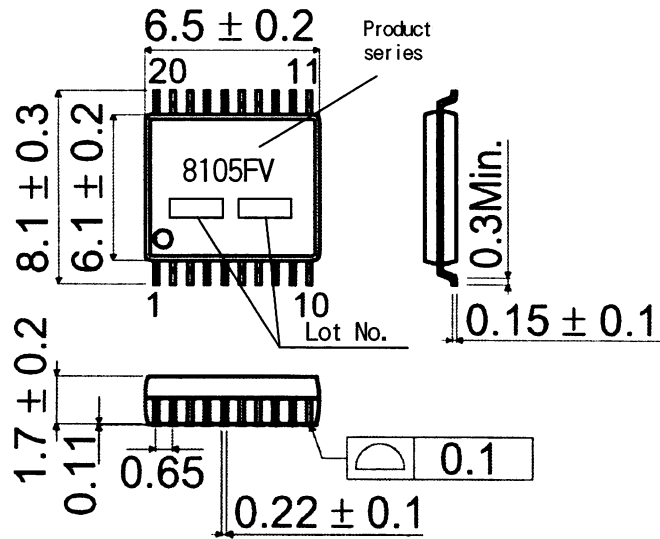 If there are any differences in translation version of this document, formal version takes priority.

●ELECTRICAL CHARACTERISTICS (Unless otherwise specified Ta=-40~105°C Vcc=4.5~5.5V)

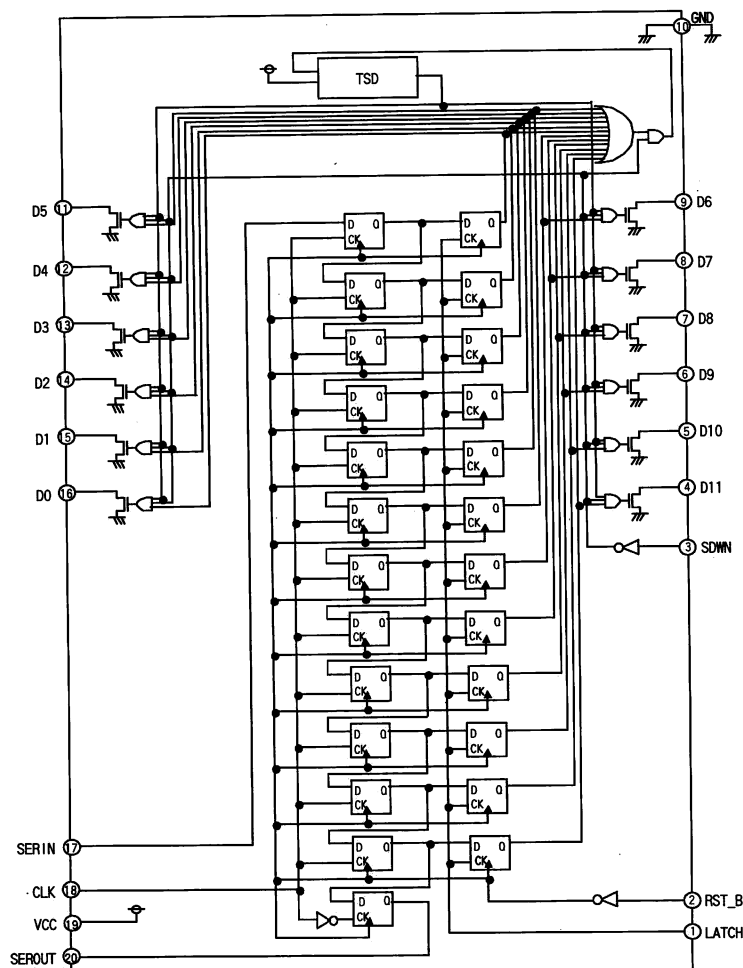| PARAMETER	SYMBOL	LIMIT			UNIT	CONDITIONS
		Min	Typ	Max		
[Output D0~D11]						
ON Resistor	RON	–	6	12	Ω	ID=20mA
Output leakage current	ILEAK	–	–	5	uA	VD=34V
[Logic input]						
Upper limit threshold voltage	VtH	Vcc ×0.8	–	–	V	
Bottom limit threshold voltage	VtL	–	–	Vcc ×0.2	V	
Serial clock frequency	fCLK	–	–	1	MHz	
Input Current	IIN	20	–	100	uA	VIN=5V
Input leakage Current	IINL	–	–	5	uA	VIN=0V
[WHOLE]						
Circuit Current	ICC1	–	–	5	mA	出力ON
Static Current	ICC2	–	–	50	uA	出力OFF
[SER OUT]						
Output Voltage high	VOH	4.6	4.8	–	V	Vcc=5V, Iso=-5mA
Output voltage Low	VOL	–	0.2	0.4	V	Vcc=5V, Iso=5mA

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●PHYSICAL DIMENSIONS・MARKING

SSOP-B20W (UNIT:mm)

● BLOCK DIAGRAM

※ Refer to the Technical Note about the details of the application.

●Pin No, Pin Name, Function

Pin No	Pin Name	Function	Pin No	Pin Name	Function
1	LATCH	Latch signal input terminal (H: Data latch)	11	D5	Drain output terminal 5
2	RST_B	Reset return input terminal (L:FF data 0)	12	D4	Drain output terminal 4
3	SDWN	Shut down input terminal (H: Output OFF)	13	D3	Drain output terminal 3
4	D11	Drain output terminal 11	14	D2	Drain output terminal 2
5	D10	Drain output terminal 10	15	D1	Drain output terminal 1
6	D9	Drain output terminal 9	16	D0	Drain output terminal 0
7	D8	Drain output terminal 8	17	SERIN	Serial data input terminal
8	D7	Drain output terminal 7	18	CLK	Clock input terminal
9	D6	Drain output terminal 6	19	VCC	Power supply voltage input terminal
10	GND	GND terminal	20	SEROUT	Serial data output terminal

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●Operation Notes

(1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

(2) Reverse connection of a power supply connector

If the connector of power is wrong connected, it may result in IC breakage. In order to prevent the breakage from the wrong connection, the diode should be connected between external power and the power terminal of IC as protection solution.

(3) GND potential

Ensure a minimum GND pin potential in all operating conditions.

(4) Setting of heat

Use a setting of heat that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(5) Pin short and mistake fitting

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage.

(6) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(7) ASO

When use this IC, please set it so that output Tr is not beyond absolute maximum rating and ASO.

(8) Thermal shutdown circuit(TSD)

This IC built-in a Thermal shutdown circuit (TSD circuit). If Chip temperature becomes 175°C(TYP.), make the output an Open state. Eventually, warmly clearing the circuit is decided by the condition of whether the heat excesses over the assigned limit, resulting the cutoff of the circuit of IC, and not by the purpose of preventing and ensuring the IC. Therefore, the warm switch-off should not be applied in the premise of continuous employing and operation after the circuit is switched on.

(9) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process

(10) IC terminal input

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.

For example, when a resistor and transistor are connected to pins. (See the chart below.)

Othe P/N junction functions as a parasitic diode when GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN).

OSimilarly, when GND > (Pin B) for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (PCB) voltage to input pins.
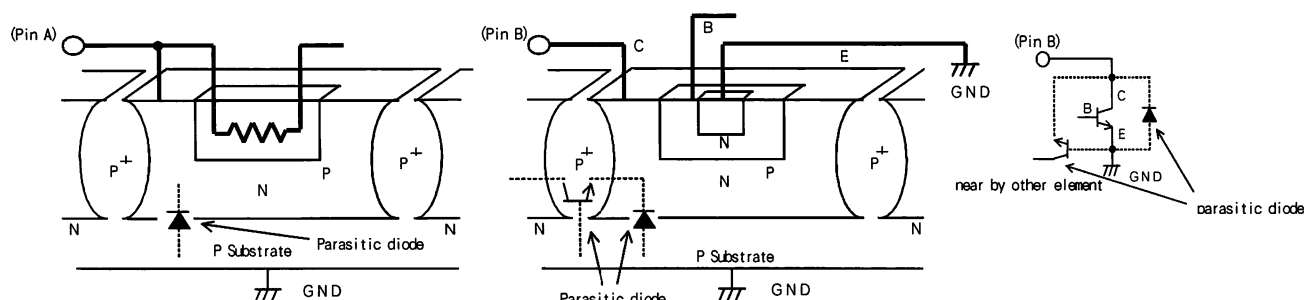

Fig of chart of Parasitic diode

(11) Ground wiring patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

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