

DATA SHEET

74ABT899

9-bit dual latch transceiver with 8-bit
parity generator/checker (3-State)

Product specification
Supersedes data of 1993 Oct 04
IC23 Data Handbook

1998 Jan 16

9-bit dual latch transceiver with 8-bit parity generator/checker (3-State)

74ABT899

FEATURES

- Symmetrical (A and B bus functions are identical)
- Selectable generate parity or "feed-through" parity for A-to-B and B-to-A directions
- Independent transparent latches for A-to-B and B-to-A directions
- Selectable ODD/EVEN parity
- Continuously checks parity of both A bus and B bus latches as \overline{ERRA} and \overline{ERRB}
- Ability to simultaneously generate and check parity
- Can simultaneously read/latch A and B bus data
- Output capability: +64 mA/−32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power up 3-State
- Power-up reset
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT899 is a 9-bit to 9-bit parity transceiver with separate transparent latches for the A bus and B bus. Either bus can generate or check parity. The parity bit can be fed-through with no change or the generated parity can be substituted with the \overline{SEL} input.

Parity error checking of the A and B bus latches is continuously provided with \overline{ERRA} and \overline{ERRB} , even with both buses in 3-State.

The 74ABT899 features independent latch enables for the A and B bus latches, a select pin for ODD/EVEN parity, and separate error signal output pins for checking parity.

FUNCTIONAL DESCRIPTION

The 74ABT899 has three principal modes of operation which are outlined below. All modes apply to both the A-to-B and B-to-A directions.

Transparent latch, Generate parity, Check A and B bus parity:

Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as \overline{BPAP} (\overline{APAP}). If \overline{LEA} and \overline{LEB} are High and the Mode Select (\overline{SEL}) is Low, the parity generated from A0-A7 and B0-B7 can be checked and monitored by \overline{ERRA} and \overline{ERRB} . (Fault detection on both input and output buses.)

Transparent latch, Feed-through parity, Check A and B bus parity:

Bus A (B) communicates to Bus B (A) in a feed-through mode if \overline{SEL} is High. Parity is still generated and checked as \overline{ERRA} and \overline{ERRB} and can be used as an interrupt to signal a data/parity bit error to the CPU.

Latched input, Generate/Feed-through parity, Check A (and B) bus parity:

Independent latch enables (\overline{LEA} and \overline{LEB}) allow other permutations of:

- Transparent latch / 1 bus latched / both buses latched
- Feed-through parity / generate parity
- Check in bus parity / check out bus parity / check in and out bus parity

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$; $GND = 0V$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	$C_L = 50\text{pF}$; $V_{CC} = 5V$	2.9	ns
t_{PLH} t_{PHL}	Propagation delay An to \overline{ERRA}	$C_L = 50\text{pF}$; $V_{CC} = 5V$	6.1	ns
C_{IN}	Input capacitance	$V_I = 0V$ or V_{CC}	4	pF
C_{IO}	Output capacitance	Outputs disabled; $V_O = 0V$ or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 5.5V$	50	μA

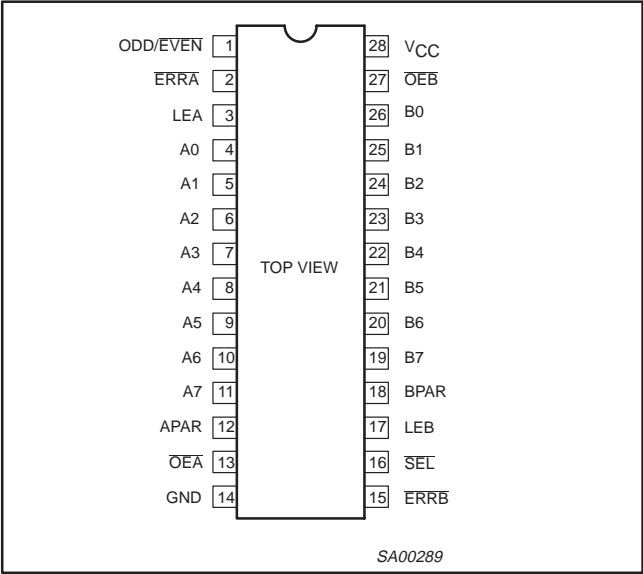
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
28-Pin Plastic PLCC	−40°C to +85°C	74ABT899 A	74ABT899 A	SOT261-3
28-Pin Plastic SOP	−40°C to +85°C	74ABT899 D	74ABT899 D	SOT136-1
28-Pin Plastic SSOP	−40°C to +85°C	74ABT899 DB	74ABT899 DB	SOT341-1

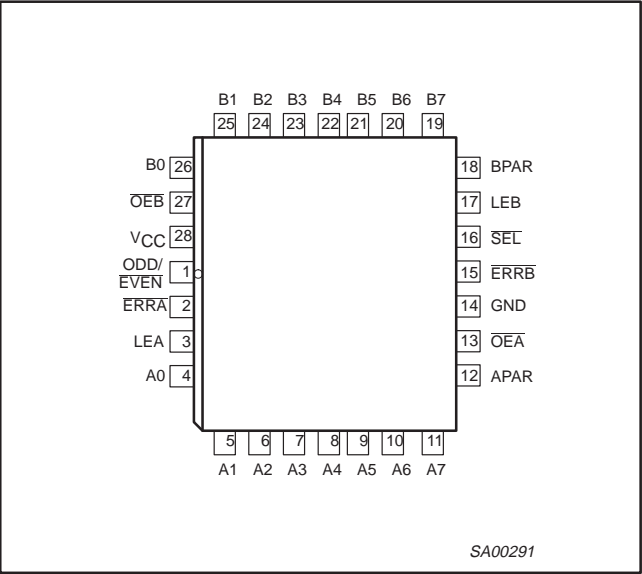
9-bit dual latch transceiver with 8-bit parity generator/checker (3-State)

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PIN CONFIGURATION



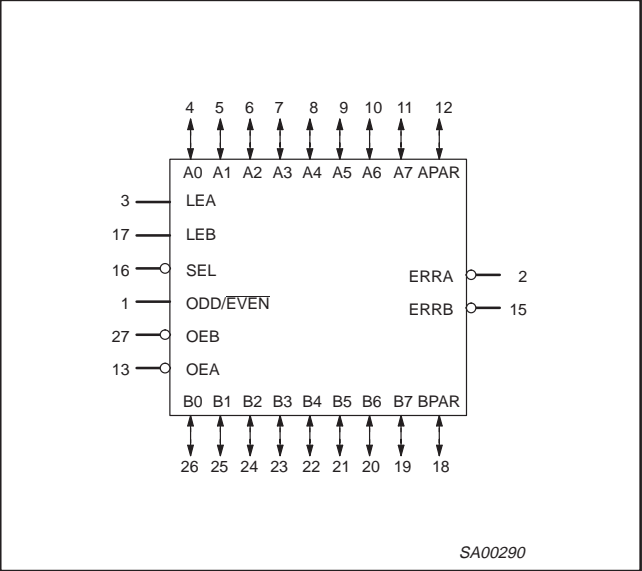
PLCC PIN CONFIGURATION



PIN DESCRIPTION

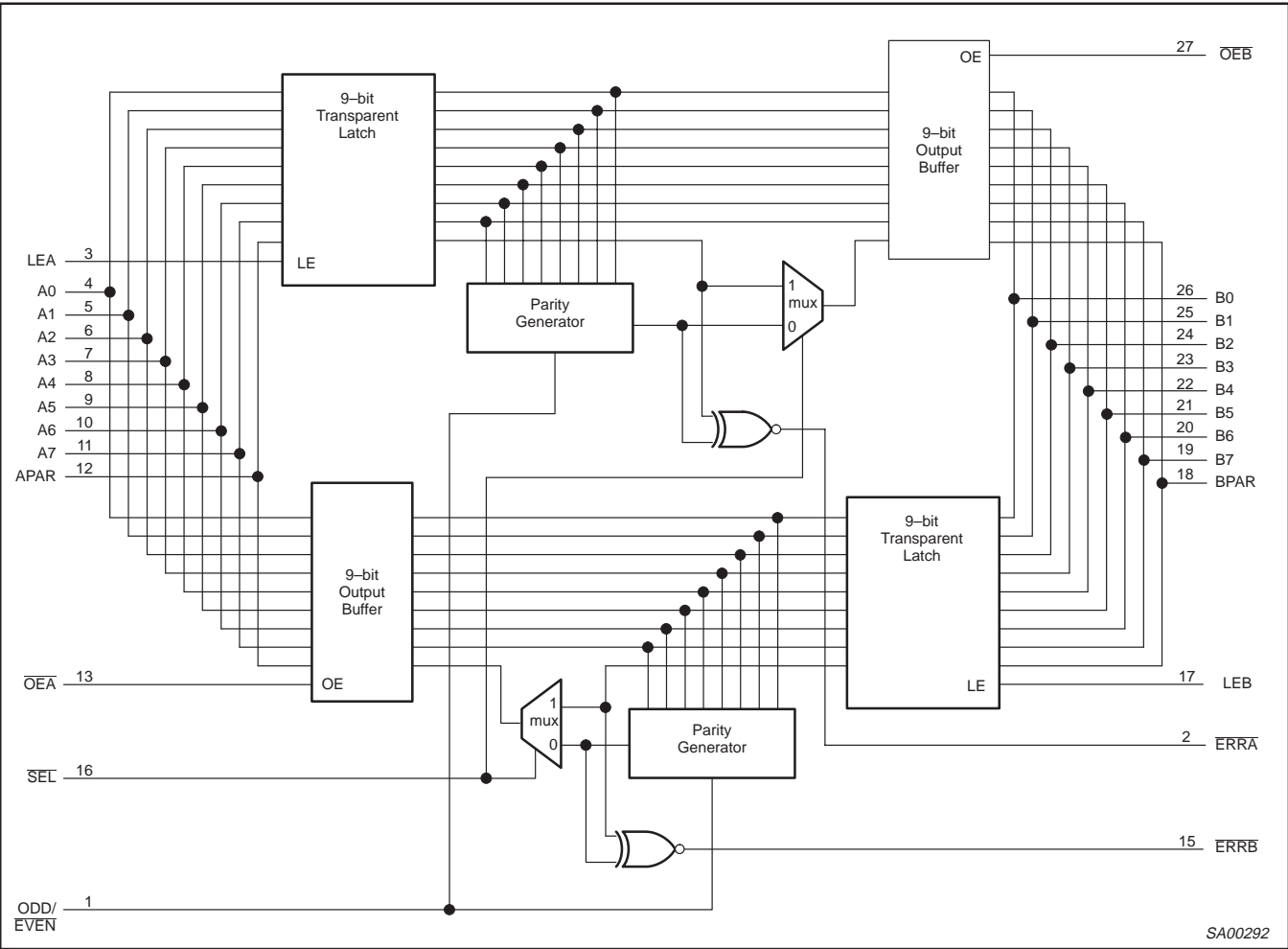
SYMBOL	PIN NUMBER	NAME AND FUNCTION
A0 - A7	4, 5, 6, 7, 8, 9, 10, 11	Latched A bus 3-State inputs/outputs
B0 - B7	19, 20, 21, 22, 23, 24, 25, 26	Latched B bus 3-State inputs/outputs
APAR	12	A bus parity 3-State input
BPAR	18	B bus parity 3-State input
ODD/EVEN	1	Parity select input (Low for EVEN parity)
OEA, OEB	13, 27	Output enable inputs (gate A to B, B to A)
SEL	16	Mode select input (Low for generate)
LEA, LEB	3, 17	Latch enable inputs (transparent High)
ERRA, ERRB	2, 15	Error signal outputs (active-Low)
GND	14	Ground (0V)
VCC	28	Positive supply voltage

LOGIC SYMBOL



9-bit dual latch transceiver with 8-bit parity generator/checker (3-State)

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FUNCTION TABLE

INPUTS					OPERATING MODE
OEB	OEA	SEL	LEA	LEB	
H	H	X	X	X	3-State A bus and B bus (input A & B simultaneously)
H	L	L	L	H	B → A, transparent B latch, generate parity from B0 - B7, check B bus parity
H	L	L	H	H	B → A, transparent A & B latch, generate parity from B0 - B7, check A & B bus parity
H	L	L	X	L	B → A, B bus latched, generate parity from latched B0 - B7 data, check B bus parity
H	L	H	X	H	B → A, transparent B latch, parity feed-through, check B bus parity
H	L	H	H	H	B → A, transparent A & B latch, parity feed-through, check A & B bus parity
L	H	L	H	X	A → B, transparent A latch, generate parity from A0 - A7, check A bus parity
L	H	L	H	H	A → B, transparent A & B latch, generate parity from A0 - A7, check A & B bus parity
L	H	L	L	X	A → B, A bus latched, generate parity from latched A0 - A7 data, check A bus parity
L	H	H	H	L	A → B, transparent A latch, parity feed-through, check A bus parity
L	H	H	H	H	A → B, transparent A & B latch, parity feed-through, check A & B bus parity
L	L	X	X	X	Output to A bus and B bus (NOT ALLOWED)

H = High voltage level
L = Low voltage level
X = Don't care

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PARITY AND ERROR FUNCTION TABLE

INPUTS				OUTPUTS			PARITY MODES	
SEL	ODD/EVEN	xPAR (A or B)	Σ of High Inputs	xPAR (B or A)	ERRt	ERRr*		
H	H	H	Even Odd	H H	H L	H L	Odd Mode	Feed-through/check parity
H	H	L	Even Odd	L L	L H	L H		
H	L	H	Even Odd	H H	L H	L H	Even Mode	
H	L	L	Even Odd	L L	H L	H L		
L	H	H	Even Odd	H L	H L	H H	Odd Mode	Generate parity
L	H	L	Even Odd	H L	L H	H H		
L	L	H	Even Odd	L H	L H	H H	Even Mode	
L	L	L	Even Odd	L H	H L	H H		

H = High voltage level

L = Low voltage level

t = Transmit—if the data path is from A→B then ERRt is ERRĀ

r = Receive—if the data path is from A→B then ERRr is ERB

* Blocked if latch is not transparent

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		−0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	−18	mA
V _I	DC input voltage ³		−1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	−50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	−0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
T _{stg}	Storage temperature range		−65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T _{amb} = +25°C			T _{amb} = −40°C to +85°C		
				Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage		V _{CC} = 4.5V; I _{IK} = −18mA		−0.9	−1.2		−1.2	V
V _{OH}	High-level output voltage		V _{CC} = 4.5V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}	2.5	3.5		2.5		V
			V _{CC} = 5.0V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}	3.0	4.0		3.0		V
			V _{CC} = 4.5V; I _{OH} = −32mA; V _I = V _{IL} or V _{IH}	2.0	2.6		2.0		V
V _{OL}	Low-level output voltage		V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	V
V _{RST}	Power-up output low voltage ³		V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V
I _I	Input leakage current	Control pins	V _{CC} = 5.5V; V _I = GND or 5.5V		±0.01	±1.0		±1.0	μA
		Data pins	V _{CC} = 5.5V; V _I = GND or 5.5V		±5	±100		±100	μA
I _{OFF}	Power-off leakage current		V _{CC} = 0.0V; V _O or V _I ≤ 4.5V		±5.0	±100		±100	μA
I _{PU} /I _{PD}	Power-up/down 3-State output current ⁴		V _{CC} = 2.1V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = Don't care		±5.0	±50		±50	μA
I _{IH} + I _{OZH}	3-State output High current		V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}		5.0	50		50	μA
I _{IL} + I _{OZL}	3-State output Low current		V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		−5.0	−50		−50	μA
I _{CEX}	Output High leakage current		V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		5.0	50		50	μA
I _O	Output current ¹		V _{CC} = 5.5V; V _O = 2.5V	−50	−80	−180	−50	−180	mA
I _{CCH}	Quiescent supply current		V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		50	250		250	μA
I _{CCL}				28	34		34	mA	
I _{CCZ}				50	250		250	μA	
ΔI _{CC}	Additional supply current per input pin ²		V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND		0.3	1.5		1.5	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From $V_{CC} = 2.1\text{V}$ to $V_{CC} = 5\text{V} \pm 10\%$, a transition time of up to 100 μsec is permitted.

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AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{\text{amb}} = +25^{\circ}\text{C}$ $V_{\text{CC}} = +5.0\text{V}$ $C_{\text{L}} = 50\text{pF}$ $R_{\text{L}} = 500\Omega$			$T_{\text{amb}} = -40 \text{ to } +85^{\circ}\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 10\%$ $C_{\text{L}} = 50\text{pF}$ $R_{\text{L}} = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	3.2 2.7	4.5 4.1	1.0 1.0	4.9 4.6	ns
t_{PLH} t_{PHL}	Propagation delay An to BPAR or Bn to APAR	2	3.0 2.5	6.0 6.4	7.5 7.9	3.0 2.5	9.0 8.8	ns
t_{PLH} t_{PHL}	Propagation delay An to $\overline{\text{ERRA}}$ or Bn to $\overline{\text{ERRB}}$	3	2.8 2.8	6.0 6.7	8.0 8.5	2.8 2.8	9.1 9.3	ns
t_{PLH} t_{PHL}	Propagation delay APAR to BPAR or BPAR to APAR	1	2.0 1.3	4.0 3.2	5.2 4.4	2.0 1.3	5.7 5.0	ns
t_{PLH} t_{PHL}	Propagation delay APAR to $\overline{\text{ERRA}}$ or BPAR to $\overline{\text{ERRB}}$	6	1.5 1.5	4.2 4.0	5.4 5.4	1.5 1.5	6.0 6.1	ns
t_{PLH} t_{PHL}	Propagation delay ODD/ $\overline{\text{EVEN}}$ to APAR or BPAR	5	2.6 2.5	5.5 5.3	6.8 6.7	2.6 2.5	8.1 7.8	ns
t_{PLH} t_{PHL}	Propagation delay ODD/ $\overline{\text{EVEN}}$ to $\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$	4	2.3 2.6	5.4 5.7	6.8 7.2	2.3 2.6	7.9 8.4	ns
t_{PLH} t_{PHL}	Propagation delay SEL to APAR or BPAR	8	1.3 1.4	4.1 4.1	5.2 5.3	1.3 1.4	6.0 5.9	ns
t_{PLH} t_{PHL}	Propagation delay SEL to $\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$	8	3.7 5.1	6.8 8.3	8.3 9.7	3.7 5.1	9.8 11.0	ns
t_{PLH} t_{PHL}	Propagation delay LEA to Bn or LEB to An	9	1.0 1.0	3.2 3.1	4.4 4.5	1.0 1.0	4.9 5.0	ns
t_{PLH} t_{PHL}	Propagation delay LEA to BPAR or LEB to APAR	9	2.0 1.7	6.8 6.3	8.3 7.9	2.0 1.7	9.7 9.0	ns
t_{PLH} t_{PHL}	Propagation delay LEA to $\overline{\text{ERRA}}$ or LEB to $\overline{\text{ERRB}}$	7	2.0 2.0	6.3 7.1	8.3 9.2	2.0 2.0	9.6 10.3	ns
t_{pZH} t_{pZL}	Output enable time $\overline{\text{OE}}\text{A}$ to An, APAR or $\overline{\text{OEB}}$ to Bn, BPAR	11, 12	1.0 1.0	3.0 3.4	4.3 4.8	1.0 1.0	5.1 5.4	ns
t_{pHZ} t_{pLZ}	Output disable time $\overline{\text{OE}}\text{A}$ to An, APAR or $\overline{\text{OEB}}$ to Bn, BPAR	11, 12	1.0 0.5	3.4 3.0	4.7 4.2	1.0 0.5	5.5 4.7	ns

AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$

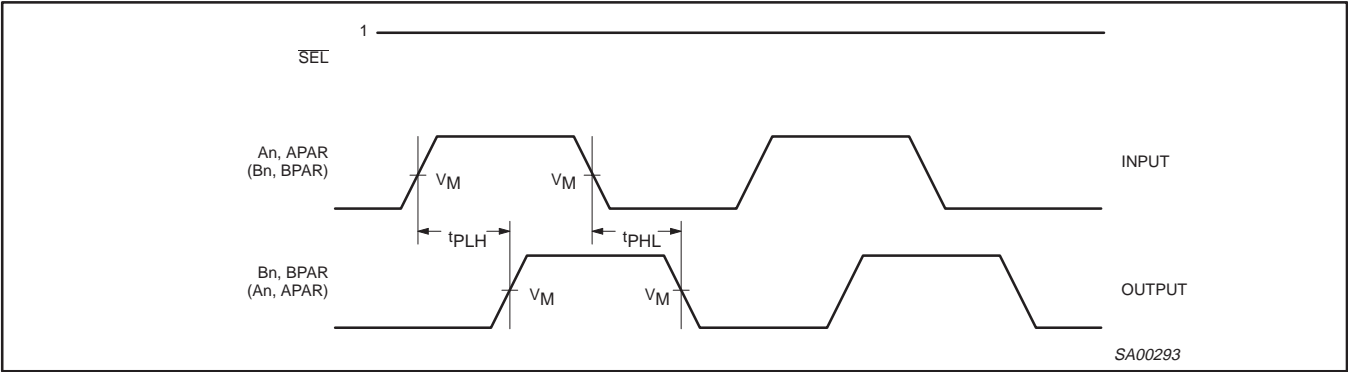
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF R _L = 500Ω			T _{amb} = −40 to +85°C V _{CC} = +5.0V ±10% C _L = 50pF R _L = 500Ω		
			Min	Typ	Max	Min	Max	
t _s (H) t _s (L)	Setup time, High or Low An, APAR to LEA or Bn, BPAR to LEB	10	2.0 1.5	0.4 0.0		2.0 1.5		ns
t _h (H) t _h (L)	Hold time, High or Low An, APAR to LEA or Bn, BPAR to LEB	10	1.5 1.0	0.0 −0.2		1.5 1.0		ns
t _w (H)	Pulse width, High LEA or LEB	10	3.0	1.9		3.0		ns

9-bit dual latch transceiver with 8-bit parity generator/checker (3-State)

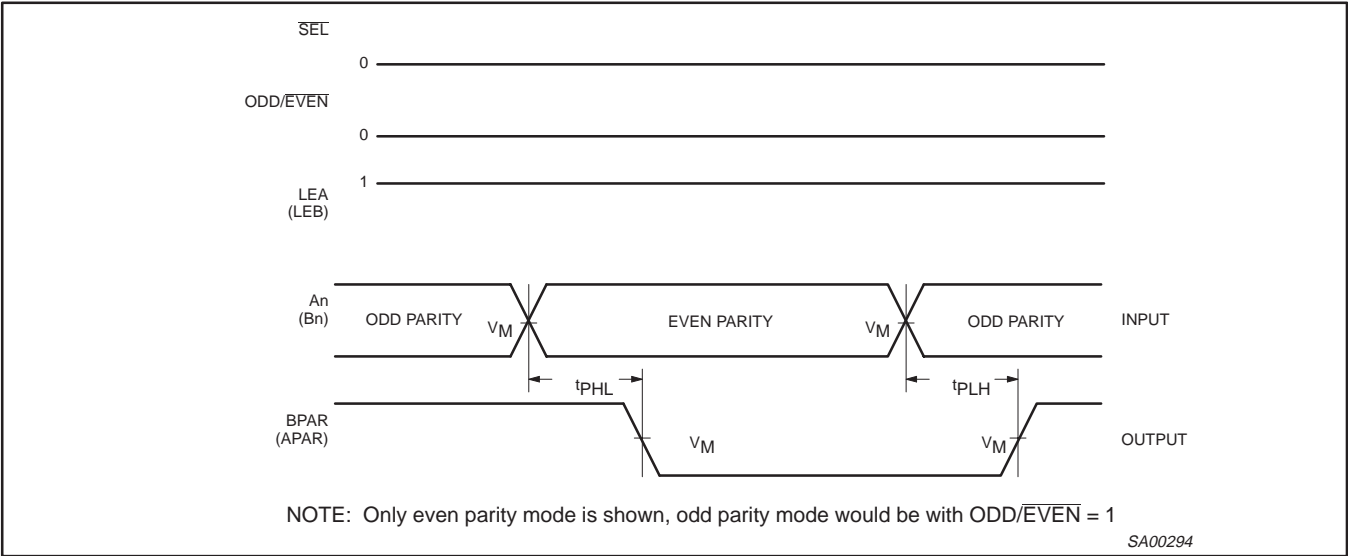
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AC WAVEFORMS

$V_M = 1.5V$, $V_{IN} = GND$ to $3.0V$

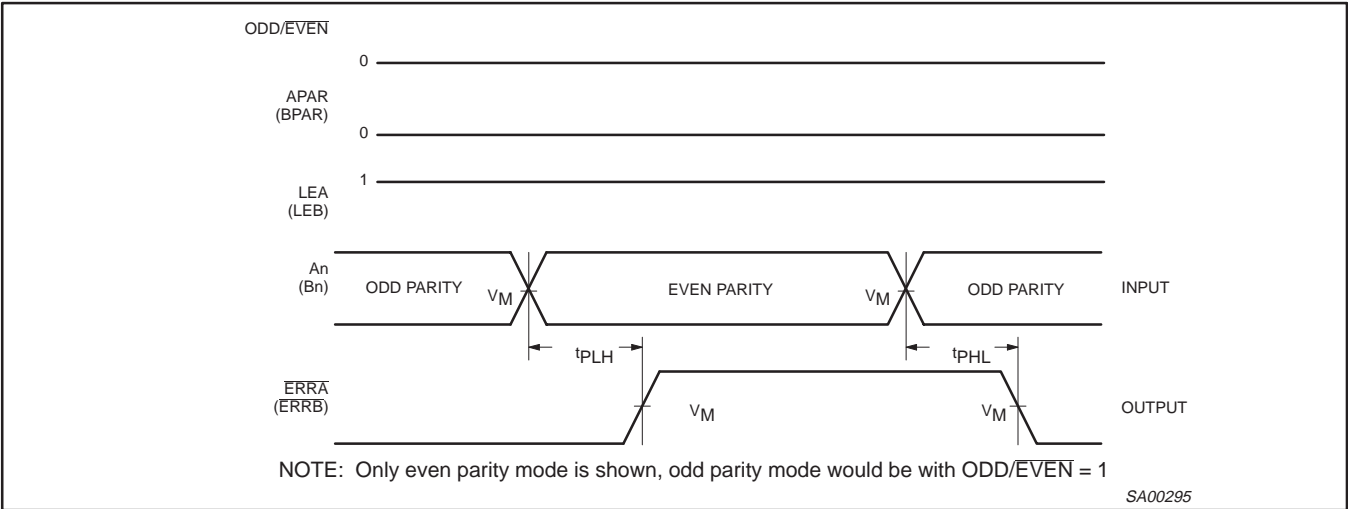


Waveform 1. Propagation Delay, An to Bn, Bn to An, APAR to BPAR, BPAR to APAR



NOTE: Only even parity mode is shown, odd parity mode would be with $ODD/\overline{EVEN} = 1$

Waveform 2. Propagation Delay, An to BPAR or Bn to APAR

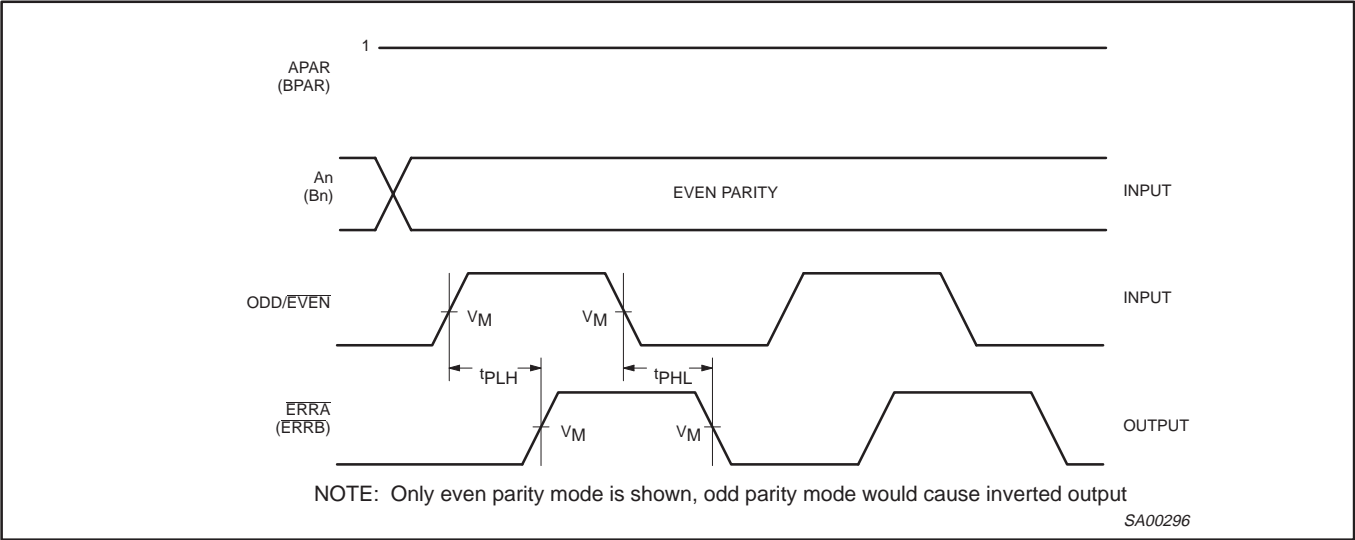


NOTE: Only even parity mode is shown, odd parity mode would be with $ODD/\overline{EVEN} = 1$

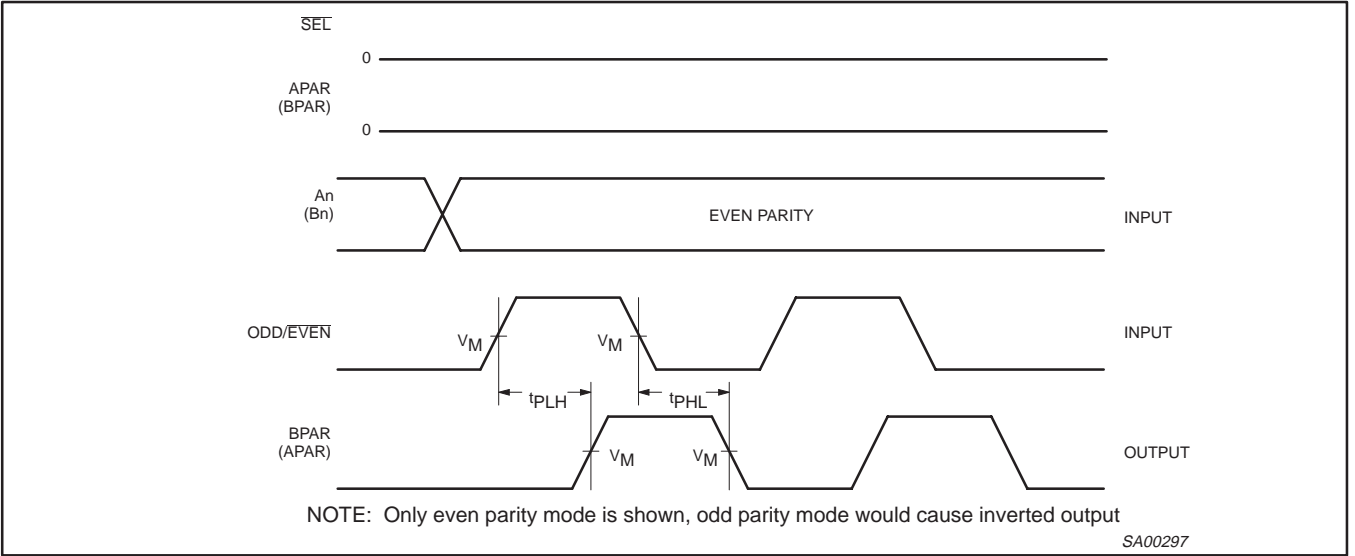
Waveform 3. Propagation Delay, An to \overline{ERRA} or Bn to \overline{ERRB}

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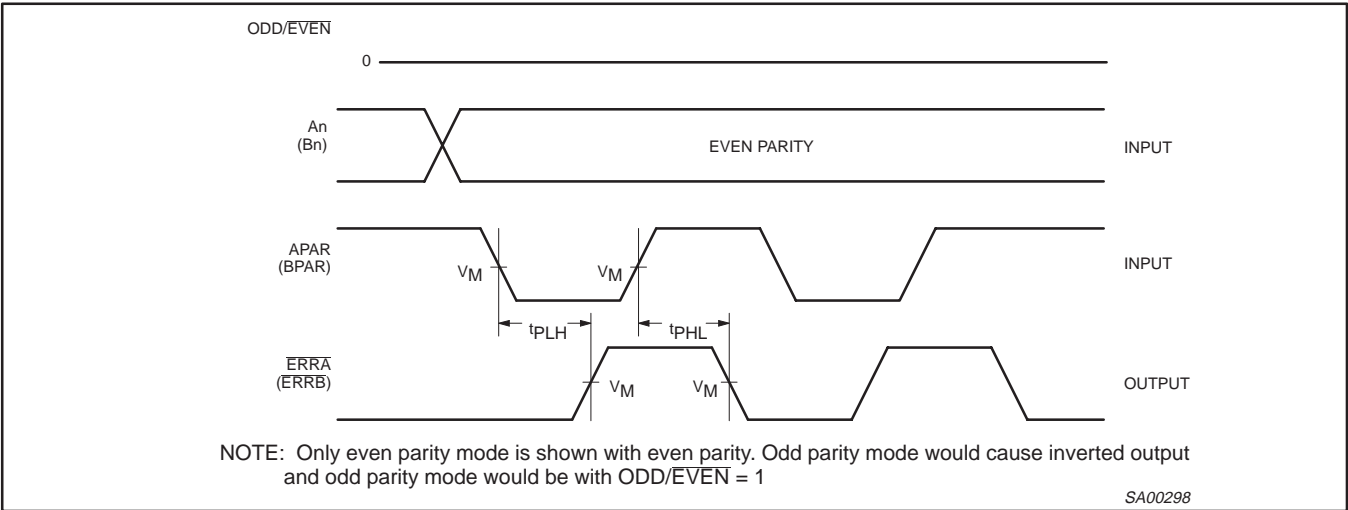
Waveform 4. Propagation Delay, ODD/EVEN to \overline{ERRA} or ODD/EVEN to \overline{ERRB}



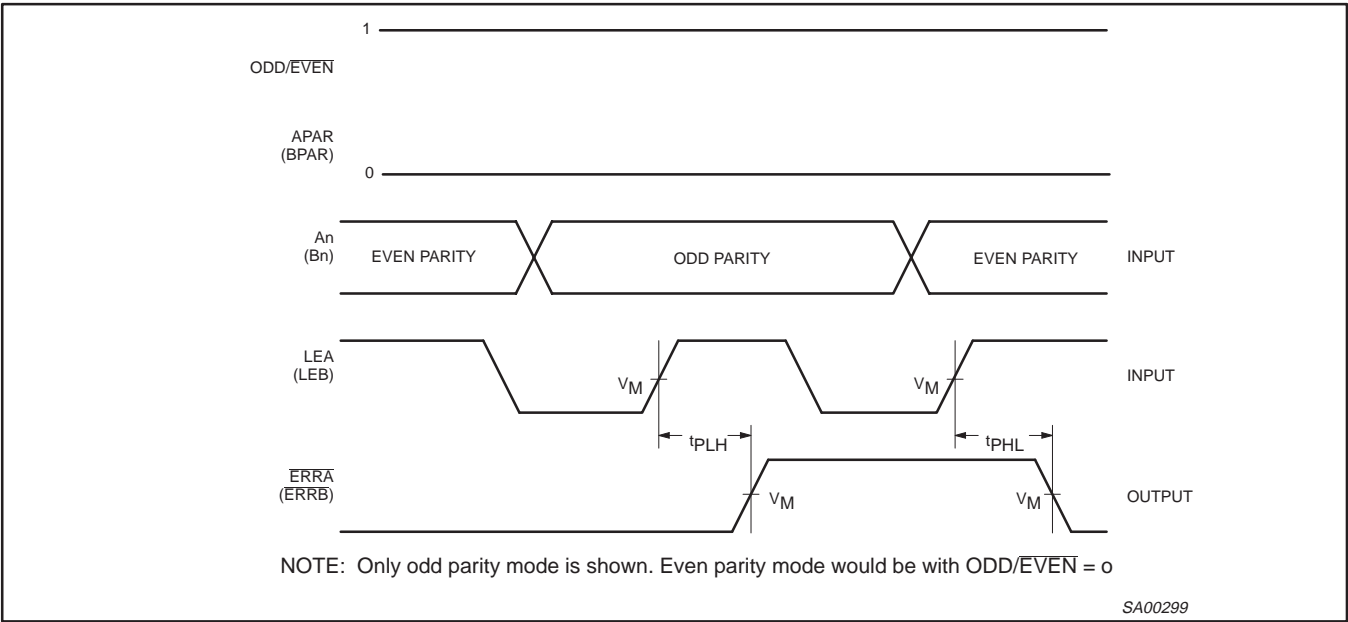
Waveform 5. Propagation Delay, ODD/EVEN to APAR or ODD/EVEN to BPAR

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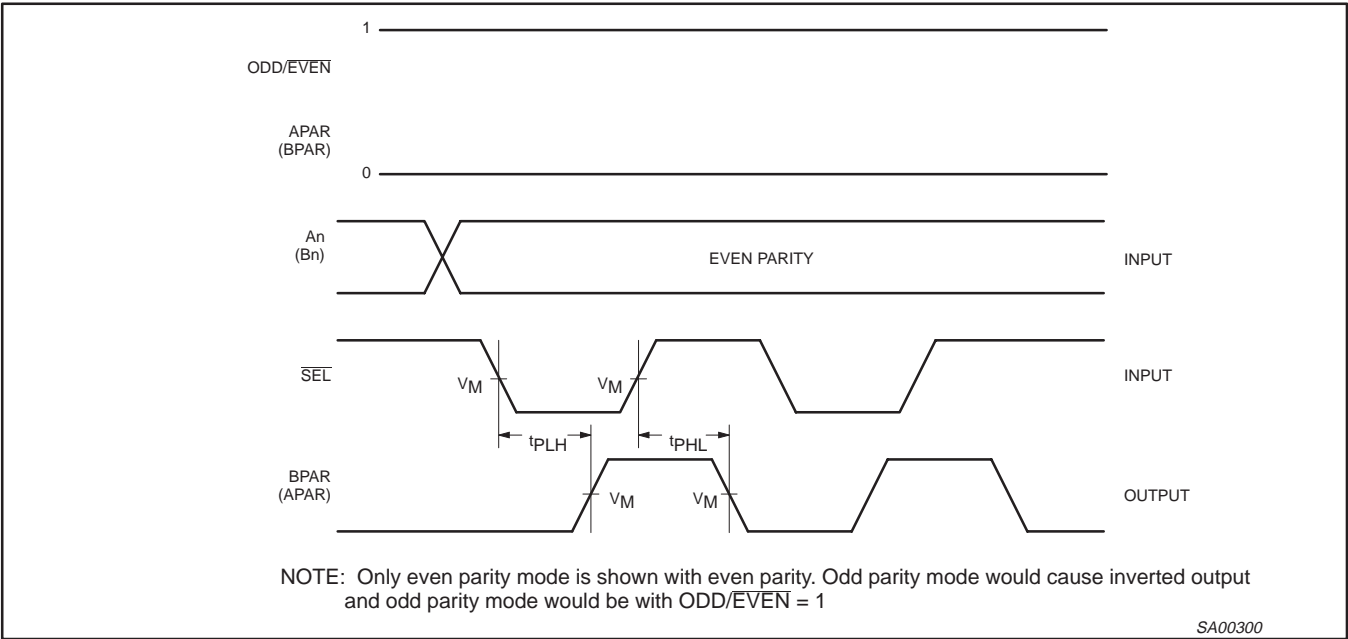
Waveform 6. Propagation Delay, APAR to $\overline{\text{ERRA}}$ or BPAR to $\overline{\text{ERRB}}$



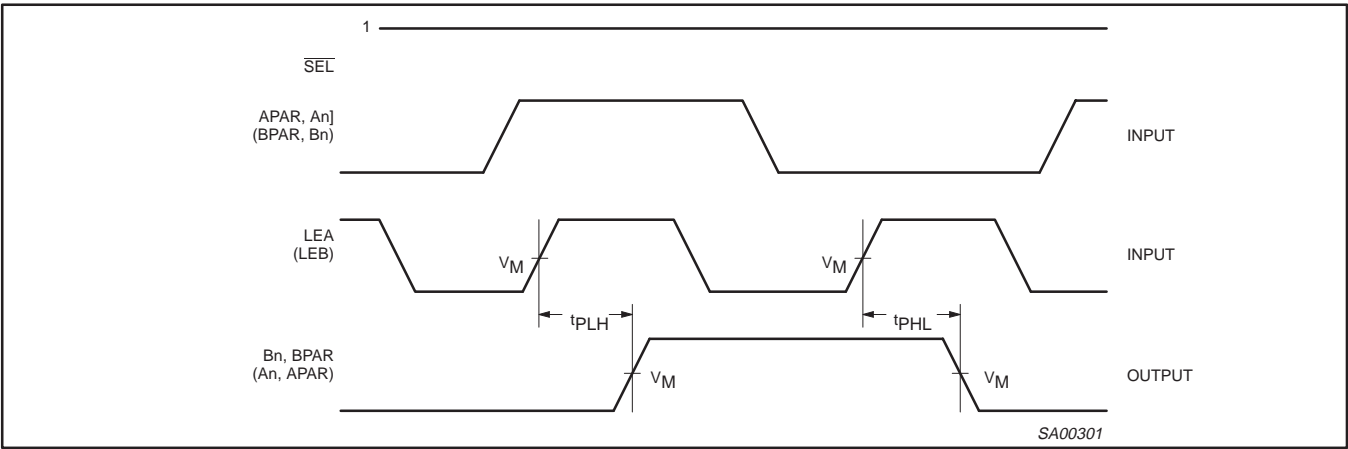
Waveform 7. Propagation Delay, LEA to $\overline{\text{ERRA}}$ or LEB to $\overline{\text{ERRB}}$

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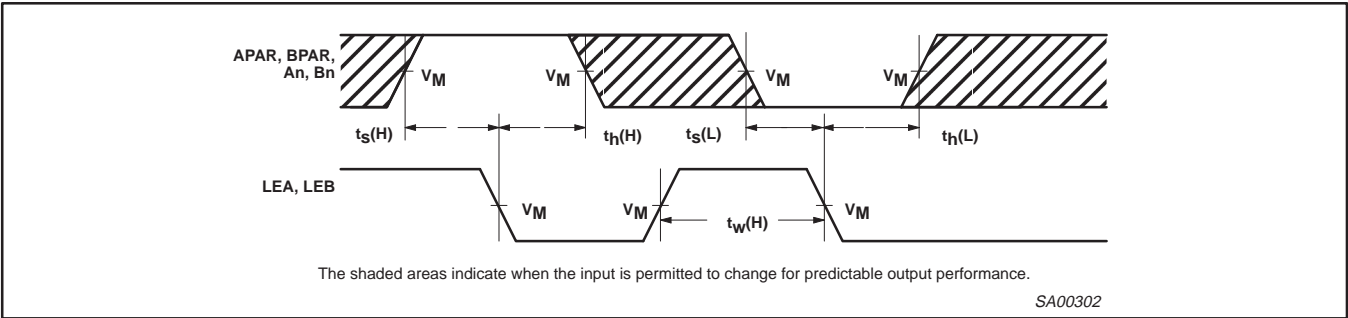
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Waveform 8. Propagation Delay, $\overline{\text{SEL}}$ to BPAR or $\overline{\text{SEL}}$ to APAR



Waveform 9. Propagation Delay, LEA to BPAR or LEB to APAR, LEA to Bn or LEB to An



Waveform 10. Data Setup and Hold Times, Pulse Width High

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Load Circuit

TEST	S1
t_{pd}	open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	open

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

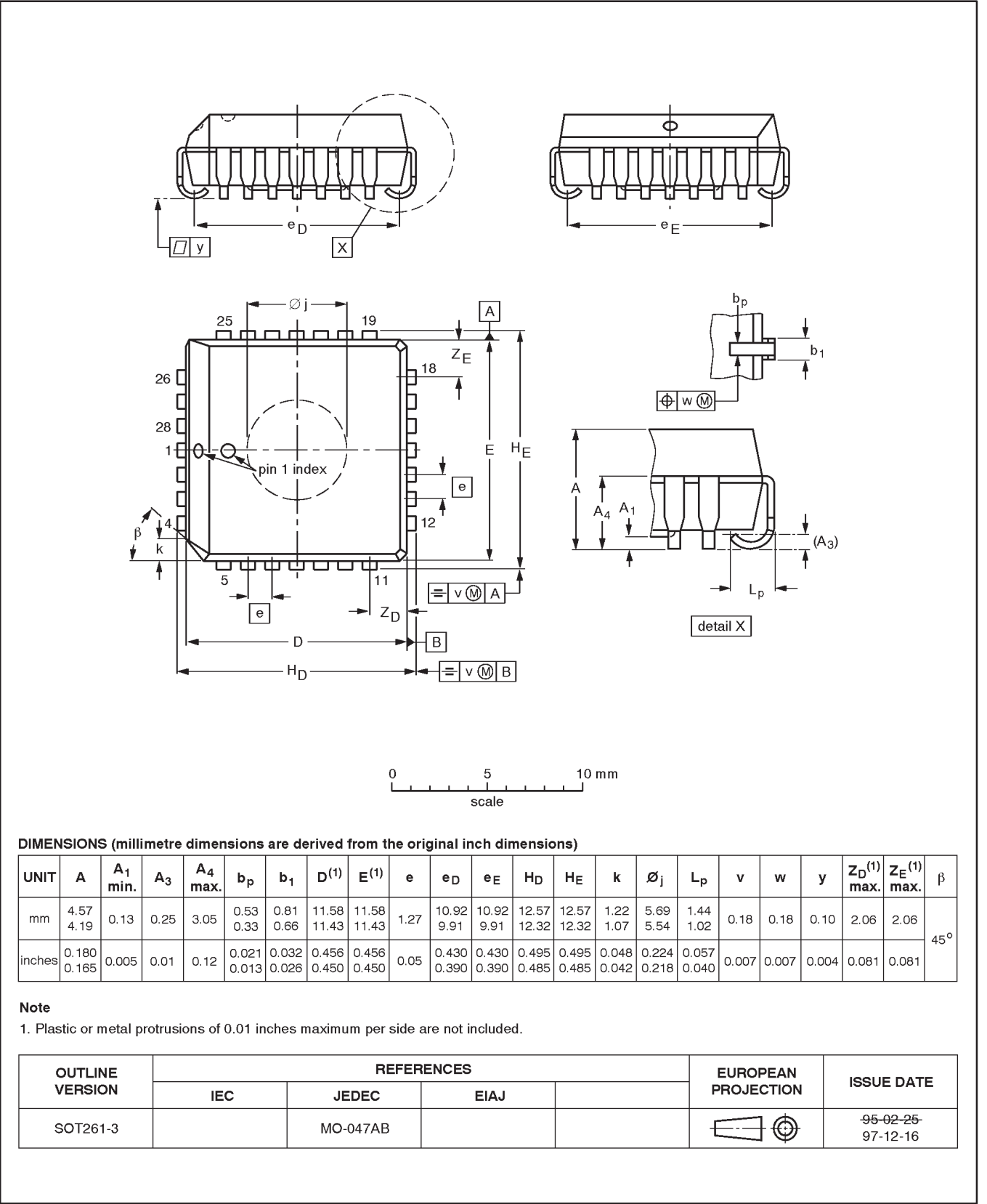
SA00012

9-bit dual latch transceiver with 8-bit parity generator/checker (3-State)

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PLCC28: plastic leaded chip carrer; 28 leads; pedestal

SOT261-3

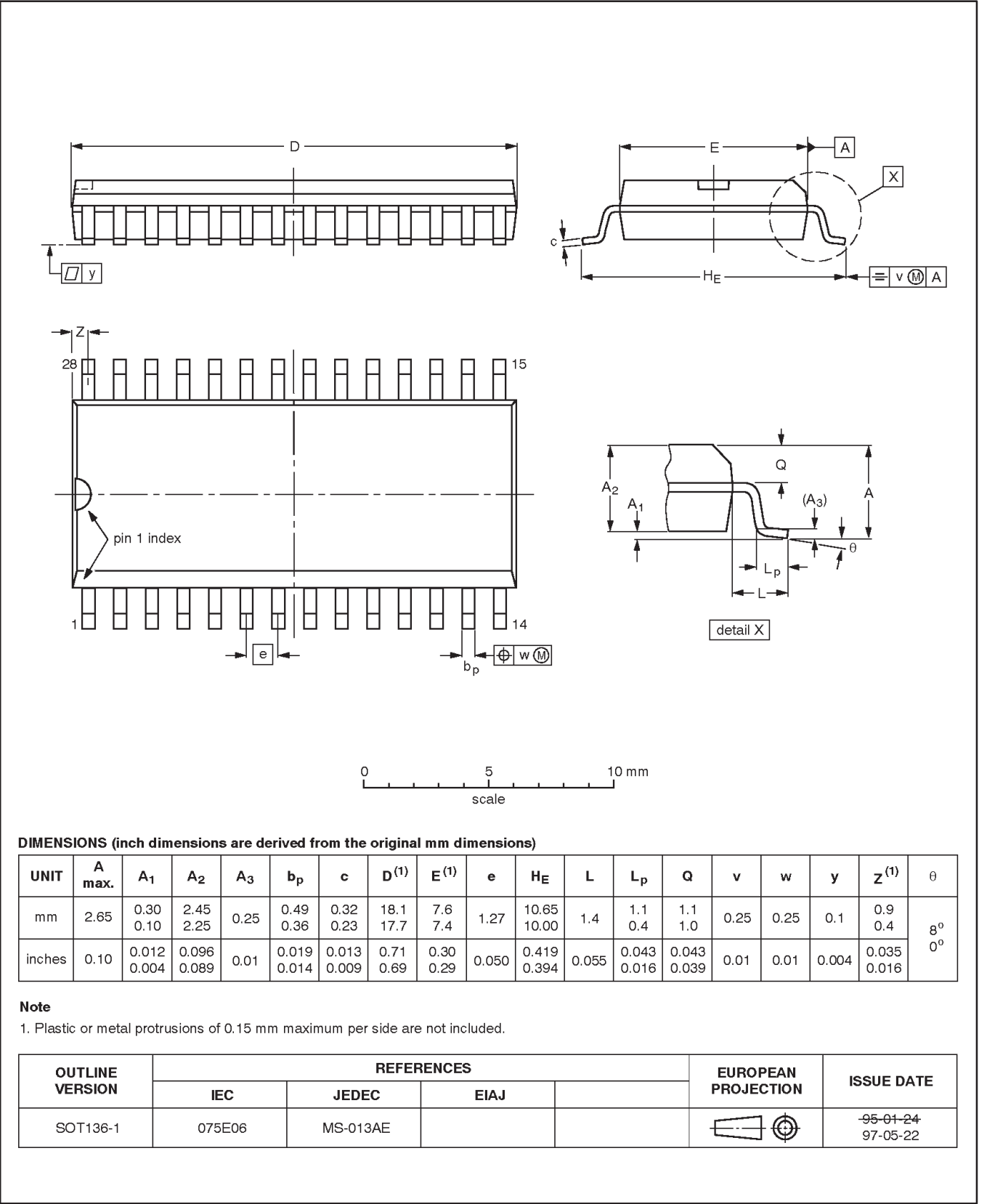


9-bit dual latch transceiver with 8-bit parity generator/checker (3-State)

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SO28: plastic small outline package; 28 leads; body width 7.5mm

SOT136-1

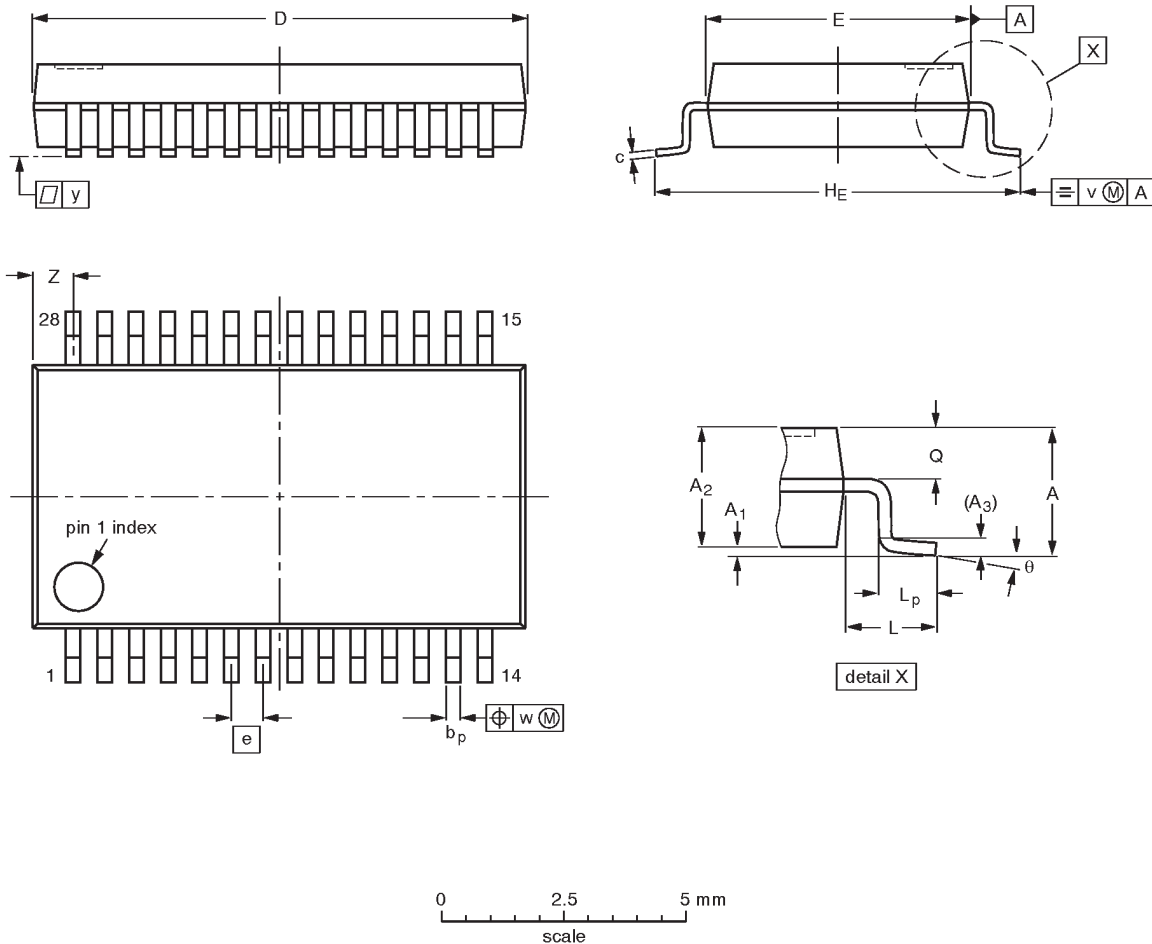


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SSOP28: plastic shrink small outline package; 28 leads; body width 5.3mm

SOT341-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				93-09-08 95-02-04

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Data sheet status

Data sheet status	Product status	Definition [1]
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