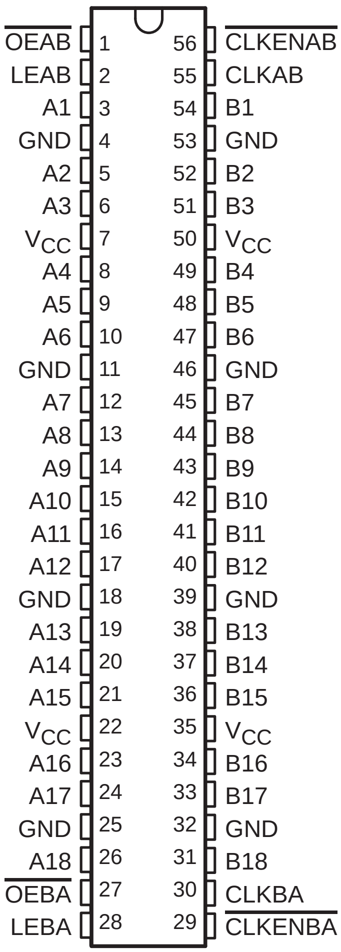
SN74ALVCHR162601
18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES123E – SEPTEMBER 1997 – REVISED FEBRUARY 1999

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages**

NOTE: For order entry:
The DGG package is abbreviated to G, and
the DGV package is abbreviated to V.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCHR162601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, clocked, and clock-enabled modes.

Data flow in each direction is controlled by output-enable ($\overline{\mathrm{OEAB}}$ and $\overline{\mathrm{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{\mathrm{CLKENAB}}$ and $\overline{\mathrm{CLKENBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When $\overline{\mathrm{OEAB}}$ is low, the outputs are active. When $\overline{\mathrm{OEAB}}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\mathrm{OEBA}}$, LEBA, CLKBA, and $\overline{\mathrm{CLKENBA}}$.

The outputs include equivalent 26-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{\mathrm{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCHR162601 is characterized for operation from –40°C to 85°C.

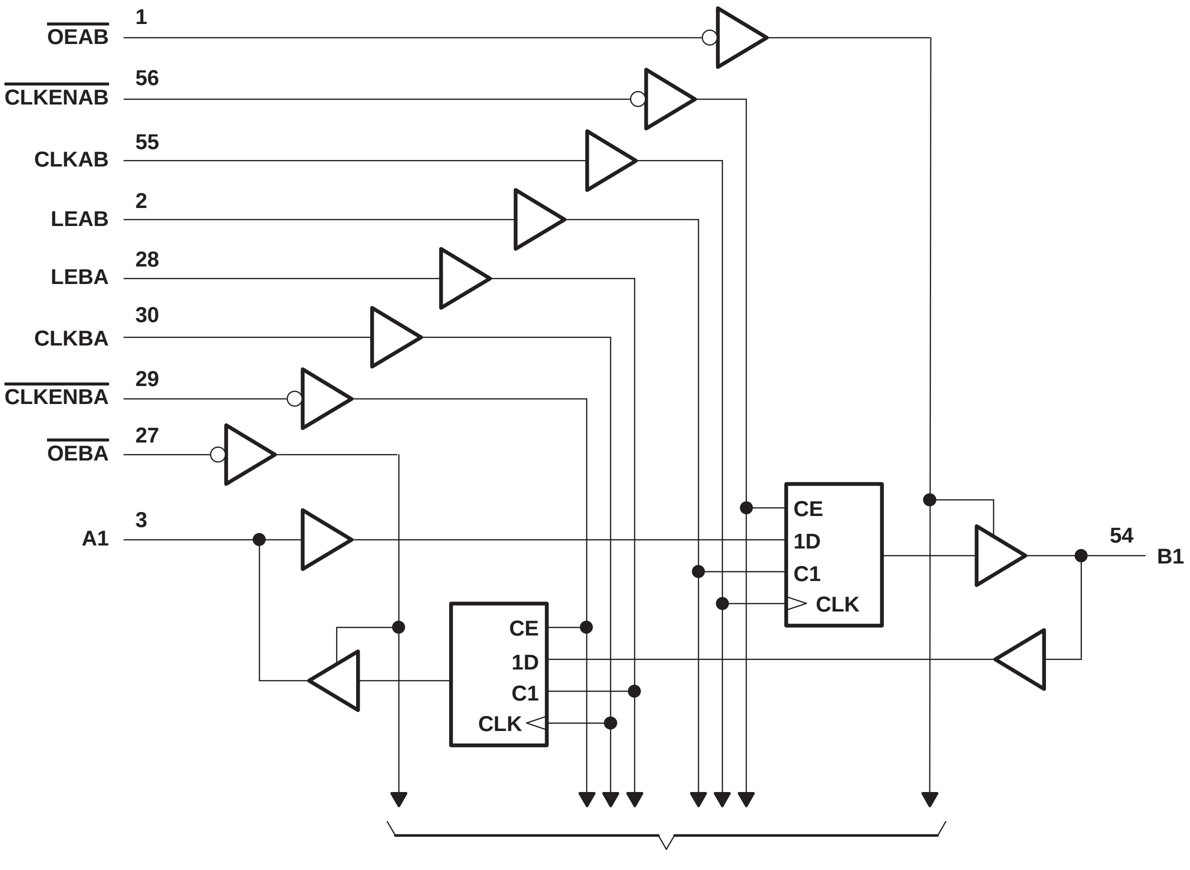
FUNCTION TABLE[†]

INPUTS					OUTPUT
$\overline{\text{CLKENAB}}$	$\overline{\text{OEAB}}$	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0[‡]
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L or H	X	B_0[‡]

[†] A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, CLKBA, and $\overline{\text{CLKENBA}}$.

[‡] Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



To 17 Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		–0.5 V to 4.6 V
Input voltage range, V_I:	Except I/O ports (see Note 1)	–0.5 V to 4.6 V
	I/O ports (see Notes 1 and 2)	–0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2)		–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Output clamp current, I_{OK} ($V_O < 0$)		–50 mA
Continuous output current, I_O		±50 mA
Continuous current through each V_{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	DGG package	81°C/W
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–2	mA
		V_{CC} = 2.3 V		–6	
		V_{CC} = 2.7 V		–8	
		V_{CC} = 3 V		–12	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		2	mA
		V_{CC} = 2.3 V		6	
		V_{CC} = 2.7 V		8	
		V_{CC} = 3 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 μA	1.65 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –2 mA	1.65 V	1.2			
		I_{OH} = –4 mA	2.3 V	1.9			
		I_{OH} = –6 mA	2.3 V	1.7			
			3 V	2.4			
		I_{OH} = –8 mA	2.7 V	2			
		I_{OH} = –12 mA	3 V	2			
V_{OL}		I_{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
		I_{OL} = 2 mA	1.65 V			0.45	
		I_{OL} = 4 mA	2.3 V			0.4	
		I_{OL} = 6 mA	2.3 V			0.55	
			3 V			0.55	
		I_{OL} = 8 mA	2.7 V			0.6	
		I_{OL} = 12 mA	3 V			0.8	
I_I		$V_I = V_{CC}$ or GND	3.6 V			±5	μA
$I_{I(hold)}$		V_I = 0.58 V	1.65 V	25			μA
		V_I = 1.07 V		–25			
		V_I = 0.7 V	2.3 V	45			
		V_I = 1.7 V		–45			
		V_I = 0.8 V	3 V	75			
		V_I = 2 V		–75			
		V_I = 0 to 3.6 V‡	3.6 V			±500	
I_{OZ}§		$V_O = V_{CC}$ or GND	3.6 V			±10	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μA
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V		4		pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V		8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

				V_{CC} = 1.8 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency				†		150		150		150	MHz
t_w	Pulse duration	LE high		†		3.3		3.3		3.3		ns
		CLK high or low		†		3.3		3.3		3.3		
t_{su}	Setup time	Data before CLK↑		†		2.3		2.4		2.1		ns
		Data before LE↓	CLK high	†		2		1.6		1.6		
			CLK low	†		1.3		1.2		1.1		
		$\overline{\text{CLKEN}}$ before CLK↑		†		2		2		1.7		
t_h	Hold time	Data after CLK↑		†		0.7		0.7		0.8		ns
		Data after LE↓	CLK high	†		1.3		1.6		1.4		
			CLK low	†		1.7		2		1.7		
		$\overline{\text{CLKEN}}$ after CLK↑		†		0.3		0.5		0.6		

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			†		150		150		150		MHz
t_{pd}	A or B	B or A		†	1	4.8		5.1	1	4.4	ns
	LEAB or LEBA			†	1	5.5		5.8	1	5.1	
	CLKAB or CLKBA			†	1.2	5.9		6.3	1.4	5.4	
t_{en}	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	B or A		†	1.1	6.3		6.6	1.1	5.6	ns
t_{dis}	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	B or A		†	1	4.2		5.1	1.6	4.7	ns

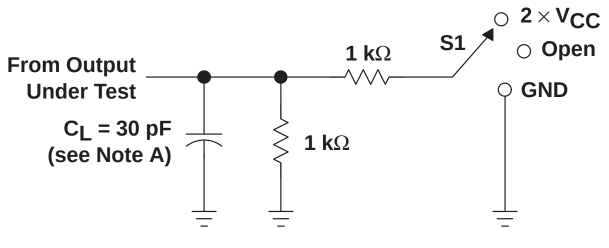
† This information was not available at the time of publication.

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 0, f = 10 MHz	†	56	63	pF
		Outputs disabled		†	12	13	

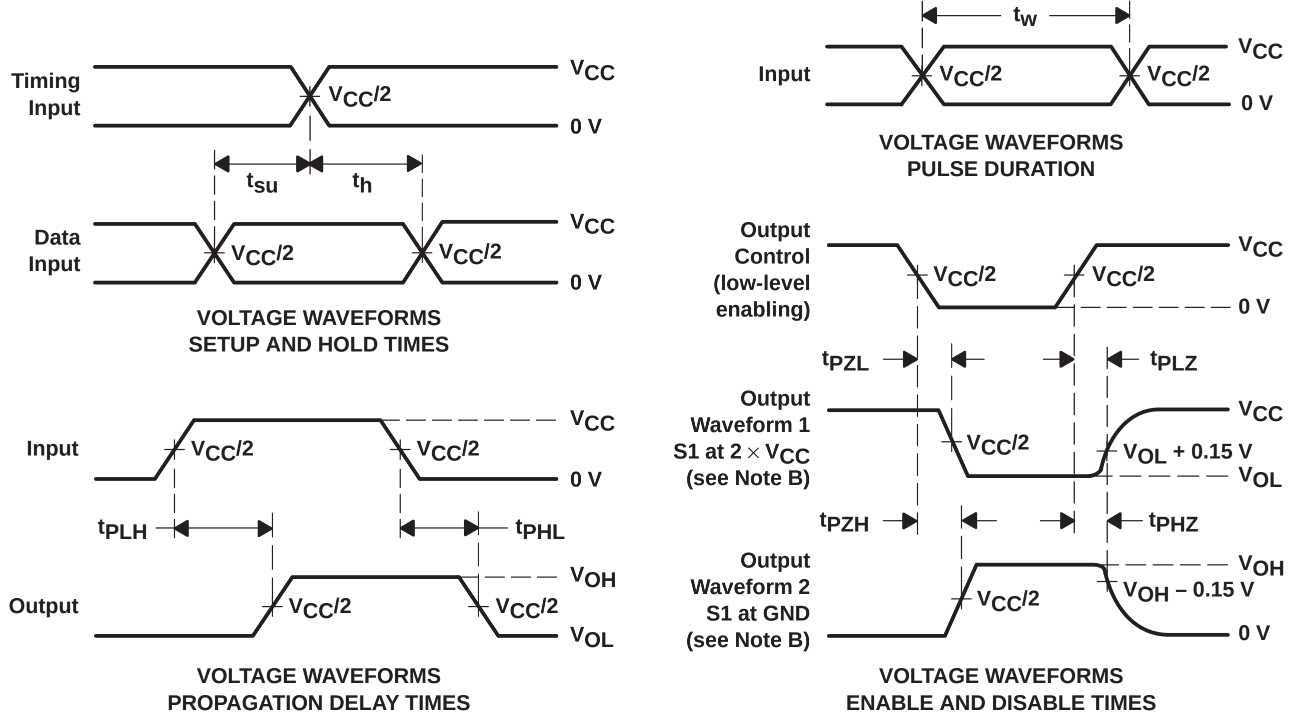
† This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.8 V



LOAD CIRCUIT

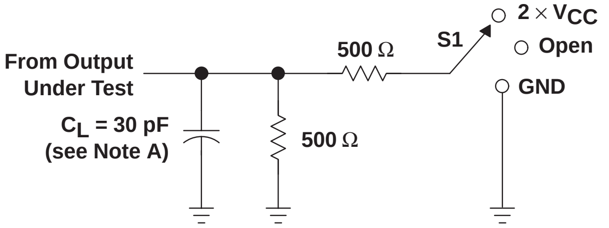
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

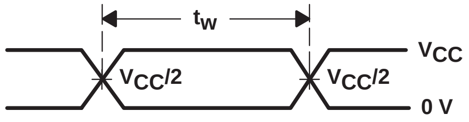
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

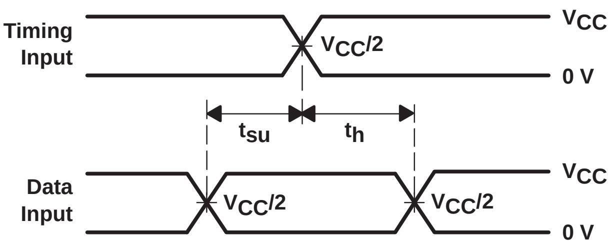


LOAD CIRCUIT

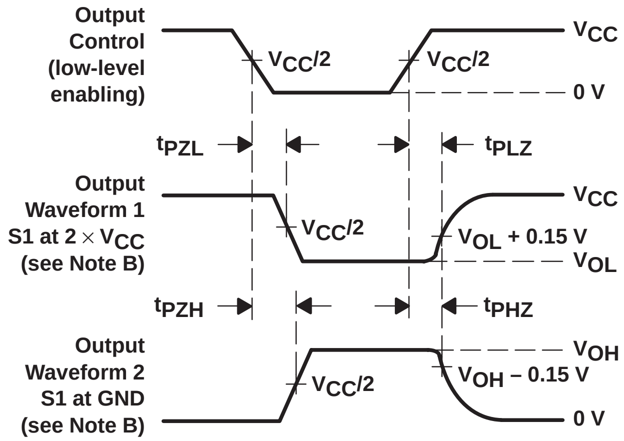
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



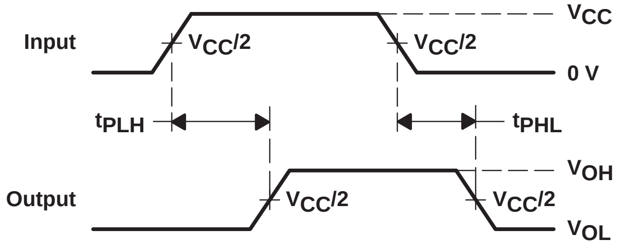
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

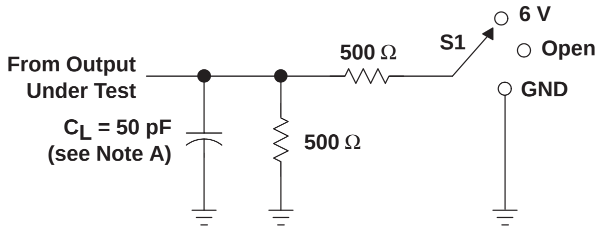


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

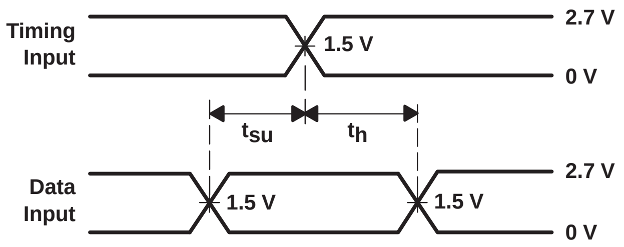
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

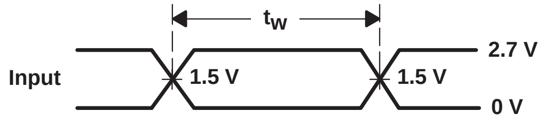


LOAD CIRCUIT

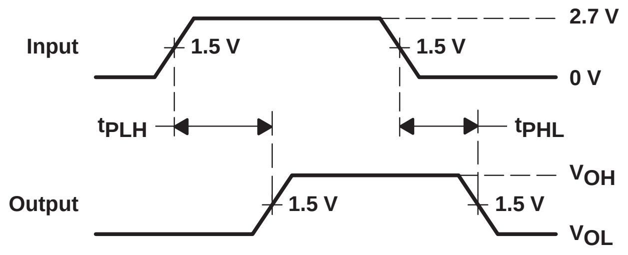
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



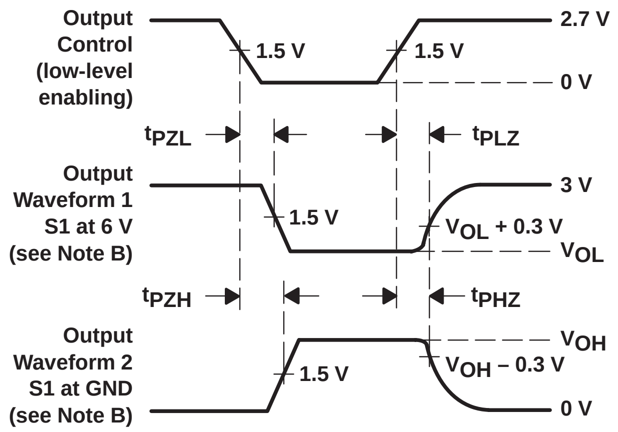
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Load Circuit and Voltage Waveforms

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