LCD controller driver for dot matrix displays

BU97701 / BU97702

The BU97701 and BU97702 are controller drivers used in dot matrix liquid crystal displays that display English-language characters, Japanese kana characters, and symbols. These products can be controlled by a 4-bit or an 8-bit MPU. All of the functions necessary to drive dot matrix displays are contained on a single chip, enabling liquid crystal displays to be configured with a small number of chips. These products are available in QFP-T80 (BU97701) and SQFP-T80 (BU97702) packages.

●Applications

Liquid crystal display systems for character displays

●Features

1) Can accommodate 5 × 7 and 5 × 10 dot matrix LCDs.
2) Equipped with an internal display data RAM of 80 × 8 bits; an expansion driver (BU9706KS) can be used to expand the display up to 80 characters.
3) Internal display data ROM of 12,000 bits
4) Diverse variety of functions includes display clear, cursor home, display on / off, display character blink, display shift, and others.

●Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Power supply voltage		V_{DD}	– 0.3 ~ + 7.0	V
Power dissipation	BU97701	Pd	900*1	mW
	BU97702		800*2	
Operating temperature		Topr	– 20 ~ + 75	°C
Storage temperature		Tstg	– 55 ~ + 125	°C

*1 Reduced by 9.0mW for each increase in Ta of 1°C over 25°C (QFP-T80).

*2 Reduced by 8.0mW for each increase in Ta of 1°C over 25°C (SQFP-T80).

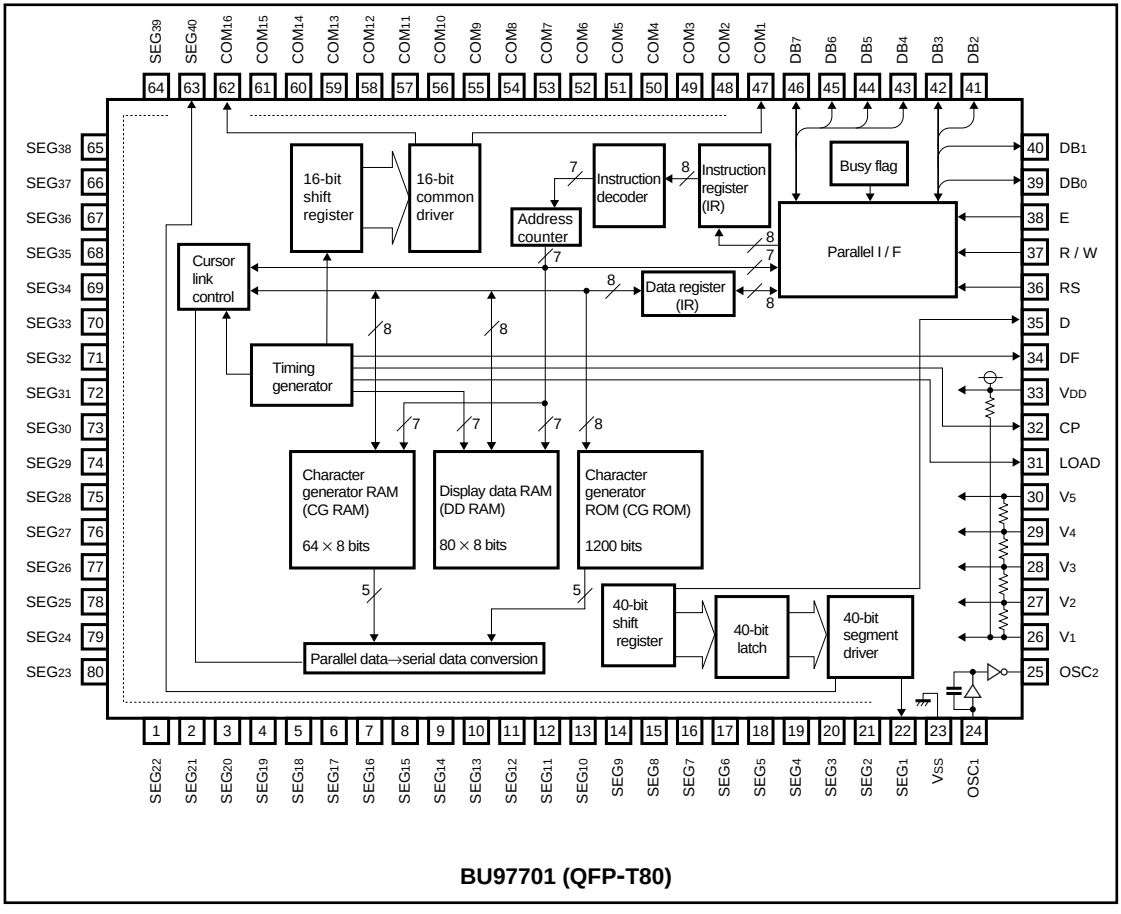
●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.5	—	5.5	V

●Model names

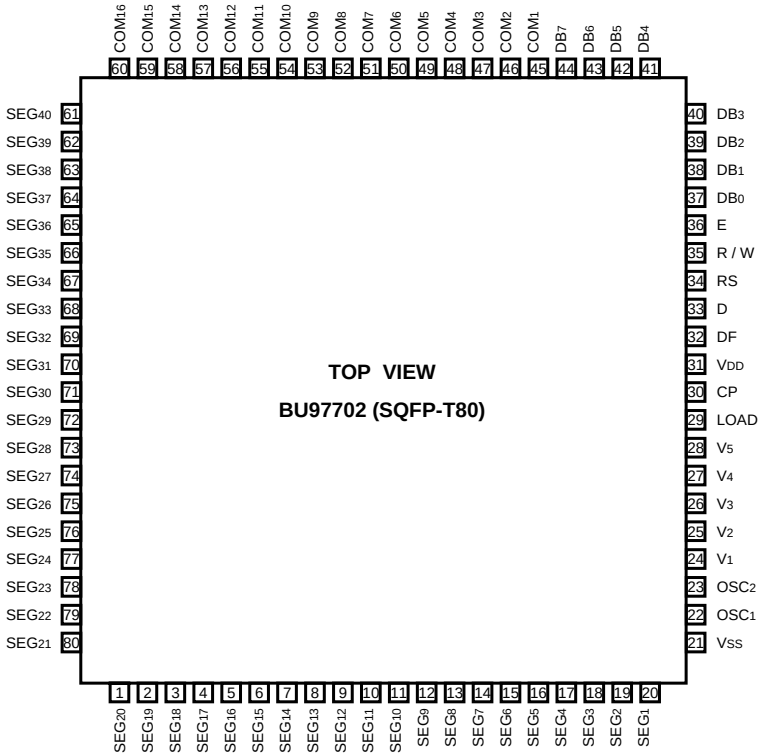
Model Number	Built-in font
BU97701-00 / BU97702-00	ROM Ver.00
BU97701-01 / BU97702-01	ROM Ver.01
BU97701-02 / BU97702-02	ROM Ver.02

●Block diagram



BU97701 (QFP-T80)

●Pin assignments

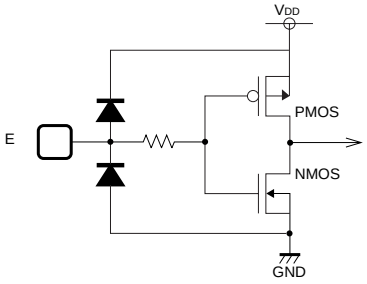


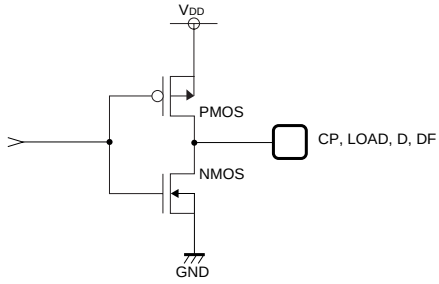
●Pin descriptions

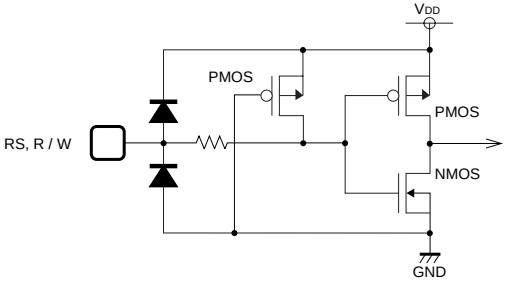
Pin No.	Pin name	Function	
36 (34)	RS	Selects the register used to read / write instructions and data. If RS = 0 and R / W = 0: Instruction register If RS = 0 and R / W = 1: Busy flag and address counter If RS = 1: Data register	
37 (35)	R / W	Signal that selects the read or write operation. This sends and receives data between the BU97701-00 (BU97702) and host computer. R / W = 0: Write R / W = 1: Read	
38 (36)	E	Signal which enables reading / writing.	
39 ~ 42 (37 ~ 40)	DB_0 ~ DB_3	Highest four bits of 3-state bi-directional bus. These send and receive data between the BU97701 (BU97702) and host MPU. These are not used with 4-bit operation.	
43 ~ 46 (41 ~ 44)	DB_4 ~ DB_7	Lowest four bits of 3-state bi-directional bus. These send and receive data between the BU97701 (BU97702) and host MPU.	
31 (29)	LOAD	Signal output which latches the serial data of the external segment driver.	
32 (30)	CP	Signal output which shifts the serial data of the external segment driver.	
34 (32)	DF	AC signal output of the LCD drive waveform.	
35 (33)	D	Outputs the data corresponding to the character pattern to an external segment register. 0: OFF data 1: ON data	
47 ~ 62 (45 ~ 60)	COM_1 ~ COM_{16}	Commons: these are common drive signals. At 1 / 8 duty, COM9 to COM16 are de-selected waveforms. At 1 / 11 duty, COM12 to COM16 are de-selected waveforms.	
22 ~ 1 (20 ~ 1) 80 ~ 63 (80 ~ 61)	SEG_1 ~ SEG_{40}	Segments: segment drive signals.	
30 (28)	V_5	LCD power supply	These must satisfy the following relationship: $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5 \geqq V_{SS}$
26 ~ 29 (24 ~ 27)	V_1 ~ V_4	LCD power supply for external driver.	
33, 23 (31, 21)	V_{DD}, V_{SS}	Power supply pins; V_{DD} = 5.0 ± 10%, V_{SS} = 0V	
24, 25 (22, 23)	OSC_1, OSC_2	When the internal clock is operating, the resistance is connected to these pins. When an external clock is operating, the clock is input to OSC_1. (OSC_2 is open.)	

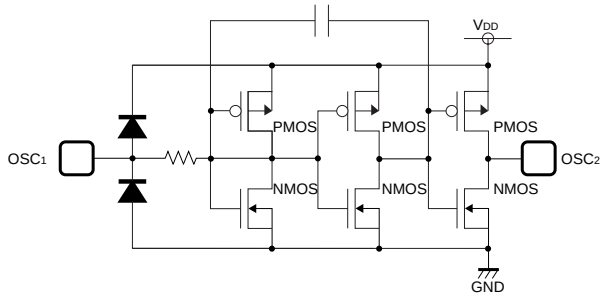
* The 97702 pin numbers are indicated within parentheses.

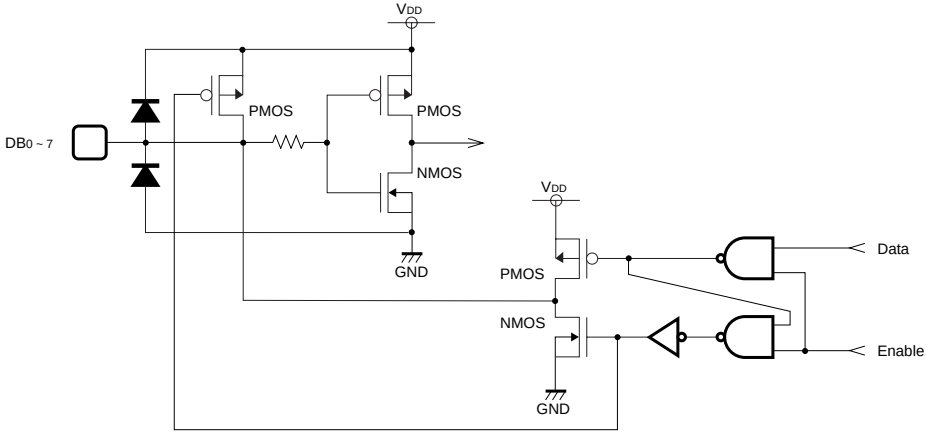
●Input / output circuits











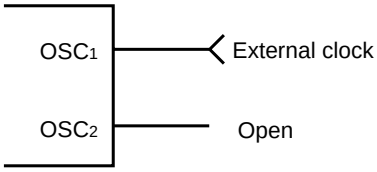
●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 5V, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement circuit
Input high level voltage 1	V_{IH1}	0.8 × V_{DD}	—	V_{DD}	V		Fig.1
Input low level voltage 1	V_{IL1}	0	—	0.2 × V_{DD}	V		Fig.1
Input high level voltage 2	V_{IH2}	2.2	—	—	V		Fig.1
Input low level voltage 2	V_{IL2}	—	—	0.8	V		Fig.1
Output high level voltage 1	V_{OH1}	V_{DD} – 0.3	—	—	V	I_{OH} = – 0.625mA	Fig.1
Output low level voltage 1	V_{OL1}	—	—	0.3	V	I_{OL} = 0.625mA	Fig.1
Output high level voltage 2	V_{OH2}	2.4	—	—	V	I_{OH} = – 1.2mA	Fig.1
Output low level voltage 2	V_{OL2}	—	—	0.4	V	I_{OL} = 2.0mA	Fig.1
COM driver ON resistance	R_{COM}	—	—	20	kΩ	I_d = ± 50µA	Fig.1
SEG driver ON resistance	R_{SEG}	—	—	30	kΩ	I_d = ± 50µA	Fig.1
Input current 1	I_{IN1}	– 1	—	1	µA	V_{IN} = 0 ~ V_{DD} Note 1	Fig.1
Input current 2	I_{IN2}	50	125	250	µA	V_{DD} = 5V, V_{IN} = 0V	Fig.1
Current dissipation	I_{DD}	—	350	600	µA	Note 2	Fig.1
External clock operating frequency	f_{IN}	125	250	350	kHz	Note 3	—
External clock duty	f_{Duty}	45	50	55	%	Note 4	—
External clock rise time	t_r	—	—	200	ns	Note 5	—
External clock fall time	tf	—	—	200	ns	Note 6	—
Internal clock oscillation frequency	f_{OSC}	190	270	350	kHz		Fig.2
Enable cycle time	t_{EC}	500	—	—	ns		Fig.2
Enable pulse width	t_{EP}	220	—	—	ns		Fig.2
Enable rise / fall times	t_{Er}, t_{Ef}	—	—	20	ns		Fig.2
Address setup time	t_{AS}	40	—	—	ns		Fig.2
Address hold time	t_{AH}	10	—	—	ns		Fig.2
Data setup time	t_{DS}	60	—	—	ns		Fig.2
Data hold time (writing)	t_{DH}	10	—	—	ns		Fig.2
Data delay time	t_{DD1}	—	—	250	ns		Fig.2
Data hold time (reading)	t_{OH}	20	—	—	ns		Fig.2
CP cycle time	t_{CC}	1800	—	—	ns		Fig.2
CP pulse time	t_{WH}, t_{WL}	800	—	—	ns		Fig.2
CP rise / fall times	t_{Cr}, t_{Cf}	—	—	100	ns		Fig.2
D delay time	t_{DD2}	—	—	100	ns		Fig.2
LOAD pulse width	t_{WCP}	800	—	—	ns		Fig.2
CP→LOAD time	t_{CL}	125	—	—	ns		Fig.2
LOAD→CP time	t_{LC}	0	—	—	ns		Fig.2
DF delay time	t_{DFD}	– 100	—	100	ns		Fig.2

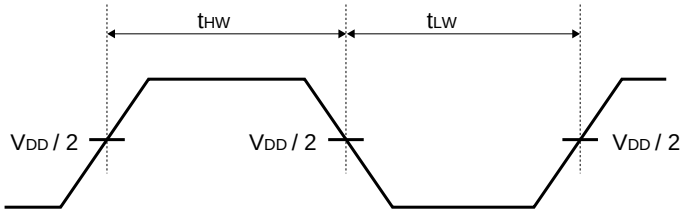
Note 1: Current does not include pull-up MOS current.

Note 2: External resistance oscillation or external clock input- · · · V_{DD} = 5.0V, f_{OSC} = fcp = 270kHz

Note 3: External clock operating

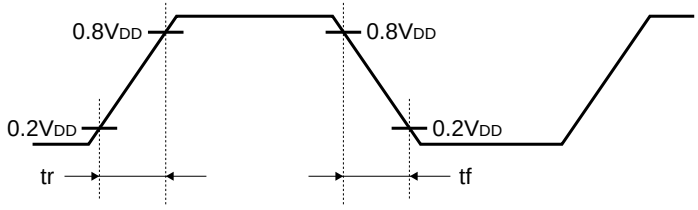


Note 4: Applies to OSC_1 pin

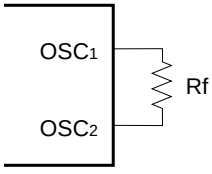


$f_{Duty} = t_{HW} / (t_{HW} + t_{LW}) \times 100$ (%)

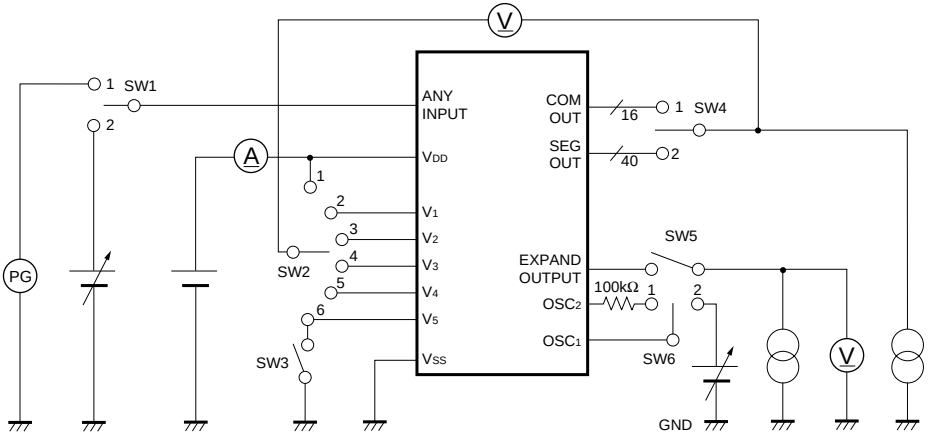
Note 5: Applies to OSC_1 pin



Note 6: Internal oscillation caused by external resistance



●Measurement circuits



SW1	1: ON resistance, output voltage measurement	SW3	ON: ON resistance measurement
	2: Input voltage, input current measurement		OFF: Current consumption measurement
SW2	1: ON resistance (in relation to V_{DD}) measurement	SW4	1: ON resistance (COM output) measurement
	2: ON resistance (in relation to V_1) measurement		2: ON resistance (COM output) measurement
	3: ON resistance (in relation to V_2) measurement	SW5	ON: Output voltage measurement
	4: ON resistance (in relation to V_3) measurement		OFF: Current consumption measurement
	5: ON resistance (in relation to V_4) measurement	SW6	1: Current consumption, ON resistance measurement
	6: ON resistance (in relation to V_5) measurement		2: Input voltage measurement

Fig. 1 DC characteristics measurement circuit

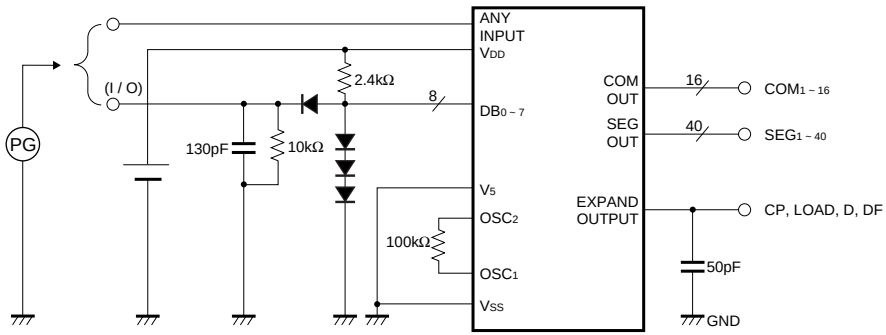


Fig. 2 Switching characteristics measurement circuit

●Timing charts

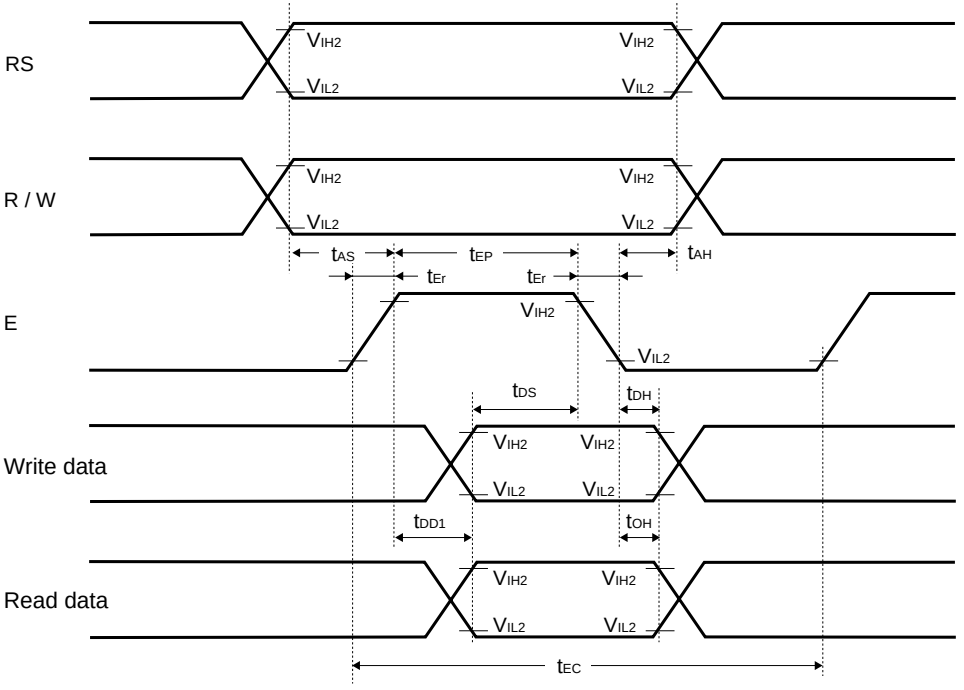


Fig. 3 Bus read / write timing

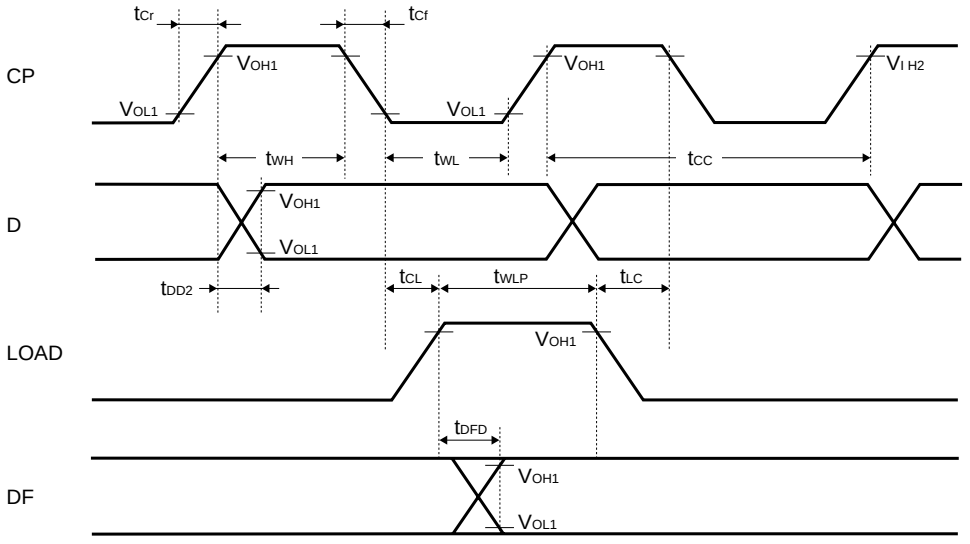


Fig. 4 Output to expansion driver

●Correspondence between character codes and character patterns

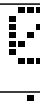
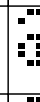
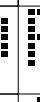
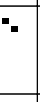
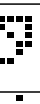
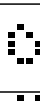
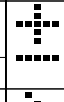
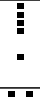
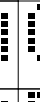
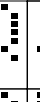
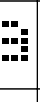
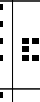
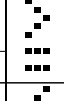
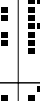
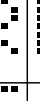
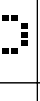
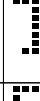
Rohm Standard: ROM Ver. 00

Upper bit / Lower bit	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
XXXX0000	CGRAM (1)															
XXXX0001	(2)															
XXXX0010	(3)															
XXXX0011	(4)															
XXXX0100	(5)															
XXXX0101	(6)															
XXXX0110	(7)															
XXXX0111	(8)															
XXXX1000	(1)															
XXXX1001	(2)															
XXXX1010	(3)															
XXXX1011	(4)															
XXXX1100	(5)															
XXXX1101	(6)															
XXXX1110	(7)															
XXXX1111	(8)															

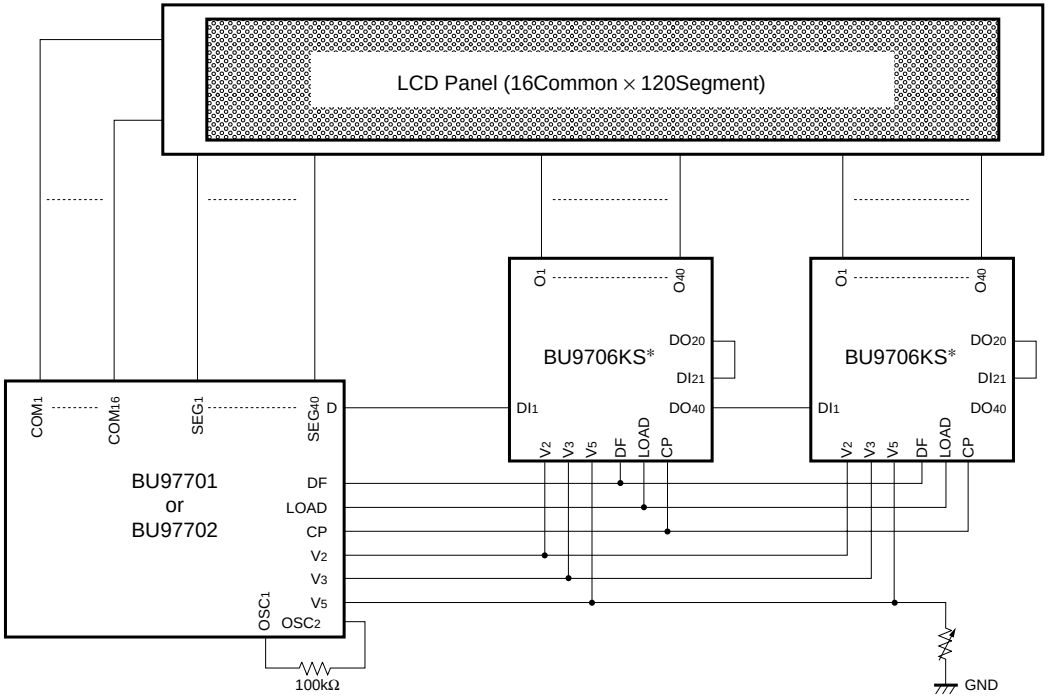
Rohm Standard: ROM Ver. 01

Upper bit / Lower bit	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
XXXX0000	CGRAM (1)															
XXXX0001	(2)															
XXXX0010	(3)															
XXXX0011	(4)															
XXXX0100	(5)															
XXXX0101	(6)															
XXXX0110	(7)															
XXXX0111	(8)															
XXXX1000	(1)															
XXXX1001	(2)															
XXXX1010	(3)															
XXXX1011	(4)															
XXXX1100	(5)															
XXXX1101	(6)															
XXXX1110	(7)															
XXXX1111	(8)															

Rohm Standard: ROM Ver. 02

Upper bit / Lower bit	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
XXXX0000	CGRAM (1)															
XXXX0001	(2)															
XXXX0010	(3)															
XXXX0011	(4)															
XXXX0100	(5)															
XXXX0101	(6)															
XXXX0110	(7)															
XXXX0111	(8)															
XXXX1000	(1)															
XXXX1001	(2)															
XXXX1010	(3)															
XXXX1011	(4)															
XXXX1100	(5)															
XXXX1101	(6)															
XXXX1110	(7)															
XXXX1111	(8)															

●Application circuit



* The BU9706KS is a segment expansion LSI.

Fig. 5

●Electrical characteristic curves

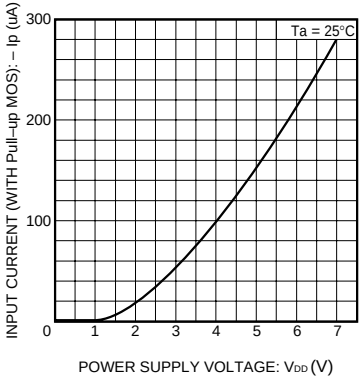


Fig. 6 Input current vs. power supply voltage

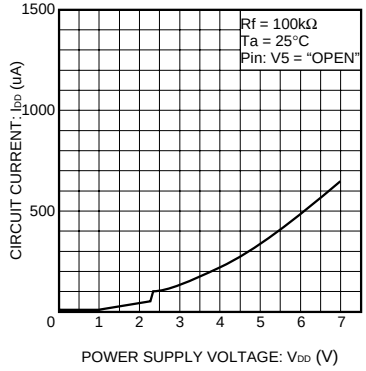
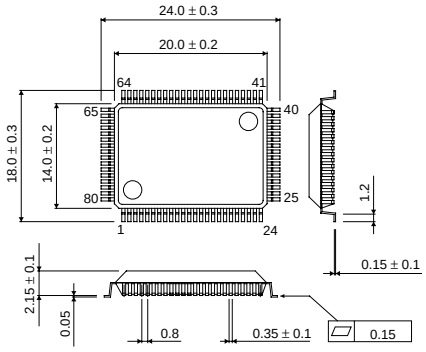


Fig. 7 Current consumption vs. power supply voltage

●External dimensions (Units: mm)

BU97701



QFP-T80

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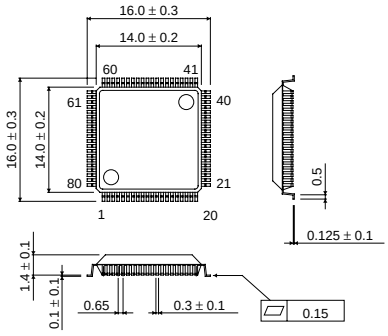

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