2.5 V 184-pin Unbuffered DDR-I SDRAM Modules

256MB & 512MB Modules

Preliminary Datasheet Rev. 0.99

- 184-pin Unbuffered 8-Byte Dual-In-Line DDR-I SDRAM non-parity and ECC-Modules for PC and Server main memory applications
- One bank 32M × 64, 32M x 72 and two bank 64M x 64, 64M × 72 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR-I SDRAM) Single + 2.5 V (± 0.2 V) power supply
- Built with 256Mbit DDR-I SDRAMs organisaed as 32Mb x 8 in 66-Lead TSOPII package
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Performance:

		-7	-7.5	-8	Unit
	Component Speed Grade	DDR266A	DDR266B	DDR200	
	Module Speed Grade	PC2100	PC2100	PC1600	
f_{CK}	Clock Frequency (max.) @ CL = 2.5	143	133	125	MHz
f_{CK}	Clock Frequency (max.) @ CL = 2	133	100	100	MHz

- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Serial Presence Detect with E^2PROM
- Jedec standard MO-206a form factor: 133.35 mm × 31.75 mm × 4.00 mm
- Jedec standard reference layout
- Gold plated contacts

The HYS64/72Dxx0x0GU are industry standard 184-pin 8-byte Dual in-line Memory Modules (DIMMs) organized as 32M × 64 and 64M × 64 for non-parity and 32M x 72 and 64M x 72 for ECC main memory applications. The memory array is designed with Double Data Rate Synchronous DRAMs. A variety of decoupling capacitors are mounted on the PC board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

Ordering Information

Type	Compliance Code	Description	SDRAM Technology
PC2100 (CL=2):			
HYS64D32000GU-7	PC2100-20330-B1	one bank 256 MB DIMM	256 MBit
HYS72D32000GU-7	PC2100-20330-B1	one bank 256 MB ECC-DIMM	256 Mbit
HYS64D64020GU-7	PC2100-20330-A1	two banks 512 MB DIMM	256 MBit
HYS72D64020GU-7	PC2100-20330-A1	two banks 512 MB ECC-DIMM	256 MBit
PC2100 (CL=2.5):			
HYS64D32000GU-7.5	PC2100-25330-B1	one bank 256 MB DIMM	256 MBit
HYS72D32000GU-7.5	PC2100-25330-B1	one bank 256 MB ECC-DIMM	256 Mbit
HYS64D64020GU-7.5	PC2100-25330-A1	two banks 512 MB DIMM	256 MBit
HYS72D64020GU-7.5	PC2100-25330-A1	two banks 512 MB ECC-DIMM	256 MBit
PC1600 (CL=2):			
HYS64D32000GU-8	PC1600-20220-B1	one bank 256 MB DIMM	256 MBit
HYS72D32000GU-8	PC1600-20220-B1	one bank 256 MB ECC-DIMM	256 Mbit
HYS64D64020GU-8	PC1600-20220-A1	two banks 512 MB DIMM	256 MBit
HYS72D64020GU-8	PC1600-20220-A1	two banks 512 MB ECC-DIMM	256 MBit

Note: All part numbers end with a place code (not shown), designating the silicon-die revision. Reference information available on request.
Example: HYS 72D32000GU-8-A, indicating Rev.A die are used for SDRAM components.

Pin Definitions and Functions

A0 - A12	Address Inputs	$\overline{S0}$, $\overline{S1}$	Chip Selects
BA0, BA1	Bank Selects	V_{DD}	Power (+ 2.5 V)
DQ0 - DQ63	Data Input/Output	V_{SS}	Ground
CB0 - CB7	Check Bits (x72 organization only)	V_{DDQ}	I/O Driver power supply
$\overline{RAS}$	Row Address Strobe	V_{DDID}	VDD Indentification flag
$\overline{CAS}$	Column Address Strobe	V_{REF}	I/O reference supply
$\overline{WE}$	Read/Write Input	V_{DDSPD}	Serial EEPROM power supply
CKE0 - CKE1	Clock Enable	SCL	Serial bus clock
DQS0 - DQS8	SDRAM low data strobes	SDA	Serial bus data line
CLK0 - CLK2,	SDRAM clock (positive lines)	SA0 - SA2	slave address select
$\overline{CLK0}$ - $\overline{CLK2}$	SDRAM clock (negative lines)	NC	no connect
DM0 - DM8 DQS9 - DQS17	SDRAM low data mask/ high data strobes		

Address Format

Density	Organization	Memory Banks	SDRAMs	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
256 MB	32M x 64	1	32M x 8	8	13/2/10	8k	64 ms	7.8 µs
256 MB	32M x 72	1	32M x 8	9	13/2/10	8k	64 ms	7.8 µs
512 MB	64M × 64	2	32M x 8	16	13/2/10	8k	64 ms	7.8 µs
512 MB	64M × 72	2	32M x 8	18	13/2/10	8k	64 ms	7.8 µs

Pin Configuration

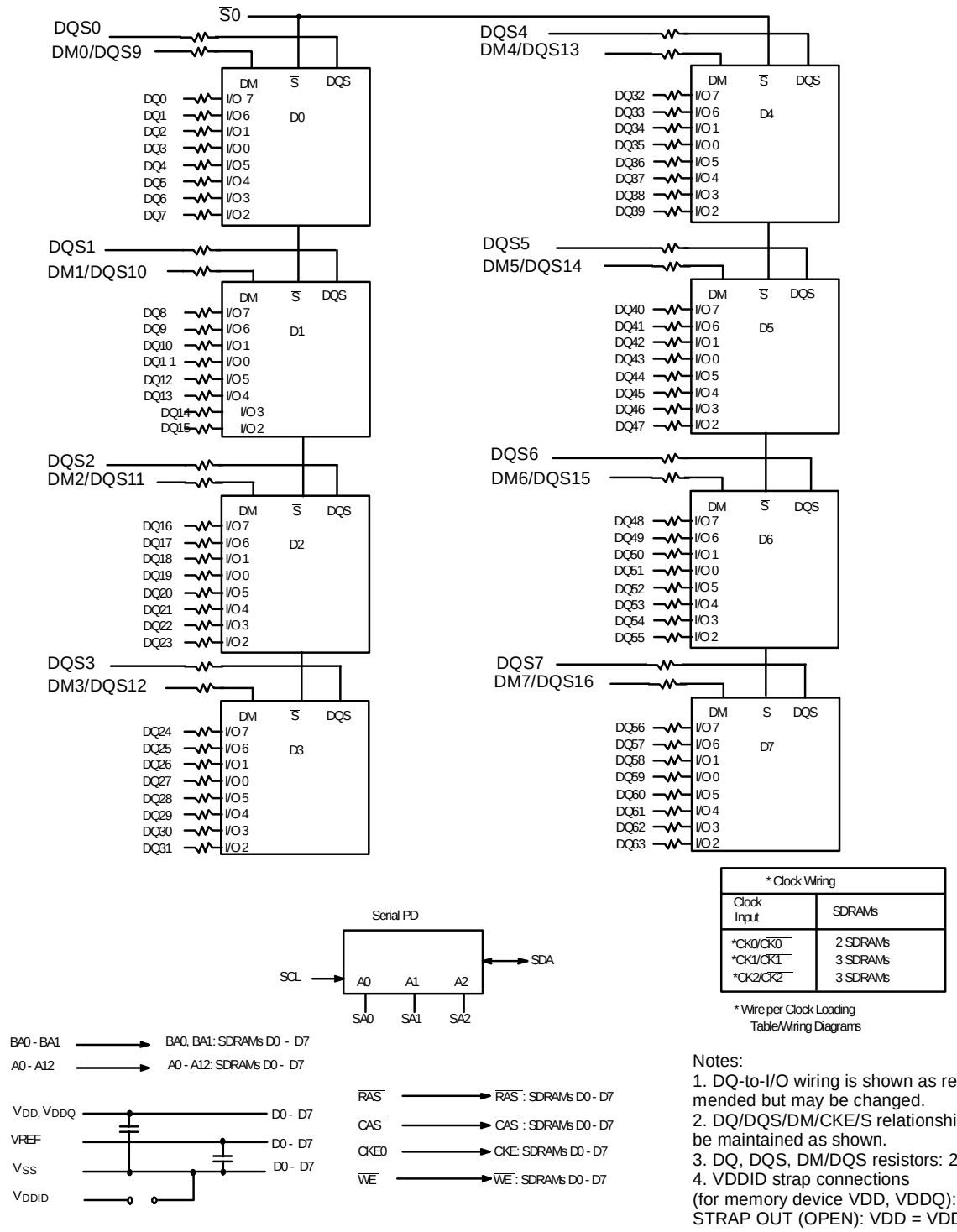
Frontside	
PIN#	Symbol
1	VREF
2	DQ0
3	VSS
4	DQ1
5	DQS0
6	DQ2
7	VDD
8	DQ3
9	NC
10	NC
11	VSS
12	DQ8
13	DQ9
14	DQS1
15	VDDQ
16	CLK1
17	$\overline{\text{CLK1}}$
18	VSS
19	DQ10
20	DQ11
21	CKE0
22	VDDQ
23	DQ16
24	DQ17
25	DQS2
26	VSS
27	A9
28	DQ18
29	A7
30	VDDQ
31	DQ19
32	A5
33	DQ24
34	VSS
35	DQ25
36	DQS3
37	A4
38	VDD
39	DQ26
40	DQ27
41	A2
42	VSS
43	A1
44	NC / CB0
45	NC / CB1
46	VDD
47	NC / DQS8

Frontside	
PIN#	Symbol
48	A0
49	NC / CB2
50	VSS
51	NC / CB3
52	BA1
KEY	
53	DQ32
54	VDDQ
55	DQ33
56	DQS4
57	DQ34
58	VSS
59	BA0
60	DQ35
61	DQ40
62	VDDQ
63	$\overline{\text{WE}}$
64	DQ41
65	$\overline{\text{CAS}}$
66	VSS
67	DQS5
68	DQ42
69	DQ43
70	VDD
71	NC
72	DQ48
73	DQ49
74	VSS
75	$\overline{\text{CLK2}}$
76	CLK2
77	VDDQ
78	DQS6
79	DQ50
80	DQ51
81	VSS
82	VDDID
83	DQ56
84	DQ57
85	VDD
86	DQS7
87	DQS8
88	DQ59
89	VSS
90	NC
91	SDA
92	SCL

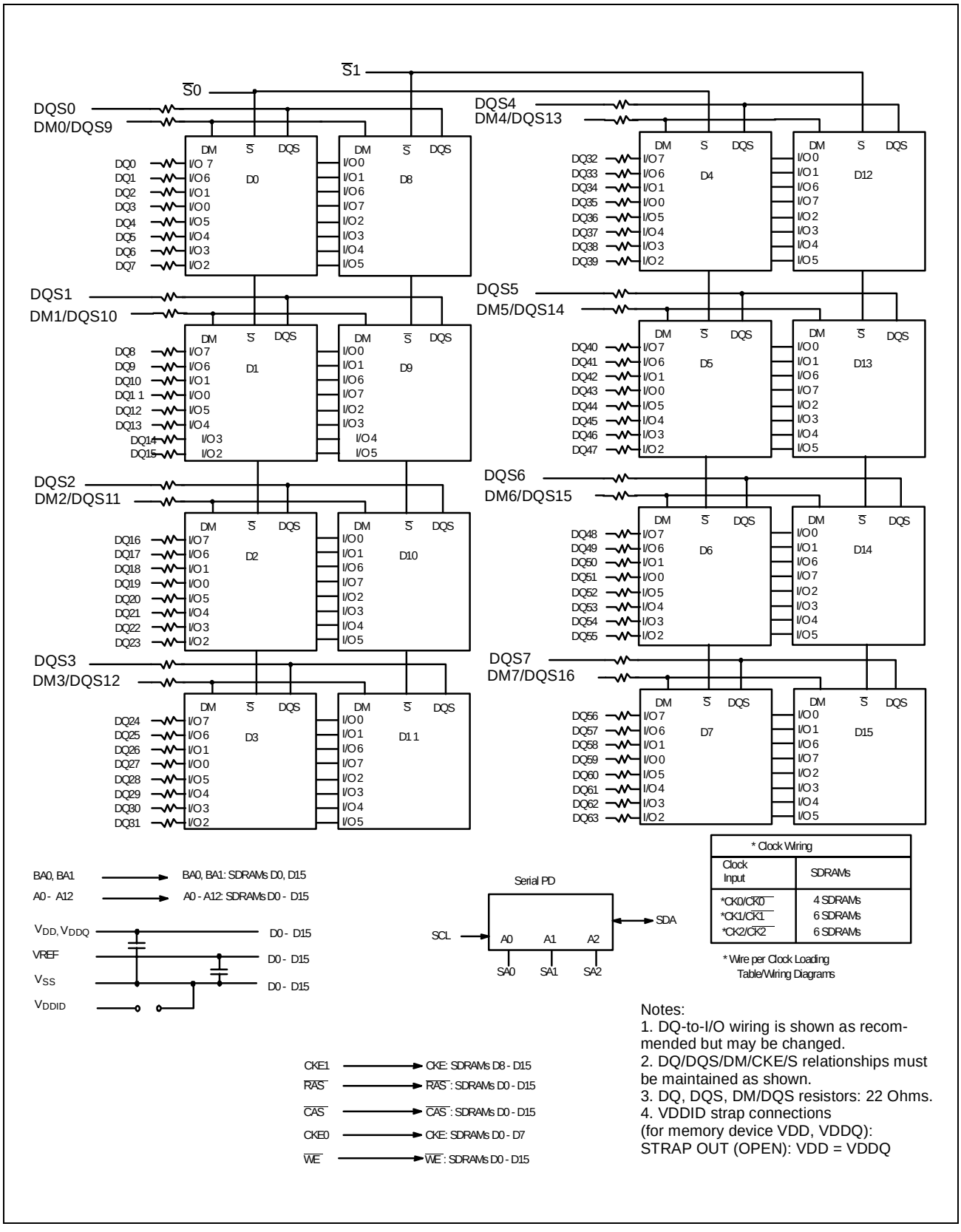
Backside	
PIN#	Symbol
93	VSS
94	DQ4
95	DQ5
96	VDDQ
97	DM0/DQS9
98	DQ6
99	DQ7
100	VSS
101	NC
102	NC
103	NC
104	VDDQ
105	DQ12
106	DQ13
107	DM1/DQS10
108	VDD
109	DQ14
110	DQ15
111	CKE1
112	VDDQ
113	NC (BA2)
114	DQ20
115	A12
116	VSS
117	DQ21
118	A11
119	DM2/DQS11
120	VDD
121	DQ22
122	A8
123	DQ23
124	VSS
125	A6
126	DQ28
127	DQ29
128	VDDQ
129	DM3/DQS12
130	A3
131	DQ30
132	VSS
133	DQ31
134	NC / CB4
135	NC / CB5
136	VDDQ
137	CK0
138	$\overline{\text{CK0}}$
139	VSS

Backside	
PIN#	Symbol
140	NC / DM8/DQS17
141	A10
142	NC / CB6
143	VDDQ
144	NC / CB7
KEY	
145	VSS
146	DQ36
147	DQ37
148	VDD
149	DM4/DQS13
150	DQ38
151	DQ39
152	VSS
153	DQ44
154	$\overline{\text{RAS}}$
155	DQ45
156	VDDQ
157	$\overline{\text{S0}}$
158	$\overline{\text{S1}}$
159	DM5/DQS14
160	VSS
161	DQ46
162	DQ47
163	NC
164	VDDQ
165	DQ52
166	DQ53
167	NC (A13)
168	VDD
169	DM6/DQS15
170	DQ54
171	DQ55
172	VDDQ
173	NC
174	DQ60
175	DQ61
176	VSS
177	DM7/DQS16
178	DQ62
179	DQ63
180	VDDQ
181	SA0
182	SA1
183	SA2
184	VDDSPD

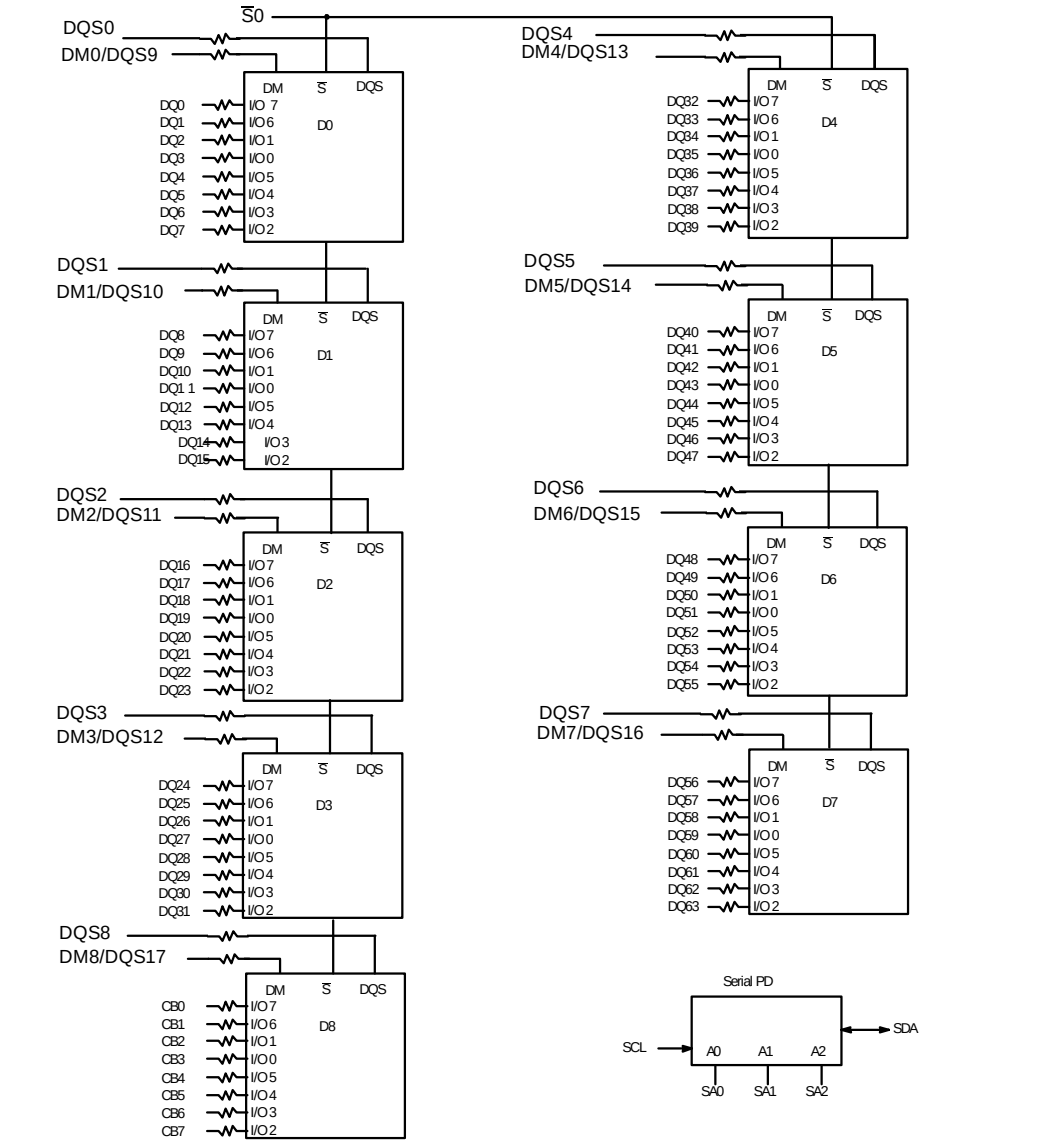
Note: Pins 44, 45, 47, 49, 51, 134, 135, 140 and 144 are NC (“no-connects”) on x64 organised non-ECC modules



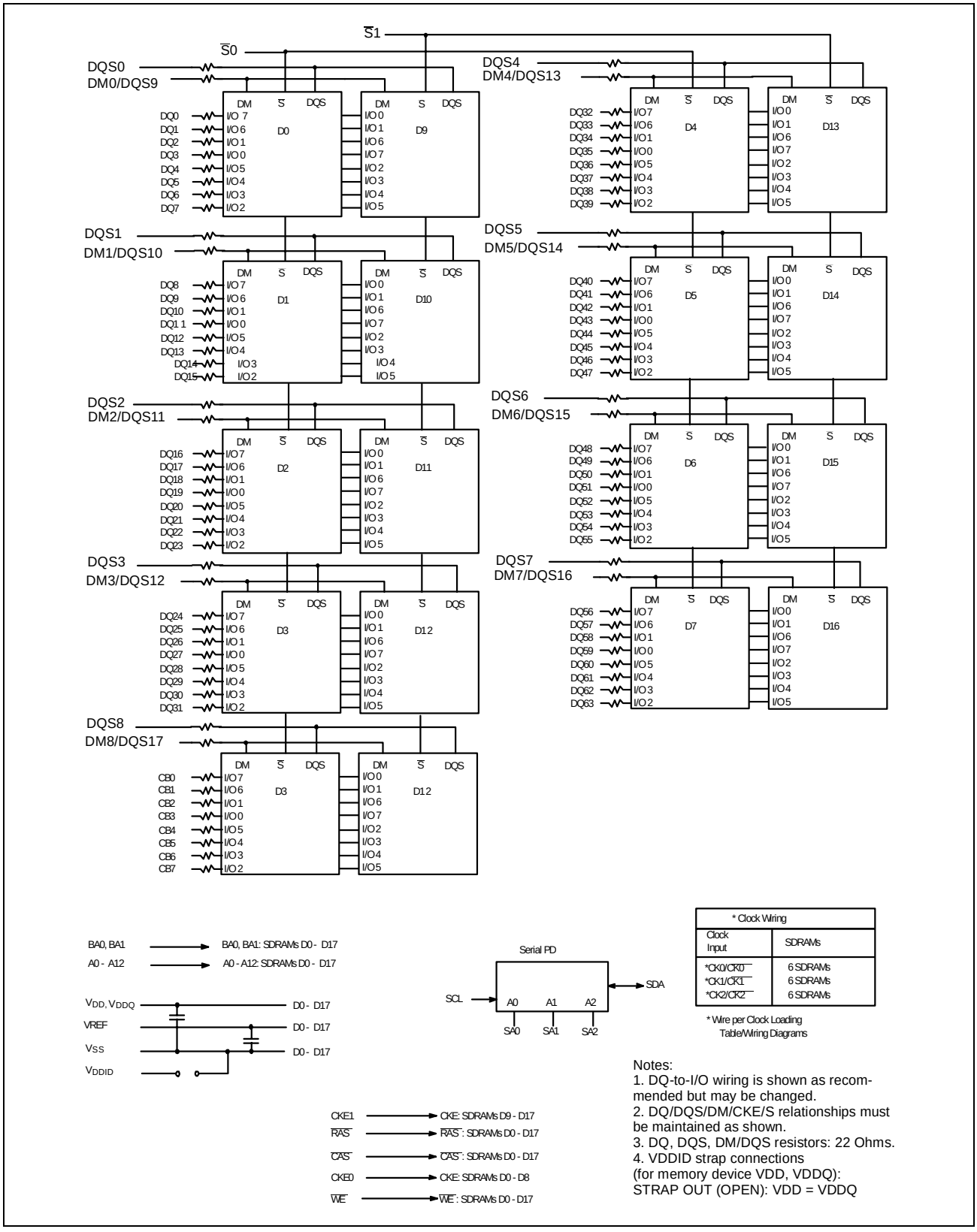
Block Diagram: One Bank 32M × 64 DDR-I SDRAM DIMM Module
HYS64D32000GU using x8 organized SDRAMs on Raw Card Version B



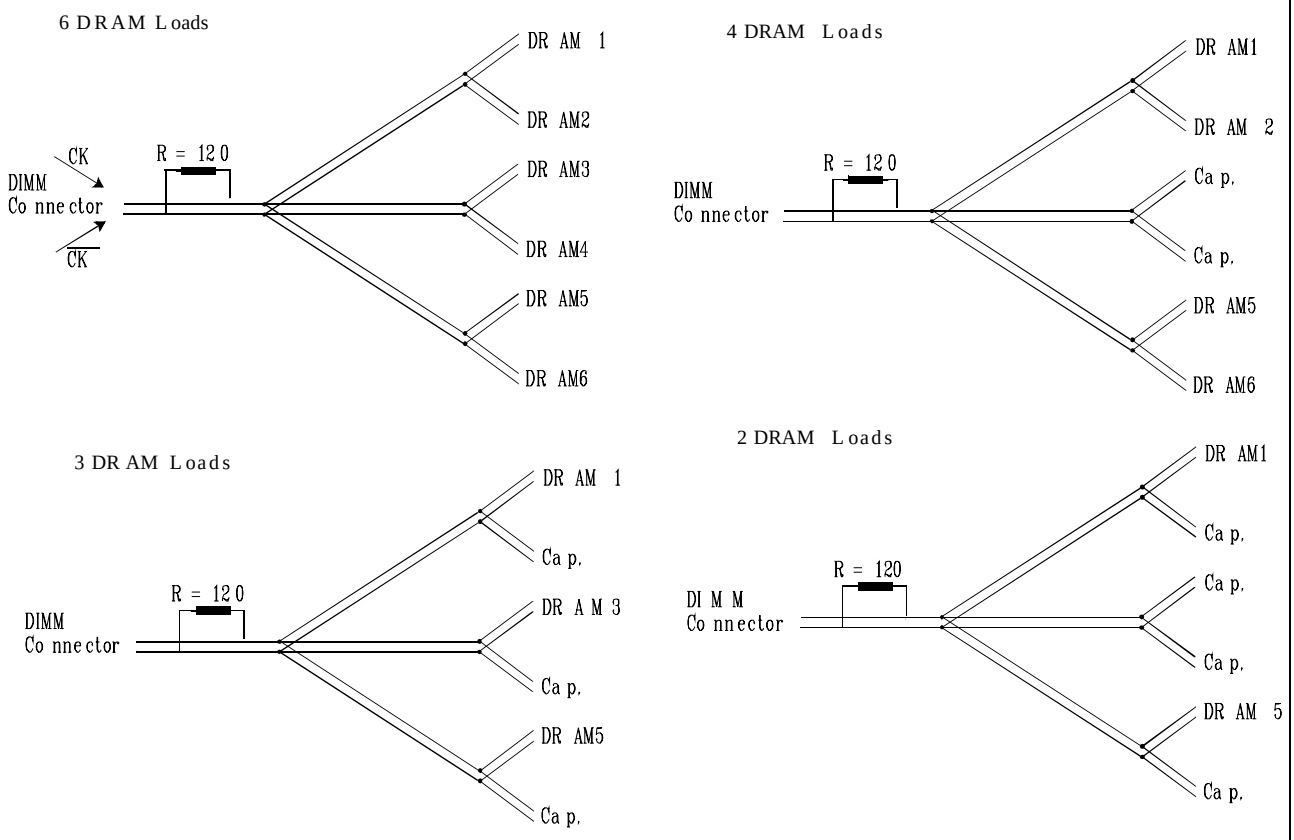
Block Diagram: Two Bank 64M × 64 DDR-I SDRAM DIMM Modules
HYS64D64020GU using x8 Organized SDRAMs on Raw Card Version A



Block Diagram: One Bank 32M × 72 DDR-I SDRAM DIMM Module HYS72D32000GU using x8 organized SDRAMs on Raw Card Version B



Block Diagram: Two Bank 64M × 72 DDR-I SDRAM DIMM Modules
HYS72D64020GU using x8 Organized SDRAMs on Raw Card Version A



Clock Net Wiring

Supply Voltage Levels

Parameter	Symbol	Limit Values			Unit	Notes
		min.	nom.	max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	–
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	1)
Input Reference Voltage	V_{REF}	1.15	1.25	1.35	V	2)
Termination Voltage	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V	3)

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.

2) Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.

3) V_{TT} of the transmitting device must track V_{REF} of the receiving device.

DC Operating Conditions (SSTL_2 Inputs)

(V_{DDQ} = 2.5 V, T_A = 70 °C, Voltage Referenced to V_{SS})

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
DC Input Logic High	$V_{IH\ (DC)}$	V_{REF} + 0.18	V_{DDQ} + 0.3	V	1)
DC Input Logic Low	$V_{IL\ (DC)}$	– 0.30	V_{REF} – 0.18	V	–
Input Leakage Current	I_{IL}	– 5	5	µA	2)
Output Leakage Current	I_{OL}	– 5	5	µA	2)

1) The relationship between the V_{DDQ} of the driving device and the V_{REF} of the receiving device is what determines noise margins. However, in the case of $V_{IH\ (max)}$ (input overdrive), it is the V_{DDQ} of the receiving device that is referenced. In the case where a device is implemented such that it supports SSTL_2 inputs but has no SSTL_2 outputs (such as a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.0 V (High corner V_{DDQ} + 300 mV).

2) For any pin under test input of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V. Values are shown per DDR-SDRAM component-

Operating, Standby and Refresh Currents (for reference only)

(values apply to one SDRAM component)

Symbol	Parameter/Condition	DDR 266A&B	DDR 200	Unit	Notes
I_{DD0}	**Operating Current**: one bank; active / precharge; $t_{RC} = t_{RC\ MIN}$; $t_{CK} = t_{CK\ MIN}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	100	90	mA	1, 2
I_{DD1}	**Operating Current**: one bank; active / read / precharge; Burst = 2; $t_{RC} = t_{RC\ MIN}$; CL = 2.5; $t_{CK} = t_{CK\ MIN}$; I_{OUT} = 0mA; address and control inputs changing once per clock cycle	120	100	mA	1, 2
I_{DD2P}	**Precharge Power-Down Standby Current**: all banks idle; power-down mode; CKE ≤ $V_{IL\ MAX}$; $t_{CK} = t_{CK\ MIN}$	20	15	mA	1, 2
I_{DD2N}	**Idle Standby Current:** $\overline{CS} \geq V_{IH\ MIN}$; all banks idle; CKE ≥ $V_{IH\ MIN}$; $t_{CK} = t_{CK\ MIN}$; address and control inputs changing once per clock cycle	40	35	mA	1, 2
I_{DD3P}	**Active Power-Down Standby Current**: one bank active; power-down mode; CKE ≤ $V_{IL\ MAX}$; $t_{CK} = t_{CK\ MIN}$	20	15	mA	1, 2
I_{DD3N}	**Active Standby Current**: one bank; active / precharge; $\overline{CS} \geq V_{IH\ MIN}$; CKE ≥ $V_{IH\ MIN}$; $t_{RC} = t_{RAS\ MAX}$; $t_{CK} = t_{CK\ MIN}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	70	60	mA	1, 2
I_{DD4R}	**Operating Current:** one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; $t_{CK} = t_{CK\ MIN}$; I_{OUT} = 0mA	190	150	mA	1, 2
I_{DD4W}	**Operating Current**: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL = 2.5; $t_{CK} = t_{CK\ MIN}$	170	130	mA	1, 2
I_{DD5}	**Auto-Refresh Current**: $t_{RC} = t_{RFC\ MIN}$	190	180	mA	1, 2
I_{DD6}	**Self-Refresh Current**: CKE ≤ 0.2V	3	3	mA	1, 2, 3
I_{DD7}	**Operating Current**: four banks; ffour bank interleaving with BL=4, address and control inputs randomly changing; 50% of data changing at every transfer; $t_{RC} = t_{RC\ MIN}$; I_{OUT} = 0mA;	325	250	mA	1, 2

1. I_{DD} specifications are tested after the device is properly initialized.
2. Input slew rate = 1V/ns.
3. Enables on-chip refresh and address counters.

AC Characteristics (for reference only) (values apply to the SDRAM component

(T_A = 0 to + 70 °C, V_{DD} = 2.5 V ± 0.2 V)

Parameter		Symbol	-7 DDR266A		-7.5 DDR266B		-8 DDR200		Unit	Notes
			min.	max.	min.	max.	min.	max.		
DQ Output Access Time from CK/$\overline{CK}$		t_{AC}	– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	–
DQS Output access Time from CK/$\overline{CK}$		t_{DQSCK}	– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	–
CLK High Level Width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	tCK	–
CLK Low Level Width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	tCK	–
Clock Period	CL = 2	t_{CK}	7.5	12	10	12	10	12	ns	1)
	CL = 2.5		7	12	7.5	12	8	12	ns	–
DQ and DM Input Hold Time		t_{DH}	0.5	–	0.5	–	0.6	–	ns	–
DQ and DM Input Setup Time		t_{DS}	0.5	–	0.5	–	0.6	–	ns	–
DQ and DM Input Pulse Width (for each input)		t_{DIPW}	1.75	–	1.75	–	2	–	ns	–
Data-Out High-impedance from CK/$\overline{CK}$		t_{HZ}	– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	–
Data-Out Low-impedance from CK/$\overline{CK}$		t_{LZ}	– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	–
Write Command to First DQS Latching Transition		t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	–
DQS-DQ Skew		t_{DQSQ}	–	+ 0.5	–	+ 0.5	–	+ 0.6	ns	–
QH Data-Out Hold Time from DQS		t_{QH}	tHP-0.75	–	tHP-0.75	–	tHP-1.0	–	ns	2)
DQS input low (high) pulse width (write cycle)		$t_{DQSL;H}$	0.35	–	0.35	–	0.35	–	t_{CK}	
DQS falling edge to CK setup time (write cycle)		t_{DSS}	0.2	–	0.2	–	0.2	–	t_{CK}	–
DQS falling edge hold time from CK (write cycle)		t_{DSH}	0.2	–	0.2	–	0.2	–	t_{CK}	
Mode register set command cycle time		t_{MRD}	14	–	15	–	16	–	ns	–
Write Preamble Setup Time		t_{WPRES}	0	–	0	–	0	–	ns	–
Write Postamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	–
Write Preamble		t_{WPRE}	0.25	–	0.25	–	0.25	–	t_{CK}	
Address and control input setup time		t_{IS}	0.9	–	0.9	–	1.2	–	ns	3)
Address and control input hold time		t_{IH}	0.9	–	0.9	–	1.2	–	ns	3)
Read Preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	–
Read Postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	–
Row Active Time		t_{RAS}	45	120K	45	120k	50	120K	ns	–
Row Cycle Time	R/W Operation	t_{RC}	65	–	65	–	70	–	ns	–
	Auto Refresh	t_{RFC}	75	–	75	–	80	–	ns	1)
$\overline{RAS}$ to $\overline{CAS}$ Delay		t_{RCD}	20	–	20	–	20	–	ns	–
Row Precharge Time		t_{RP}	20	–	20	–	20	–	ns	–
Active bank A to Active bank B command		t_{RRD}	15	–	15	–	15	–	ns	–

Parameter	Symbol	-7 DDR266A		-7.5 DDR266B		-8 DDR200		Unit	Notes
		min.	max.	min.	max.	min.	max.		
Write Recovery Time	t_{WR}	15	–	15	–	15	–	ns	–
Auto Precharge Write Recovery + Precharge Time	t_{DAL}	(twr/tck + trp/tck)						t_{CK}	–
Internal Write to Read Command Delay	t_{WTR}	1	–	1	–	1	–	t_{CK}	–
Exit self-refresh to non-read command	t_{XSNR}	75		75		80		ns	
Exit self-refresh to read command	t_{XSDR}	200		200		200		t_{CK}	
Average Periodic Refresh Intercal	t_{REF}	–	7.8	–	7.8	–	7.8	µs	–
CLK Transition Time	t_T	0.5	–	–	–	0.5	–	ns	–

1) Minimum Auto Refresh cycle time is greater than minimum cycle time during normal Read or Write operation.
2) t_{HP} is the lesser of t_{CL} and T_{CH}
3) These parameters guarantee device timing, but they are not necessarily tested on each device
they may be guaranteed by design or tester correlation
t_{IS} / t_{IH} =0.9ns for DDR266 are measured with command / address input slew rate of $\geq$ 1.0V/ns
for command / address input slew rate of $\geq$ 0.5V/ns and < 1.0V/ns t_{IS} / t_{IH} = 1.0ns should be guaranteed by design
for DDR200 t_{IS} / t_{IH} = 1.2ns command / address input slew rate of 1.0V/ns is assumed
slew rate is measured between V_{OH}(AC) and V_{OL}(AC)
CK / CK slew rates are assumed to be $\geq$ 1.0V/ns
Pulse width for command / address signals to be properly sampled at rising edges of clock shall be a minimum of 2.2ns

Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +55	°C	
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
T_{STG}	Storage Temperature	-50 to +100	°C	1)
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1)
	Barometric Pressure (operating and storage)	105 to 69	K Pascal	2)

1) stresses greater than those listed may cause permanent damage to the device. Device functional operation at or above these conditions is not implied.
2) up to 3000 m (9850 ft)

SPD Codes for PC1600 Modules "-8"

Byte#	Description	SPD Entry Value	Hex			
			256MByte one bank x64	256 MByte one bank x72	512 MByte two banks x64	512 MByte two banks x72
0	Number of SPD Bytes	128	80			
1	Total Bytes in Serial PD	256	08			
2	Memory Type	DDR-SDRAM	07			
3	Number of Row Addresses (without BA bits)	13	0D			
4	Number of Column Addresses	10	0A			
5	Number of DIMM Banks	1 / 2	01	01	02	02
6	Module Data Width	x64 / x72	40	48	40	48
7	Module Data Width (cont'd)	0	00			
8	Module Interface Levels	SSTL_2.5	04			
9	SDRAM Cycle Time at CL = 2.5	8 ns	80			
10	SDRAM Access Time from Clock at CL = 2.5	0.8 ns	80			
11	DIMM Config	non-ECC / ECC	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 7.8 µs	82			
13	SDRAM Width, Primary	x8	08			
14	Error Checking SDRAM Data Width	na / x8	00	08	00	08
15	Minimum Clock Delay for Back-to-Back Random Column Address	t_{CCD} = 1 CLK	01			
16	Burst Length Supported	2, 4 & 8	0E			
17	Number of SDRAM Banks	4	04			
18	Supported $\overline{CAS}$ Latencies	$\overline{CAS}$ latency = 2 & 2.5	0C			
19	$\overline{CS}$ Latencies	$\overline{CS}$ latency = 0	01			
20	$\overline{WE}$ Latencies	Write latency = 1	02			
21	SDRAM DIMM Module Attributes	unbuffered	20			
22	SDRAM Device Attributes: General		C0			
23	Min. Clock Cycle Time at $\overline{CAS}$ Latency = 2	10.0 ns	A0			
24	Max. Data Access Time from Clock for CL = 2	0.8 ns	80			
25	Minimum Clock Cycle Time at CL = 1.5	not supported	00			
26	Maximum Data Access Time from Clock at CL = 1.5	not supported	00			
27	Minimum Row Precharge Time	20 ns	50			

Byte#	Description	SPD Entry Value	Hex			
			256MByte one bank x64	256 MByte one bank x72	512 MByte two banks x64	512 MByte two banks x72
28	Minimum Row Active to Row Active Delay t_{RRD}	15 ns	3C			
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay t_{RCD}	20 ns	50			
30	Minimum $\overline{RAS}$ Pulse Width t_{RAS}	50 ns	32			
31	Module Bank Density (per bank)	256MByte	40			
32	Addr. and Command Setup Time	1.2 ns	C0			
33	Addr. and Command Hold Time	1.2 ns	C0			
34	Data Input Setup Time	0.6 ns	60			
35	Data Input Hold Time	0.6 ns	60			
36-40	Superset Information (may be used in future)	–	00			
41	Minimum Core Cycle Time tRC	70 ns	46			
42	Min. Auto Refresh Cmd Cycle Time tRFC	80 ns	50			
43	Maximum Clock Cycle Time tck	12 ns	30			
44	Max. DQS-DQ Skew tDDSQ	0.6 ns	3C			
45	X-Factor tQHS	1.0 ns	A0			
46-61	Superset Information (may be used in future)	-	00			
62	SPD Revision	Revision 0.0	00			
63	Checksum for Bytes 0 - 62	–	C7	D9	C8	DA
64-127	Manufacturers Information	–				

SPD Codes for PC2100 Modules "-7.5"

Byte#	Description	SPD Entry Value	Hex			
			256MByte one bank x64	256 MByte one bank x72	512 MByte two banks x64	512 MByte two banks x72
0	Number of SPD Bytes	128	80			
1	Total Bytes in Serial PD	256	08			
2	Memory Type	DDR-SDRAM	07			
3	Number of Row Addresses (without BA bits)	13	0D			
4	Number of Column Addresses	10	0A			
5	Number of DIMM Banks	1 / 2	01	01	02	02
6	Module Data Width	x64 / x72	40	48	40	48
7	Module Data Width (cont'd)	0	00			
8	Module Interface Levels	SSTL_2.5	04			
9	SDRAM Cycle Time at CL = 2.5	7.5 ns	75			
10	SDRAM Access Time from Clock at CL = 2.5	0.75 ns	75			
11	DIMM Config	non-ECC / ECC	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 7.8 µs	82			
13	SDRAM Width, Primary	x8	08			
14	Error Checking SDRAM Data Width	na / x8	00	08	00	08
15	Minimum Clock Delay for Back-to-Back Random Column Address	t_{CCD} = 1 CLK	01			
16	Burst Length Supported	2, 4 & 8	0E			
17	Number of SDRAM Banks	4	04			
18	Supported $\overline{CAS}$ Latencies	$\overline{CAS}$ latency = 2 & 2.5	0C			
19	$\overline{CS}$ Latencies	$\overline{CS}$ latency = 0	01			
20	$\overline{WE}$ Latencies	Write latency = 1	02			
21	SDRAM DIMM Module Attributes	unbuffered	20			
22	SDRAM Device Attributes: General		C0			
23	Min. Clock Cycle Time at $\overline{CAS}$ Latency = 2	10.0 ns	A0			
24	Max. Data Access Time from Clock for CL = 2	0.75 ns	75			
25	Minimum Clock Cycle Time at CL = 1.5	not supported	00			
26	Maximum Data Access Time from Clock at CL = 1.5	not supported	00			
27	Minimum Row Precharge Time	20 ns	50			

Byte#	Description	SPD Entry Value	Hex			
			256MByte one bank x64	256 MByte one bank x72	512 MByte two banks x64	512 MByte two banks x72
28	Minimum Row Active to Row Active Delay t_{RRD}	15 ns	3C			
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay t_{RCD}	20 ns	50			
30	Minimum $\overline{RAS}$ Pulse Width t_{RAS}	45 ns	2D			
31	Module Bank Density (per bank)	256MByte	40			
32	Addr. and Command Setup Time	0.9 ns	90			
33	Addr. and Command Hold Time	0.9 ns	90			
34	Data Input Setup Time	0.5 ns	50			
35	Data Input Hold Time	0.5 ns	50			
36-40	Superset Information (may be used in future)	–	00			
41	Minimum Core Cycle Time tRC	65 ns	41			
42	Min. Auto Refresh Cmd Cycle Time tRFC	75 ns	4B			
43	Maximum Clock Cycle Time tck	12 ns	30			
44	Max. DQS-DQ Skew tDDSQ	0.5 ns	32			
45	X-Factor tQHS	0.75 ns	75			
46-61	Superset Information (may be used in future)	-	00			
62	SPD Revision	Revision 0.0	00			
63	Checksum for Bytes 0 - 62	–	E2	F4	E3	F5
64-127	Manufacturers Information	–				

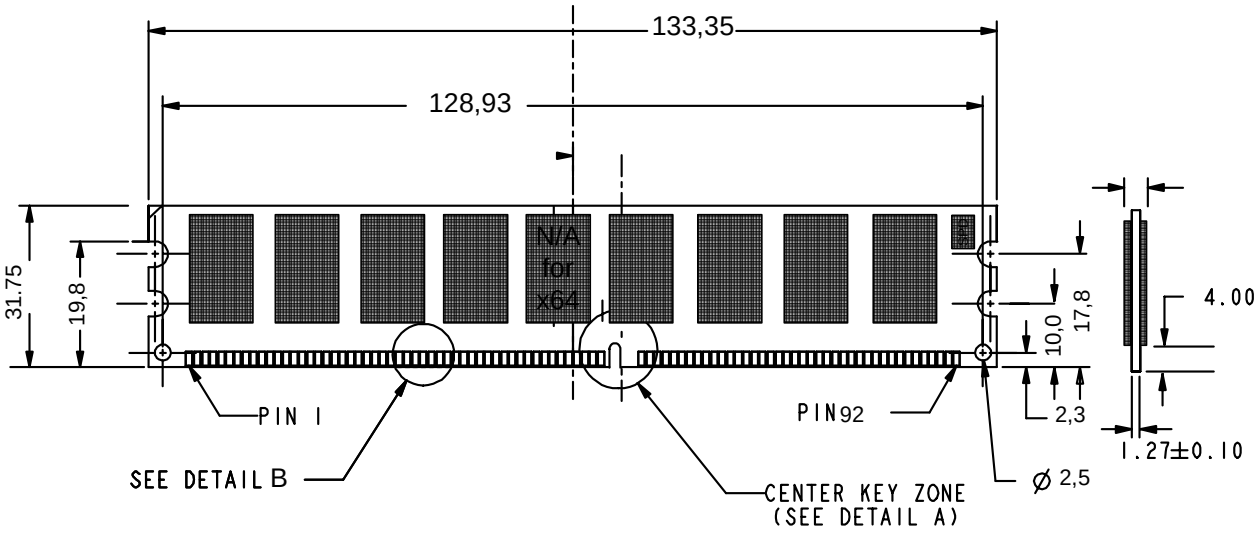
SPD Codes for PC2100 Modules "-7"

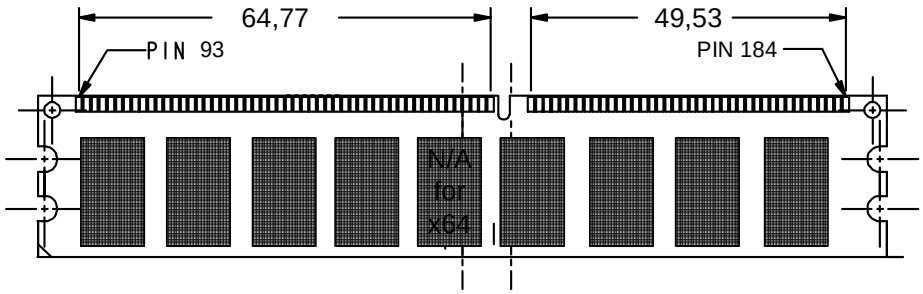
Byte#	Description	SPD Entry Value	Hex			
			256MByte one bank x64	256 MByte one bank x72	512 MByte two banks x64	512 MByte two banks x72
0	Number of SPD Bytes	128	80			
1	Total Bytes in Serial PD	256	08			
2	Memory Type	DDR-SDRAM	07			
3	Number of Row Addresses (without BA bits)	13	0D			
4	Number of Column Addresses	10	0A			
5	Number of DIMM Banks	1 / 2	01	01	02	02
6	Module Data Width	x64 / x72	40	48	40	48
7	Module Data Width (cont'd)	0	00			
8	Module Interface Levels	SSTL_2.5	04			
9	SDRAM Cycle Time at CL = 2.5	7 ns	70			
10	SDRAM Access Time from Clock at CL = 2.5	0.75 ns	75			
11	DIMM Config	non-ECC / ECC	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 7.8 µs	82			
13	SDRAM Width, Primary	x8	08			
14	Error Checking SDRAM Data Width	na / x8	00	08	00	08
15	Minimum Clock Delay for Back-to-Back Random Column Address	t_{CCD} = 1 CLK	01			
16	Burst Length Supported	2, 4 & 8	0E			
17	Number of SDRAM Banks	4	04			
18	Supported $\overline{CAS}$ Latencies	$\overline{CAS}$ latency = 2 & 2.5	0C			
19	$\overline{CS}$ Latencies	$\overline{CS}$ latency = 0	01			
20	$\overline{WE}$ Latencies	Write latency = 1	02			
21	SDRAM DIMM Module Attributes	unbuffered	20			
22	SDRAM Device Attributes: General		C0			
23	Min. Clock Cycle Time at $\overline{CAS}$ Latency = 2	7.5 ns	75			
24	Max. Data Access Time from Clock for CL = 2	0.75 ns	75			
25	Minimum Clock Cycle Time at CL = 1.5	not supported	00			
26	Maximum Data Access Time from Clock at CL = 1.5	not supported	00			
27	Minimum Row Precharge Time	20 ns	50			

Byte#	Description	SPD Entry Value	Hex			
			256MByte one bank x64	256 MByte one bank x72	512 MByte two banks x64	512 MByte two banks x72
28	Minimum Row Active to Row Active Delay t_{RRD}	15 ns	3C			
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay t_{RCD}	20 ns	50			
30	Minimum $\overline{RAS}$ Pulse Width t_{RAS}	45 ns	2D			
31	Module Bank Density (per bank)	256MByte	40			
32	Addr. and Command Setup Time	0.9 ns	90			
33	Addr. and Command Hold Time	0.9 ns	90			
34	Data Input Setup Time	0.5 ns	50			
35	Data Input Hold Time	0.5 ns	50			
36-40	Superset Information (may be used in future)	–	00			
41	Minimum Core Cycle Time tRC	65 ns	41			
42	Min. Auto Refresh Cmd Cycle Time tRFC	75 ns	4B			
43	Maximum Clock Cycle Time tck	12 ns	30			
44	Max. DQS-DQ Skew tDDSQ	0.5 ns	32			
45	X-Factor tQHS	0.75 ns	75			
46-61	Superset Information (may be used in future)	-	00			
62	SPD Revision	Revision 0.0	00			
63	Checksum for Bytes 0 - 62	–	B2	C4	B3	C5
64-127	Manufacturers Information	–				

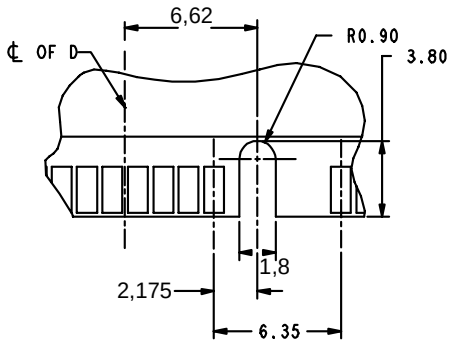
Package Outlines

Simplified Mechanical Drawing
(for details see JEDEC document MO-206a)
DDR-I Unbuffered DIMM Modules

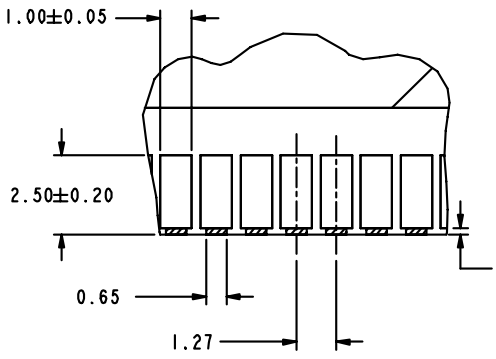




Detail A:



Detail B:



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