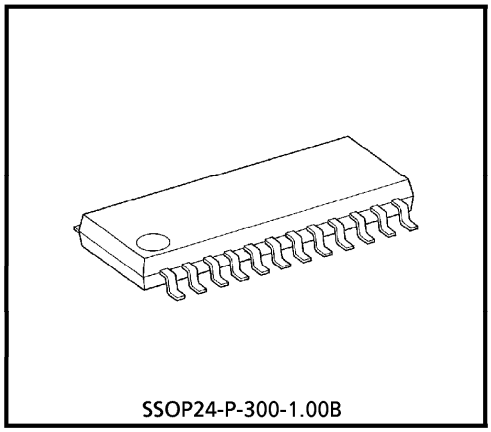
TENTATIVE

TOSHIBA INTELLIGENT POWER DEVICE
SILICON MONOLITHIC POWER MOS INTEGRATED CIRCUIT

TPD7100F

2ch HIGH-SIDE N-ch POWER MOSFET GATE DRIVER

The TPD7100F is a 2ch High-side N-ch Power MOSFET Gate Driver. This IC contains a power MOSFET driver and power MOSFET protective and diagnostic functions, allowing you to configure a high-side switch for large-current applications easily.



SSOP24-P-300-1.00B

Weight : 0.29 g (Typ.)

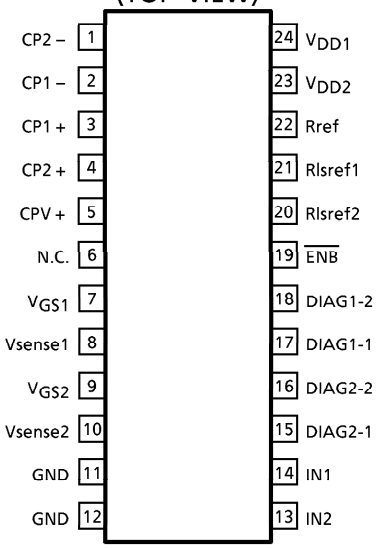
FEATURES

- The large-current charge pump allows for fast switching.
- Power MOSFET protective and diagnostic functions are built-in.
  Protective functions : Overvoltage (internal device protection), overcurrent protection, V_{DD} voltage drop detection
  * Overvoltage is internally limited. No detection or shutdown functions are included.
  Diagnostic functions : Overcurrent
- The level of Overcurrent detection can set by external resistor.
- Package : SSOP-24 (300 mil) with embossed-tape packing

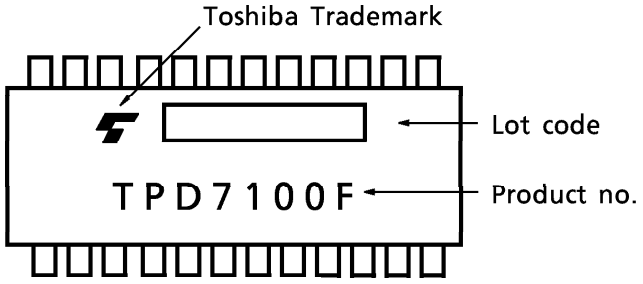
Because this product uses MOS structure, must take special care with electrostatic when handling.

PIN ASSIGNMENT

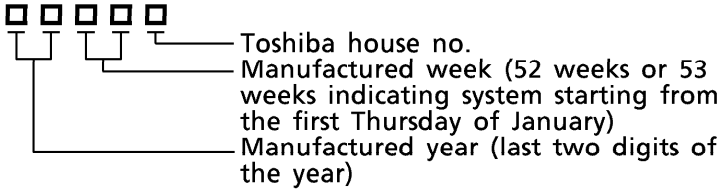
(TOP VIEW)



MARKING



Lot code naming system



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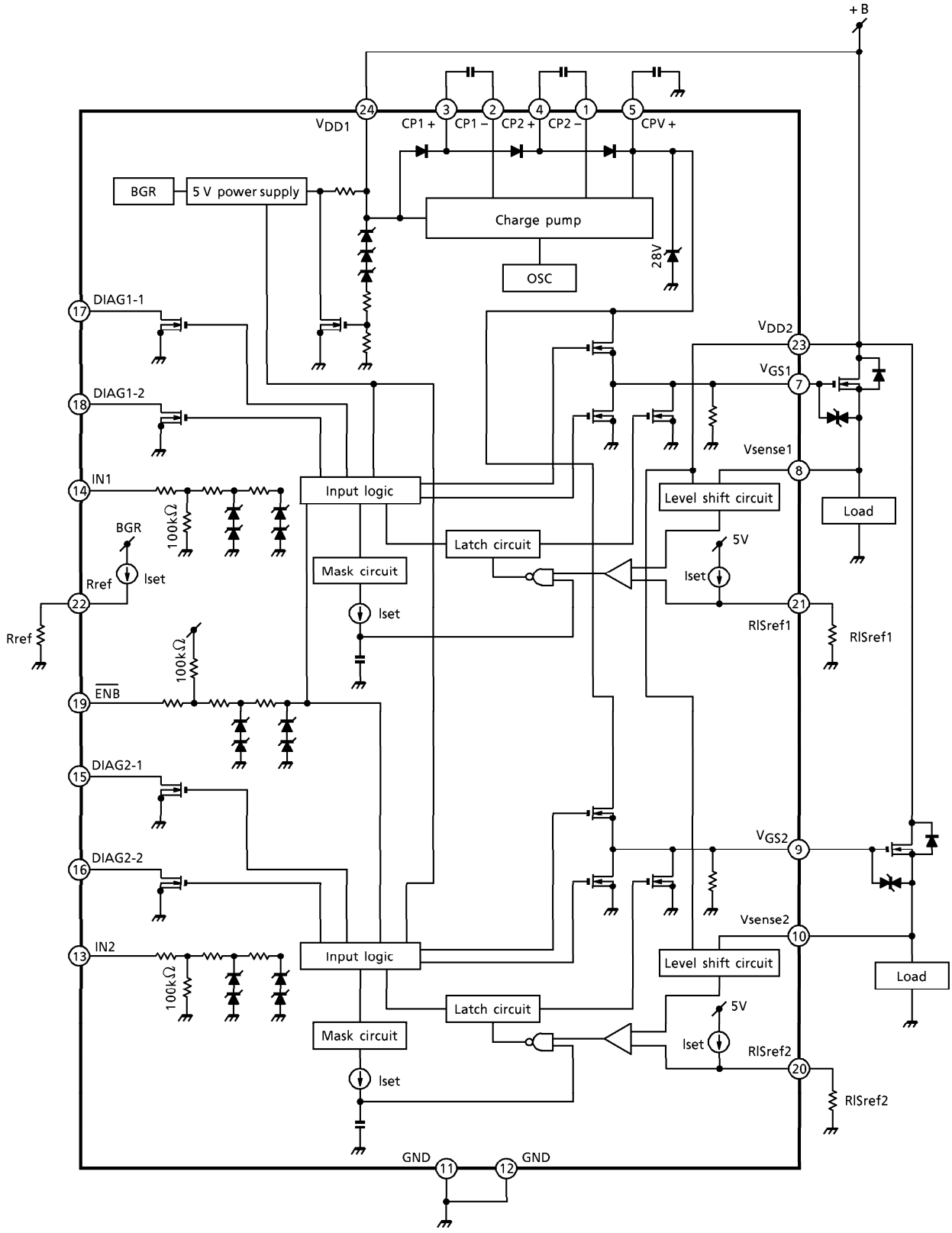
BLOCK DIAGRAM



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PIN DESCRIPTION

PIN NO.	SYMBOL	PIN DESCRIPTION
1	CP2 –	Negative side connecting pin for the charge pump's second capacitor.
2	CP1 –	Negative side connecting pin for the charge pump's first capacitor.
3	CP1 +	Positive side connecting pin for the charge pump's first capacitor.
4	CP2 +	Positive side connecting pin for the charge pump's second capacitor.
5	CPV +	Positive side connecting pin for the charge pump's third capacitor. Although about three times the V_{DD} voltage is generated, it is limited about 28 V by a voltage clamping circuit.
6	N.C.	—
7	V_{GS1}	External power MOSFET gate drive pin for ch1. This pin controls the external power MOSFET. Also, when overcurrent flows in the external power MOSFET, it shuts down the gate and is latched. It is unlatched by a low on input.
8	Vsense1	External power MOSFET monitor pin for ch1 : overcurrent is detected by comparing the difference between this and the V_{DD2} pin with the reference voltage.
9	V_{GS2}	External power MOSFET gate drive pin for ch2. This pin controls the external power MOSFET. Also, when overcurrent flows in the external power MOSFET, it shuts down the gate and is latched. It is unlatched by a low on input.
10	Vsense2	External power MOSFET monitor pin for ch2 : overcurrent is detected by comparing the difference between this and the V_{DD2} pin with the reference voltage.
11	GND	Ground pin : shared internally with pin 12.
12	GND	Shared internally with pin 11.
13	IN2	Input pin for ch2 (active high) : This pin has a pull-down resistor (100 kΩ typ.), so that even when it is open-circuited, output will not turn on inadvertently.
14	IN1	Input pin for ch1 (active high) : This pin has a pull-down resistor (100 kΩ typ.), so that even when it is open-circuited, output will not turn on inadvertently.
15	DIAG2-1	Diagnostic output pin for ch2 (N-ch open-drain) : when overcurrent condition is detected, its output goes low. Also, when overcurrent is detected, it remains latched until the next rising edge of input.
16	DIAG2-2	Diagnostic output pin for ch2 (N-ch open-drain) : by comparing the voltage between V_{DD2} and Vsense2 pins with the set overcurrent level, it outputs external power MOSFET on / off state.
17	DIAG1-1	Diagnostic output pin for ch1 (N-ch open-drain) : when overcurrent condition is detected, its output goes low. Also, when overcurrent is detected, it remains latched until the next rising edge of input.
18	DIAG1-2	Diagnostic output pin for ch1 (N-ch open-drain) : by comparing the voltage between V_{DD2} and Vsense1 pins with the set overcurrent level, it outputs external power MOSFET on / off state.
19	$\overline{ENB}$	Chip inhibit pin (active low) : By driving this pin high, all outputs can be turned off regardless of input signals. This pin has a pull-up resistor (100 kΩ typ.).

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PIN NO.	SYMBOL	PIN DESCRIPTION
20	RISref2	Overcurrent detection level setup pin for ch2 : the voltage determined by the constant current set by the resistor connected to the Rref pin and the resistance of an external resistor connected to the RISref2 pin is referenced to detect overcurrent.
21	RISref1	Overcurrent detection level setup pin for ch1 : the voltage determined by the constant current set by the resistor connected to the Rref pin and the resistance of an external resistor connected to the RISref1 pin is referenced to detect overcurrent.
22	Rref	Resistor connection pin ; This resistor determines the constant current used for the overcurrent detection circuit. Connect 62 kΩ (recommended) between this pin and GND.
23	V_{DD2}	External power MOSFET drain voltage detection pin.
24	V_{DD1}	Power supply pin : the internal device is protected when overvoltage is applied.

MAXIMUM RATING (Ta = 25°C)

CHARACTERISTICS	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	30	V
Input Voltage	V_{IN}	0.5~6	V
Diagnosis Output Current	IDIAG	2	mA
Power Dissipation	P_D	0.8	W
Operating Temperature	T_{opr}	−40~110	°C
Strage Temperature	T_{stg}	−55~150	°C

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ELECTRICAL CHARACTERISTICS (Unless otherwise specified : V_{DD} = 8~18 V, T_j = −40~110°C)

CHARACTERISTICS	RATING	PIN NO.	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	V_{DD}	V_{DD}	—	8	—	18	V
Supply Current	I_{DD}	V_{DD}	V_{DD} = 12 V, V_{IN} = 0 V, CP = 0.01 μF	—	—	10	mA
Input Voltage	V_{IN} (1)	IN1, IN2	V_{DD} = 12 V, V_{GS} = "H"	3.5	—	—	V
	V_{IN} (2)		V_{DD} = 12 V, V_{GS} = "L"	—	—	1.5	
Input Current	I_{IN} (1)	IN1, IN2	V_{DD} = 12 V, V_{IN} = 5 V	—	—	200	μA
	I_{IN} (2)		V_{DD} = 12 V, V_{IN} = 0 V	−1	—	1	
	$I_{\overline{ENB}}$ (1)	$\overline{ENB}$	V_{DD} = 12 V, $V_{\overline{ENB}}$ = 5 V	−45	—	—	
	$I_{\overline{ENB}}$ (2)		V_{DD} = 12 V, $V_{\overline{ENB}}$ = 0 V	−250	—	—	
Output Voltage	V_{OH}	V_{GS1} V_{GS2}	V_{DD} = 12 V, V_{IN} = 5 V	—	Vsense + 15*	Vsense + 19*	V
	V_{OL}		V_{DD} = 12 V, V_{IN} = 0 V	—	—	0.4	
Output Current	I_{OH}		V_{DD} = 12 V, V_{IN} = 5 V, CP = 0.01 μF	—	0.1	—	A
	I_{OL}		V_{DD} = 12 V, V_{IN} = 0 V, CP = 0.01 μF	—	0.1	—	
Overcurrent Detection Resistance Setup Range	RISref	RISref	—	10	20	40	kΩ
Constant Current Source Setup Pin Voltage	VRref	Rref	Rref = 62 kΩ	1.17	1.30	1.43	V
Overcurrent Detection Voltage	$V_{DS\ (ON)}$ (1)	V_{DD2} Vsense1 Vsense2	Rref = 62 kΩ, RISref = 10 kΩ	0.16	0.20	0.24	V
	$V_{DS\ (ON)}$ (2)		Rref = 62 kΩ, RISref = 20 kΩ	0.32	0.40	0.48	
	$V_{DS\ (ON)}$ (3)		Rref = 62 kΩ, RISref = 40 kΩ	0.64	0.80	0.96	
Diagnostic Output Current	I_{DH}	DIAG1 DIAG2	V_{DD} = 12 V, VDIAG = 5 V	—	—	10	μA
Diagnostic Output Voltage	V_{DL}		V_{DD} = 12 V, I_{DL} = 1 mA	—	—	0.6	V
Power Supply Drop Detection Voltage	VDDUV1 −	V_{DD}	—	6.3	6.7	7.3	V
Power Supply Drop Detection Reset Voltage	VDDUV1 +		—	6.6	7.2	7.8	
Undervoltage Protection	VDDUV2		—	—	—	4.5	
Switching Time	t_{ON}	V_{GS1} V_{GS2}	V_{DD} = 12V, C = 3000 pF	—	2	5	μs
	t_{OFF}			—	2	5	

* : Vsense denotes the Vsense pin voltage.

Equation to calculate overcurrent detection resistance (RISref)

$$RISref = Rref \times R_{DS\ (ON)} \times I_D / VRref$$
$$= Rref \times V_{DS\ (ON)} / VRref$$

where $R_{DS\ (ON)}$: ON-resistance of external power MOSFET
I_D : drain current of external power MOSFET
$V_{DS\ (ON)}$: ON-voltage of external power MOSFET
Rref : external resistor connected to Rref pin (used to set constant current)
VRref : Rref pin voltage

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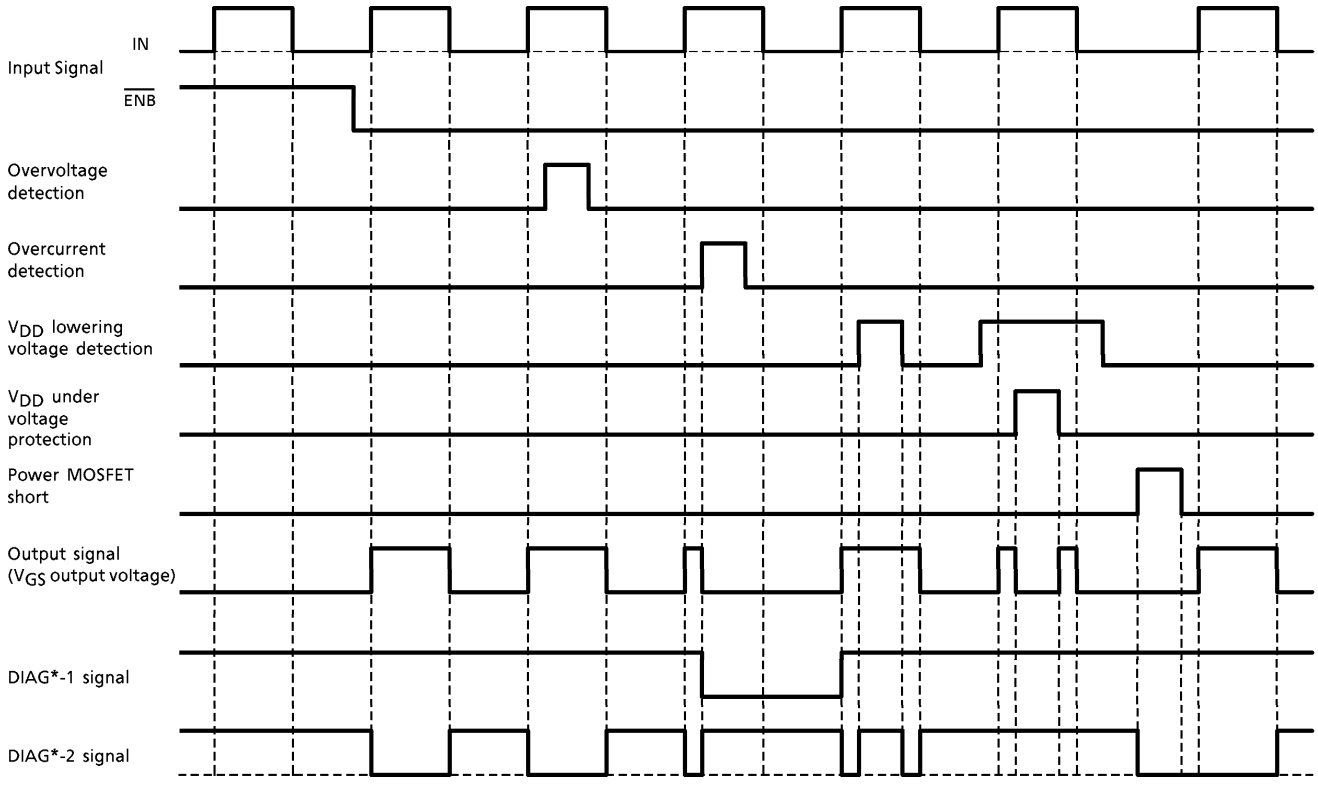
TRUTH TABLE

IN	$\overline{ENB}$	V_{GS}	DIAG*-1	DIAG*-2	MODE
L	H	L	H	H	When normal
H	H	L	H	H	
L	L	L	H	H	
H	L	H	H (Note 1)	L	
L	L	L	H	H	For overvoltage
H	L	H	H (Note 1)	L	
L	L	L	L (Note 1 / Note 2)	H	For overcurrent
H	L	L	L (Note 1)	H	
L	L	L	H	H	When supply voltage drop detected
H	L	H	H	H	
L	L	L	H	H	Undervoltage protection
H	L	L	H	H	
L	L	L	H	L	When power MOSFET shorted
H	L	H	H	L	

(Note 1) : Because overcurrent is detected by checking the drain-to-source voltage of the power MOSFET, there is a possibility of detecting overcurrent erratically for a while after input is driven high before the power MOSFET turns on, during which the drain-to-source voltage is high. To prevent this erroneous detection, DIAG detection is disabled for 15 μs (typ.) by a mask circuit. This masking time depends on the constant current determined by the internal capacitor and Rref. (The masking time is 15 μs when Rref = 62 kΩ.)

(Note 2) : After overcurrent is detected, DIAG remains latched until the next rising edge of input.

TIMIMG CHART



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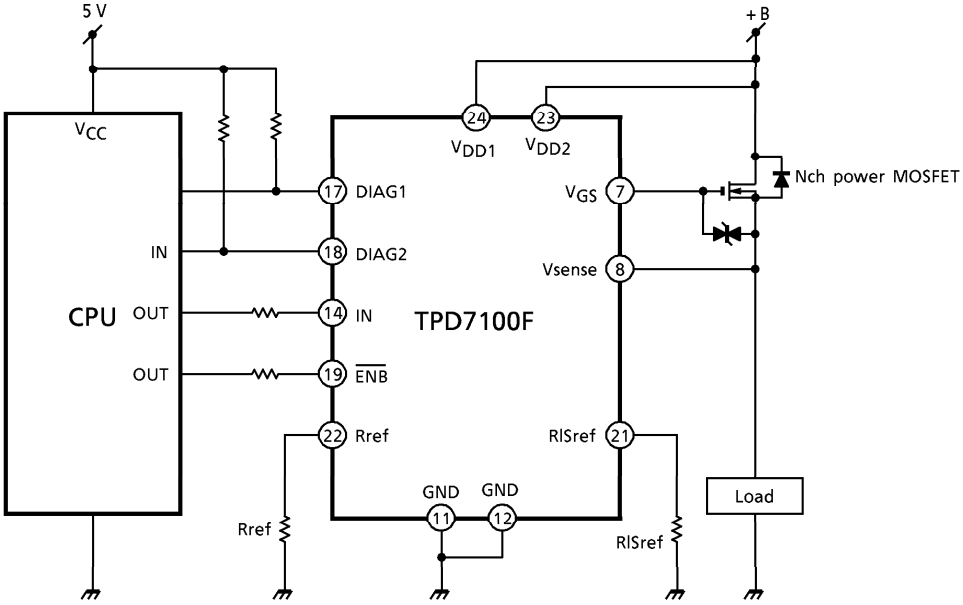
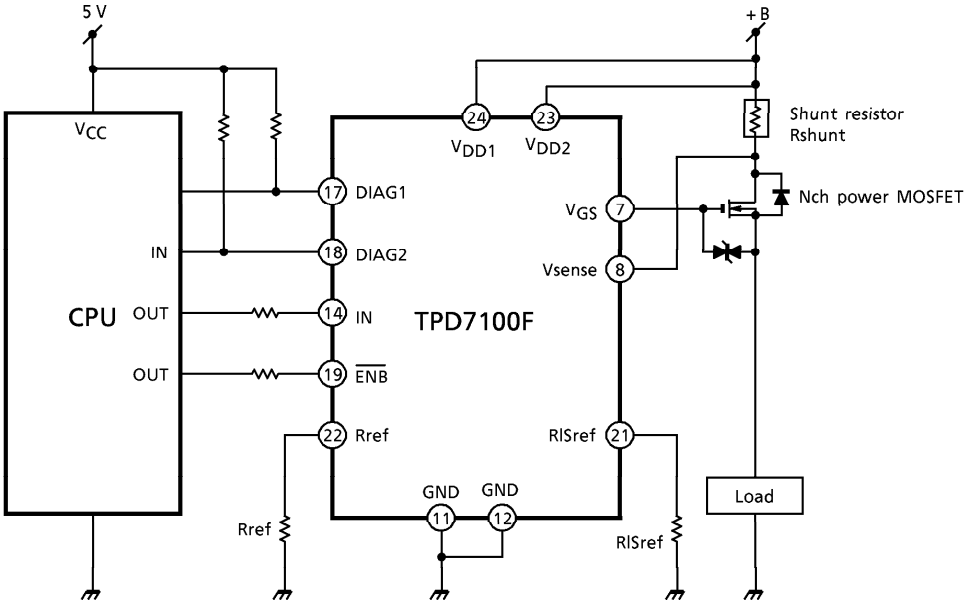
APPLICATION CIRCUIT 1

Monitoring Power MOSFET drain-soure voltage



APPLICATION CIRCUIT 2

Monitoring voltage between shunt resistors (for detecting overcurrent with high accuracy)



MOISTURE-PROOF PACKING

After the pack is opened, use the devices in a 30°C, 60% RH environment, and within the 48 hours. Embossed-tape packing cannot be baked. Devices so packed must be within their allowable time limits after unpacking, as specified on the packing.

Tape packing quantity: 500 devices / reel (EL) or 2000 devices / reel (EL1)

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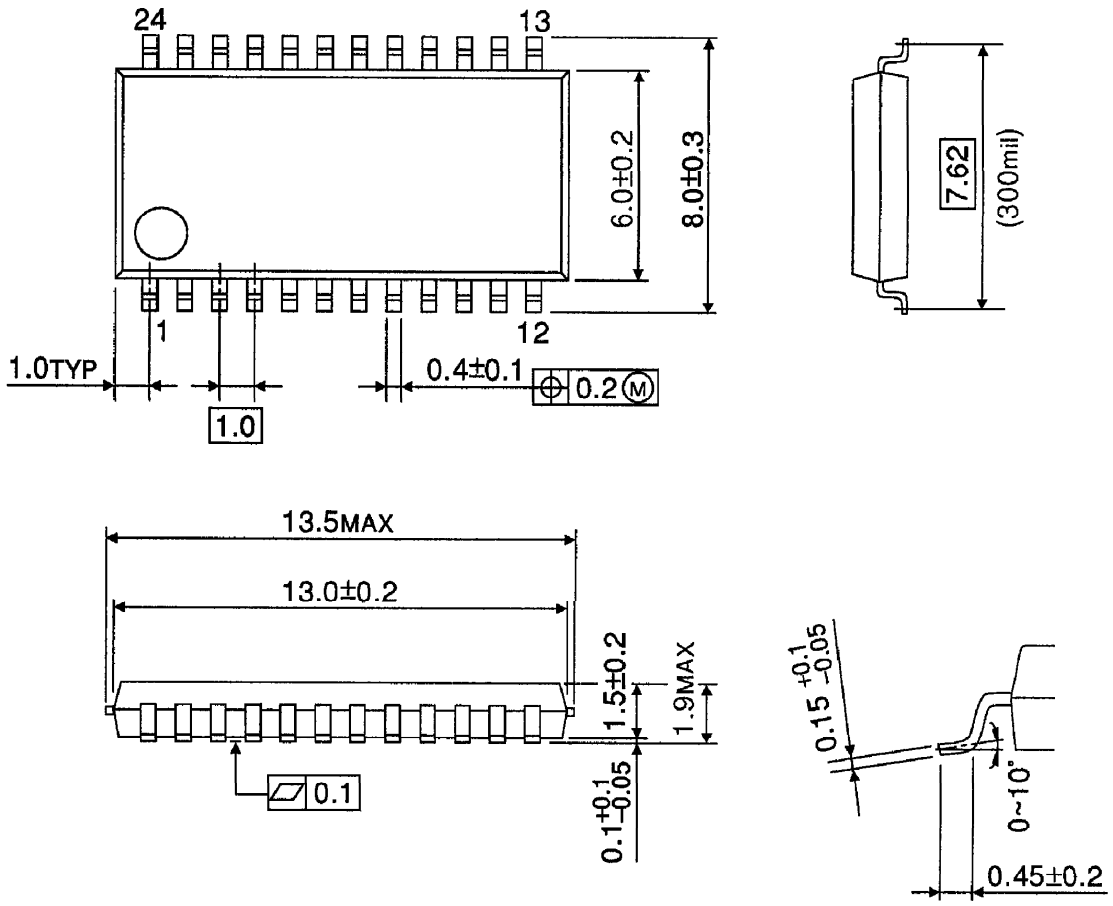
PACKAGE DIMENSIONS

SSOP24-P-300-1.00B Unit : mm



Weight : 0.29 g (Typ.)