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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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# HD404889/HD404899/HD404878/ HD404868 Series

Low-Voltage AS Microcomputers with On-Chip LCD Circuit



ADE-202-075D (O)  
Rev. 5.0  
Feb. 2000

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## Description

The HD404889, HD404899, and HD404868 Series comprise low-voltage, 4-bit single-chip microcomputers with a variety of on-chip supporting functions that include an LCD circuit, A/D converter, multifunctional timers, and large-current I/O pins. These devices are suitable for system and display panel control in a wide range of applications, including pagers, remote controllers, and home appliances equipped with an LCD display.

The HD404878 Series comprises low-voltage, 4-bit single-chip microcomputers with no on-chip A/D converter.

Each series is equipped with a 32.768 kHz sub-resonator for realtime clock use, providing a time counting facility, and a variety of low-power modes to reduce current drain.

The HD4074889, HD4074899, and HD4074869 are ZTAT™ microcomputers with on-chip PROM that drastically shortens development time and ensures a smooth transition from debugging to mass production. (The PROM programming specifications are the same as for the 27256 type.)

ZTAT™: Zero Turn-Around Time. ZTAT™ is a trademark of Hitachi, Ltd.

## Features

- 46 I/O pins (HD404889/HD404899/HD404878 Series)  
41 I/O pins (HD404868 Series)  
Large-current I/O pins (source: 10 mA max.):4  
Large-current I/O pins (sink: 15 mA max.): 8 (HD404889/HD404899/HD404878 Series)  
6 (HD404868 Series)  
LCD segment multiplexed pins:16  
Analog input multiplexed pins: 6 (HD404889 and HD404899 Series)  
4 (HD404868 Series)

- Four Timer/counters  
8-bit timer: 2 (HD404889/HD404899/HD404878 Series)  
1 (HD404868 Series)  
16-bit timer:1 (Can also be used as two 8-bit timer)
- 8-bit input capture circuit (HD404889/HD404899/HD404878 Series)
- Two timer outputs (including PWM out-put)
- Two event counter inputs (edge-programmable) (HD404889/HD404899/HD404878 Series)  
One event counter input (edge-programmable) (HD404868 Series)
- Clock-synchronous 8-bit serial interface
- A/D converter  
6 channels  $\times$  8-bit (HD404889 Series)  
6 channels  $\times$  10-bit (HD404899 Series)  
4 channels  $\times$  10-bit (HD404868 Series)
- LCD controller/driver (32 segments  $\times$  4 commons) (HD404889/HD404899/HD404878 Series)  
(24 segments  $\times$  4 commons) (HD404868 Series)
- On-chip oscillators  
— Main clock (ceramic resonator, crystal resonator, or external clock operation possible)  
— Sub-clock (32.768 kHz crystal resonator)
- Interrupts  
External: 3 (including one edge-programmable)  
Internal : 6 (HD404889 and HD404899 Series)  
: 5 (HD404878 and HD404868 Series)
- Subroutine stack up to 16 levels, including interrupts
- Four Low-power dissipation modes
- Module standby (timers, serial interface, A/D converter)
- System clock division software switching (1/4 or 1/32)
- Inputs for return from stop mode (wake-up): 4
- Instruction execution time  
Min. 0.89  $\mu$ s ( $f_{osc} = 4.5$  MHz)
- Operation voltage  
1.8 V to 5.5 V

### Cautions about operation!

- Electrical properties presented on the data sheet for the mask ROM and ZTAT<sup>TM</sup> versions will surely and sufficiently satisfy the standard values. However, real capabilities, operation margin, noise margin, and other properties may vary depending on differences of manufacturing processes, internal wiring patterns, etc. Therefore, it is requested for users to carry out an evaluation test for each product on an actual system under the same conditions to see its operation.
- Memory register, data area, and stack area values are unstable immediately after power is turned on. They must be initialized before use.

Ordering Information

HD404889 Series

| Type     | Product Name | Model Name  | ROM (Words) | RAM (Digits) | Package                         |
|----------|--------------|-------------|-------------|--------------|---------------------------------|
| Mask ROM | HD404888     | HD404888H   | 8,192       | 1,344        | 80-pin plastic QFP (FP-80A)     |
|          |              | HD404888TE  |             |              | 80-pin plastic TQFP (TFP-80C)   |
|          | HD4048812    | HD4048812H  | 12,288      |              | 80-pin plastic QFP (FP-80A)     |
|          |              | HD4048812TE |             |              | 80-pin plastic TQFP (TFP-80C)   |
|          | HD404889     | HD404889H   | 16,384      |              | 80-pin plastic QFP (FP-80A)     |
|          |              | HD404889TE  |             |              | 80-pin plastic TQFP (TFP-80C)   |
| ZTAT™    | HCD404889    | HCD404889   |             |              | Chip*2                          |
|          | HD4074889    | HD4074889H  | 16,384      |              | 80-pin plastic QFP*1 (FP-80A)   |
|          |              | HD4074889TE |             |              | 80-pin plastic TQFP*1 (TFP-80C) |

- Notes: 1. ZTAT™ chip shipment is not supported.
2. The specifications of shipped chips differ from those of the package product. Please contact our sales staff for details.

**HD404889/HD404899/HD404878/HD404868 Series**

**HD404899 Series**

| Type     | Product Name | Model Name  | ROM (Words) | RAM (Digits) | Package                         |
|----------|--------------|-------------|-------------|--------------|---------------------------------|
| Mask ROM | HD404898     | HD404898H   | 8,192       | 1,344        | 80-pin plastic QFP (FP-80A)     |
|          |              | HD404898TE  |             |              | 80-pin plastic TQFP (TFP-80C)   |
|          | HD4048912    | HD4048912H  | 12,288      |              | 80-pin plastic QFP (FP-80A)     |
|          |              | HD4048912TE |             |              | 80-pin plastic TQFP (TFP-80C)   |
|          | HD404899     | HD404899H   | 16,384      |              | 80-pin plastic QFP (FP-80A)     |
|          |              | HD404899TE  |             |              | 80-pin plastic TQFP (TFP-80C)   |
| ZTAT™    | HCD404899    | HCD404899   |             |              | Chip*2                          |
|          | HD4074899    | HD4074899H  | 16,384      |              | 80-pin plastic QFP*1 (FP-80A)   |
|          |              | HD4074899TE |             |              | 80-pin plastic TQFP*1 (TFP-80C) |

Notes: 1. ZTAT™ chip shipment is not supported.  
2. The specifications of shipped chips differ from those of the package product. Please contact our sales staff for details. In planning stage.

**HD404878 Series**

| Type     | Product Name                      | Model Name | ROM (Words) | RAM (Digits) | Package                       |
|----------|-----------------------------------|------------|-------------|--------------|-------------------------------|
| Mask ROM | HD404874                          | HD404874H  | 4,096       | 880          | 80-pin plastic QFP (FP-80A)   |
|          |                                   | HD404874TE |             |              | 80-pin plastic TQFP (TFP-80C) |
|          | HD404878                          | HD404878H  | 8,192       |              | 80-pin plastic QFP (FP-80A)   |
|          |                                   | HD404878TE |             |              | 80-pin plastic TQFP (TFP-80C) |
|          | HCD404878                         | HCD404878  |             |              | Chip*2                        |
| ZTAT™    | HD4074889 or HD4074899 is used.*1 |            |             |              |                               |

Notes: 1. ZTAT™ chip shipment is not supported.  
2. The specifications of shipped chips differ from those of the package product. Please contact our sales staff for details. In planning stage.

HD404889/HD404899/HD404878/HD404868 Series

HD404868 Series

| Type     | Product Name | Model Name | ROM (Words) | RAM (Digits) | Package                      |
|----------|--------------|------------|-------------|--------------|------------------------------|
| Mask ROM | HD404864     | HD404864H  | 4,096       | 408          | 64-pin plastic QFP (FP-64A)  |
|          |              | HD404864S  |             |              | 64-pin plastic DILP (DP-64S) |
|          | HD404868     | HD404868H  | 8,192       |              | 64-pin plastic QFP (FP-64A)  |
|          |              | HD404868S  |             |              | 64-pin plastic DILP (DP-64S) |
|          | HCD404868    | HCD404868  |             |              | Chip*1                       |
| ZTAT™    | HD4074869    | HD4074869H | 16,384      |              | 64-pin plastic QFP (FP-64A)  |
|          |              | HD4074869S |             |              | 64-pin plastic DILP (DP-64S) |

Note: 1. In planning stage

# HD404889/HD404899/HD404878/HD404868 Series

## List of Functions

| Product Name                             |                               | HD404888                                                                 | HD4048812                        | HD404889 | HCD404889 |
|------------------------------------------|-------------------------------|--------------------------------------------------------------------------|----------------------------------|----------|-----------|
| ROM (words)                              |                               | 8,192                                                                    | 12,288                           | 16,384   |           |
| RAM (digit)                              |                               |                                                                          | 1,344                            |          |           |
| I/O                                      |                               |                                                                          | 46 (max)                         |          |           |
|                                          | Large-current I/O pins        | 4 (source, 10 mA max), 8 (sink, 15 mA max)                               |                                  |          |           |
|                                          | LCD segment multiplexed pins  |                                                                          | 16                               |          |           |
|                                          | Analog input multiplexed pins |                                                                          | 6                                |          |           |
| Timer/counter                            |                               | 16-bit timer: 1 (Can also be used as two 8-bit timer),<br>8-bit timer: 2 |                                  |          |           |
|                                          | Input capture                 |                                                                          | 8 bit × 1                        |          |           |
|                                          | Timer output                  |                                                                          | 2 (PWM output possible)          |          |           |
|                                          | Event input                   |                                                                          | 2 (edge selection possible)      |          |           |
| Serial interface                         |                               |                                                                          | 1 (8-bit synchronous)            |          |           |
| A/D converter                            |                               |                                                                          | 8 bits × 6 channels              |          |           |
| LCD circuit                              |                               |                                                                          | Max. 32 seg × 4 com              |          |           |
| Interrupt sources                        | External                      | 3 (edge selection possible for 1)                                        |                                  |          |           |
|                                          | Internal                      |                                                                          | 6                                |          |           |
| Low-power modes                          |                               |                                                                          | 4                                |          |           |
|                                          | Stop mode                     |                                                                          | O                                |          |           |
|                                          | Watch mode                    |                                                                          | O                                |          |           |
|                                          | Standby mode                  |                                                                          | O                                |          |           |
|                                          | Subactive mode                |                                                                          | O                                |          |           |
| Module standby                           |                               |                                                                          | O                                |          |           |
| System clock division software switching |                               |                                                                          | O                                |          |           |
| Main oscillator                          | Ceramic oscillation           |                                                                          | O                                |          |           |
|                                          | Crystal oscillation           |                                                                          | O                                |          |           |
| Sub-oscillator                           | Crystal oscillation           |                                                                          | O (32.768kHz)                    |          |           |
| Minimum instruction execution time       |                               |                                                                          | 0.89μs(f <sub>osc</sub> =4.5MHz) |          |           |
| Operating voltage (V)                    |                               |                                                                          | 1.8 to 5.5                       |          |           |
| Package                                  |                               | 80-pin plastic QFP (FP-80A)<br>80-pin plastic TQFP (TFP-80C)             |                                  |          | Chip      |
| Guaranteed operation temperature(°C)     |                               |                                                                          | −20 to +75                       |          | +75       |

# HD404889/HD404899/HD404878/HD404868 Series

| Product Name                             |                               | HD4074889                                                                | HD404898             | HD4048912                     | HD404899 |
|------------------------------------------|-------------------------------|--------------------------------------------------------------------------|----------------------|-------------------------------|----------|
| ROM (words)                              |                               | 16,384PROM                                                               | 8,192                | 12,288                        | 16,384   |
| RAM (digit)                              |                               |                                                                          | 1,344                |                               |          |
| I/O                                      |                               |                                                                          | 46 (max)             |                               |          |
|                                          | Large-current I/O pins        | 4 (source, 10 mA max), 8 (sink, 15 mA max)                               |                      |                               |          |
|                                          | LCD segment multiplexed pins  | 16                                                                       |                      |                               |          |
|                                          | Analog input multiplexed pins | 6                                                                        |                      |                               |          |
| Timer/counter                            |                               | 16-bit timer: 1 (Can also be used as two 8-bit timer),<br>8-bit timer: 2 |                      |                               |          |
|                                          | Input capture                 | 8 bit × 1                                                                |                      |                               |          |
|                                          | Timer output                  | 2 (PWM output possible)                                                  |                      |                               |          |
|                                          | Event input                   | 2 (edge selection possible)                                              |                      |                               |          |
| Serial interface                         |                               | 1 (8-bit synchronous)                                                    |                      |                               |          |
| A/D converter                            |                               | 8 bits × 6 channels                                                      | 10 bits × 6 channels |                               |          |
| LCD circuit                              |                               | Max. 32 seg × 4 com                                                      |                      |                               |          |
| Interrupt sources                        | External                      | 3 (edge selection possible for 1)                                        |                      |                               |          |
|                                          | Internal                      | 6                                                                        |                      |                               |          |
| Low-power modes                          |                               | 4                                                                        |                      |                               |          |
|                                          | Stop mode                     | O                                                                        |                      |                               |          |
|                                          | Watch mode                    | O                                                                        |                      |                               |          |
|                                          | Standby mode                  | O                                                                        |                      |                               |          |
|                                          | Subactive mode                | O                                                                        |                      |                               |          |
| Module standby                           |                               | O                                                                        |                      |                               |          |
| System clock division software switching |                               | O                                                                        |                      |                               |          |
| Main oscillator                          | Ceramic oscillation           | O                                                                        |                      |                               |          |
|                                          | Crystal oscillation           | O                                                                        |                      |                               |          |
| Sub-oscillator                           | Crystal oscillation           | O (32.768kHz)                                                            |                      |                               |          |
| Minimum instruction execution time       |                               | 0.89μs(f <sub>osc</sub> =4.5MHz)                                         |                      |                               |          |
| Operating voltage (V)                    |                               | 2.0 to 5.5                                                               | 1.8 to 5.5           |                               |          |
| Package                                  |                               | 80-pin plastic QFP (FP-80A)                                              |                      | 80-pin plastic TQFP (TFP-80C) |          |
| Guaranteed operation temperature(°C)     |                               | −20 to +75                                                               |                      |                               |          |

## HD404889/HD404899/HD404878/HD404868 Series

| Product Name                             |                                                                   | HD40C4899                                                                | HD4074899                                                    | HD404874   | HD404878 |
|------------------------------------------|-------------------------------------------------------------------|--------------------------------------------------------------------------|--------------------------------------------------------------|------------|----------|
| ROM (words)                              |                                                                   | 16,384                                                                   | 16,384PROM                                                   | 4,096      | 8,192    |
| RAM (digit)                              |                                                                   | 1,344                                                                    |                                                              | 880        |          |
| I/O                                      | 46 (max)                                                          |                                                                          |                                                              |            |          |
|                                          | Large-current I/O pins 4 (source, 10 mA max), 8 (sink, 15 mA max) |                                                                          |                                                              |            |          |
|                                          | LCD segment multiplexed pins 16                                   |                                                                          |                                                              |            |          |
|                                          | Analog input multiplexed pins 6 —                                 |                                                                          |                                                              |            |          |
| Timer/counter                            |                                                                   | 16-bit timer: 1 (Can also be used as two 8-bit timer),<br>8-bit timer: 2 |                                                              |            |          |
|                                          |                                                                   | Input capture 8 bit × 1                                                  |                                                              |            |          |
|                                          |                                                                   | Timer output 2 (PWM output possible)                                     |                                                              |            |          |
|                                          |                                                                   | Event input 2 (edge selection possible)                                  |                                                              |            |          |
| Serial interface                         |                                                                   | 1 (8-bit synchronous)                                                    |                                                              |            |          |
| A/D converter                            |                                                                   | 10 bits × 6 channels                                                     |                                                              | —          |          |
| LCD circuit                              |                                                                   | Max. 32 seg × 4 com                                                      |                                                              |            |          |
| Interrupt sources                        | External                                                          | 3 (edge selection possible for 1)                                        |                                                              |            |          |
|                                          | Internal                                                          | 6                                                                        |                                                              | 5          |          |
| Low-power modes                          |                                                                   | 4                                                                        |                                                              |            |          |
|                                          |                                                                   | Stop mode O                                                              |                                                              |            |          |
|                                          |                                                                   | Watch mode O                                                             |                                                              |            |          |
|                                          |                                                                   | Standby mode O                                                           |                                                              |            |          |
|                                          |                                                                   | Subactive mode O                                                         |                                                              |            |          |
| Module standby                           |                                                                   | O                                                                        |                                                              |            |          |
| System clock division software switching |                                                                   | O                                                                        |                                                              |            |          |
| Main oscillator                          | Ceramic oscillation                                               |                                                                          | O                                                            |            |          |
|                                          | Crystal oscillation                                               |                                                                          | O                                                            |            |          |
| Sub-oscillator                           | Crystal oscillation                                               |                                                                          | O (32.768kHz)                                                |            |          |
| Minimum instruction execution time       |                                                                   | 0.89μs(f <sub>osc</sub> =4.5MHz)                                         |                                                              |            |          |
| Operating voltage (V)                    |                                                                   | 1.8 to 5.5                                                               | 2.0 to 5.5                                                   | 1.8 to 5.5 |          |
| Package                                  |                                                                   | Chip                                                                     | 80-pin plastic QFP (FP-80A)<br>80-pin plastic TQFP (TFP-80C) |            |          |
| Guaranteed operation temperature(°C)     |                                                                   | +75                                                                      |                                                              | −20 to +75 |          |

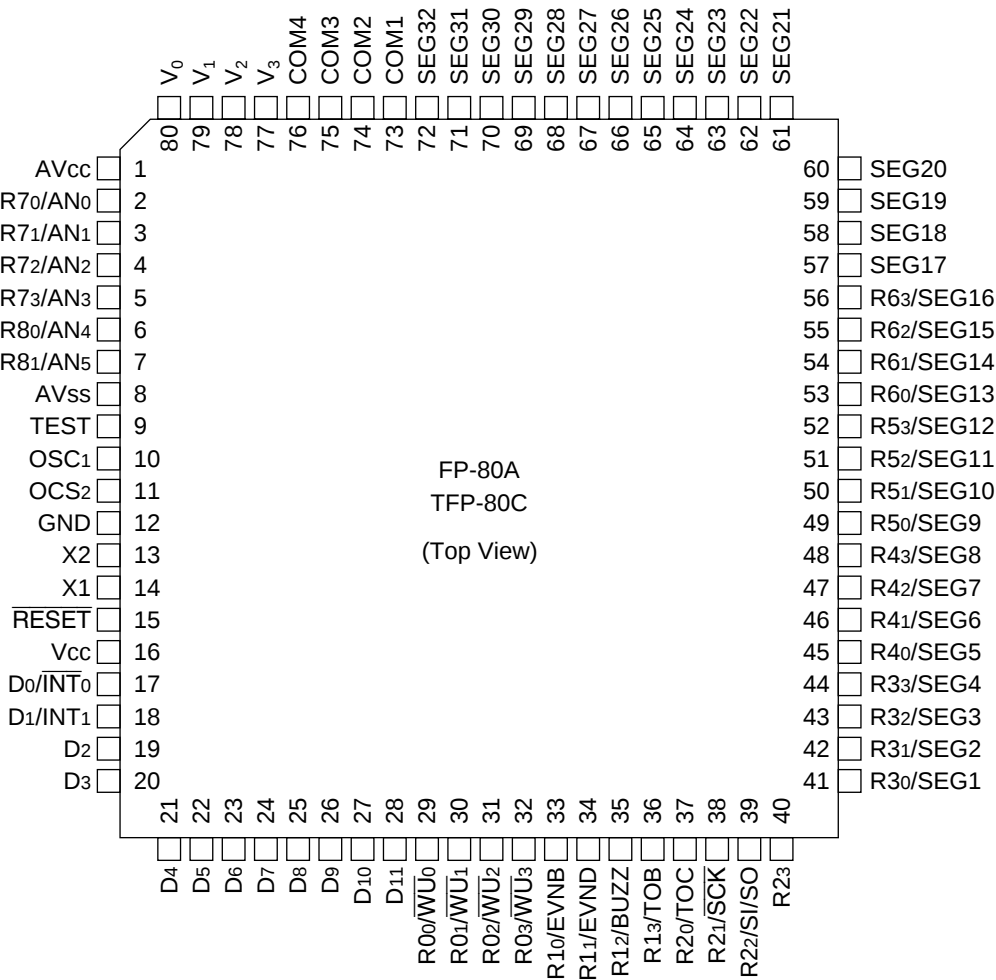
# HD404889/HD404899/HD404878/HD404868 Series

| Product Name                             |                               | HCD404878                                                                   | HD404864                                                              | HD404868 | HD4074869  |
|------------------------------------------|-------------------------------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------|----------|------------|
| ROM (words)                              |                               | 8,192                                                                       | 4,096                                                                 | 8,192    | 16,384PROM |
| RAM (digit)                              |                               | 880                                                                         | 408                                                                   |          |            |
| I/O                                      |                               | 46 (max)                                                                    | 41 (max)                                                              |          |            |
|                                          | Large-current I/O pins        | 4 (source, 10 mA max),<br>8 (sink, 15 mA max)                               | 4 (source, 10 mA max), 6 (sink, 15 mA max)                            |          |            |
|                                          | LCD segment multiplexed pins  |                                                                             | 16                                                                    |          |            |
|                                          | Analog input multiplexed pins | —                                                                           | 4                                                                     |          |            |
| Timer/counter                            |                               | 16-bit timer: 1<br>(Can also be used as two 8-bit timer),<br>8-bit timer: 2 | 16-bit timer: 1 (Can also be used as two 8-bit timer), 8-bit timer: 1 |          |            |
|                                          | Input capture                 | 8 bit × 1                                                                   | —                                                                     |          |            |
|                                          | Timer output                  |                                                                             | 2 (PWM output possible)                                               |          |            |
|                                          | Event input                   | 2 (edge selection possible)                                                 | 1 (edge selection possible)                                           |          |            |
| Serial interface                         |                               |                                                                             | 1 (8-bit synchronous)                                                 |          |            |
| A/D converter                            |                               | —                                                                           | 10 bits × 4 channels                                                  |          |            |
| LCD circuit                              |                               | Max. 32 seg × 4 com                                                         | Max. 24 seg × 4 com                                                   |          |            |
| Interrupt sources                        | External                      |                                                                             | 3 (edge selection possible for 1)                                     |          |            |
|                                          | Internal                      |                                                                             | 5                                                                     |          |            |
| Low-power modes                          |                               |                                                                             | 4                                                                     |          |            |
|                                          | Stop mode                     |                                                                             | O                                                                     |          |            |
|                                          | Watch mode                    |                                                                             | O                                                                     |          |            |
|                                          | Standby mode                  |                                                                             | O                                                                     |          |            |
|                                          | Subactive mode                |                                                                             | O                                                                     |          |            |
| Module standby                           |                               |                                                                             | O                                                                     |          |            |
| System clock division software switching |                               |                                                                             | O                                                                     |          |            |
| Main oscillator                          | Ceramic oscillation           |                                                                             | O                                                                     |          |            |
|                                          | Crystal oscillation           |                                                                             | O                                                                     |          |            |
| Sub-oscillator                           | Crystal oscillation           |                                                                             | O (32.768kHz)                                                         |          |            |
| Minimum instruction execution time       |                               |                                                                             | 0.89μs(f <sub>osc</sub> =4.5MHz)                                      |          |            |
| Operating voltage (V)                    |                               | 1.8 to 5.5                                                                  |                                                                       |          | 2.0 to 5.5 |
| Package                                  |                               | Chip                                                                        | 64-pin plastic QFP (FP-64A)<br>64-pin plastic DILP (DP-64S)           |          |            |
| Guaranteed operation temperature(°C)     |                               | +75                                                                         | −20 to +75                                                            |          |            |

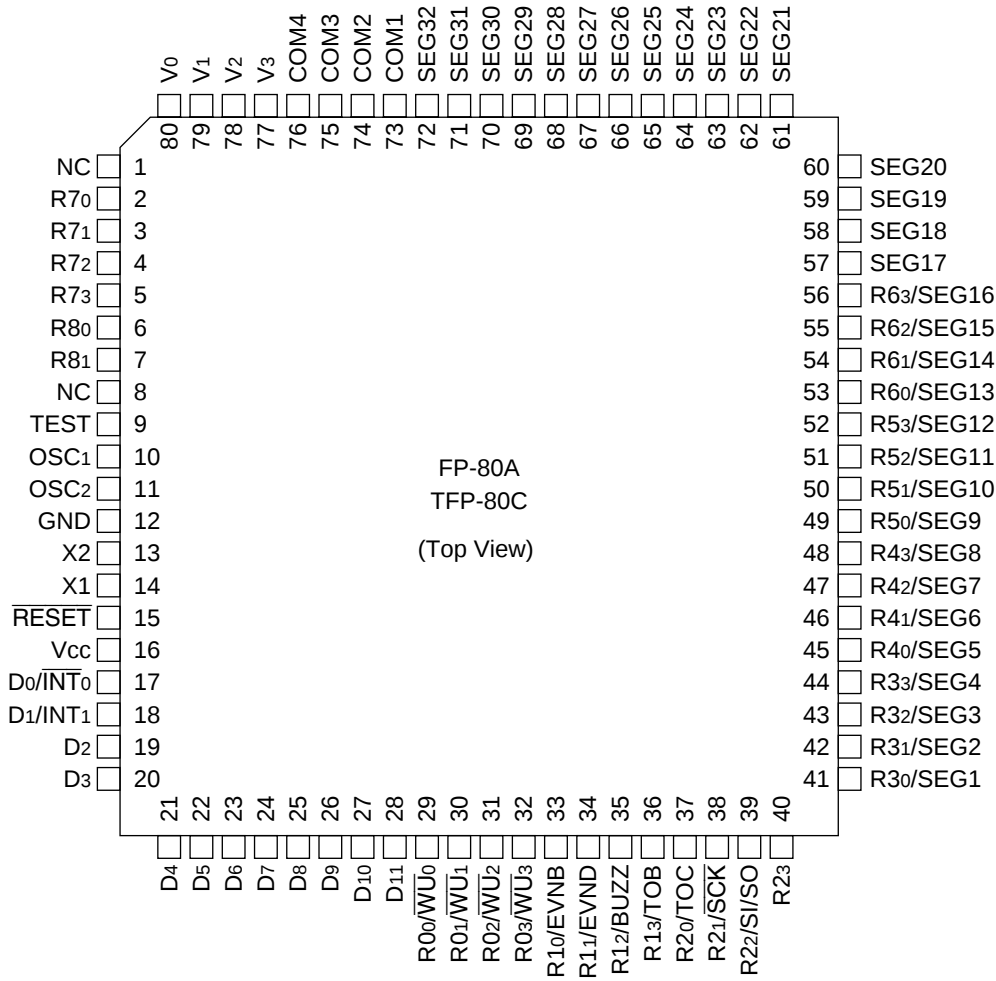
HD404889/HD404899/HD404878/HD404868 Series

Pin Arrangement

HD404889/HD404899 Series

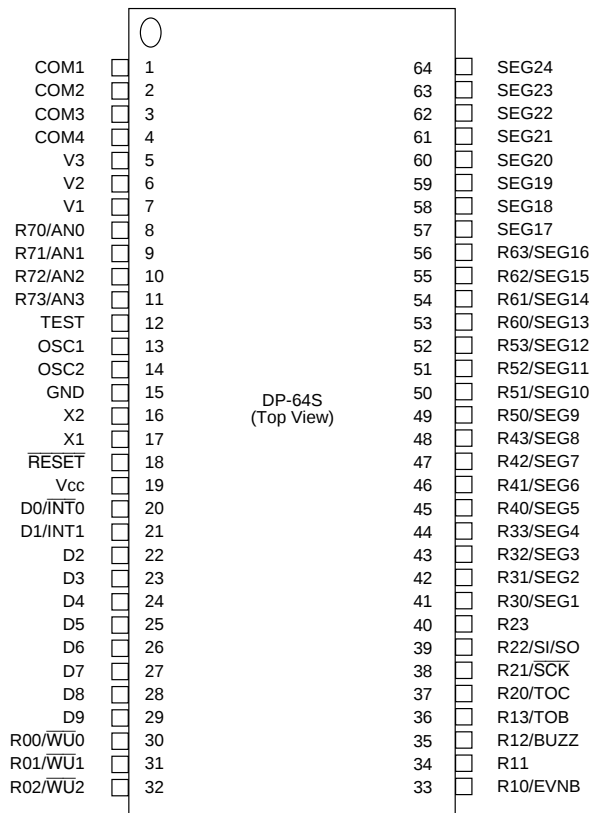
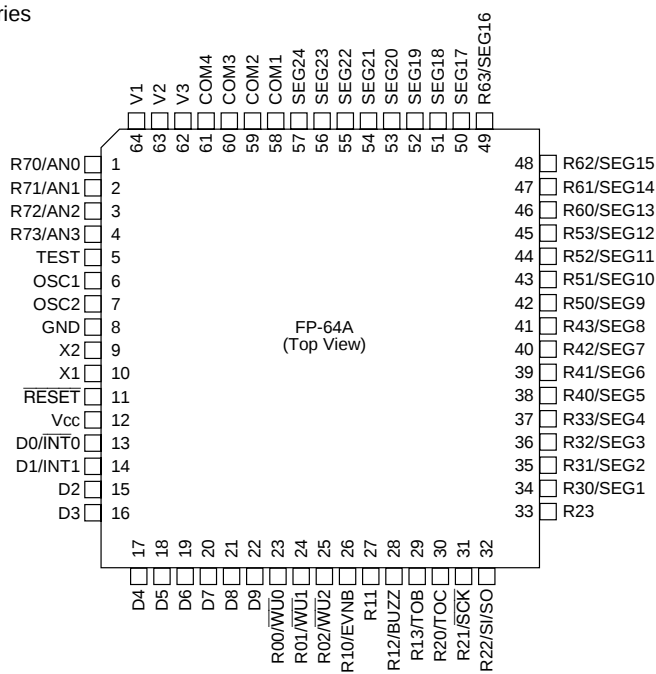


HD404878 Series



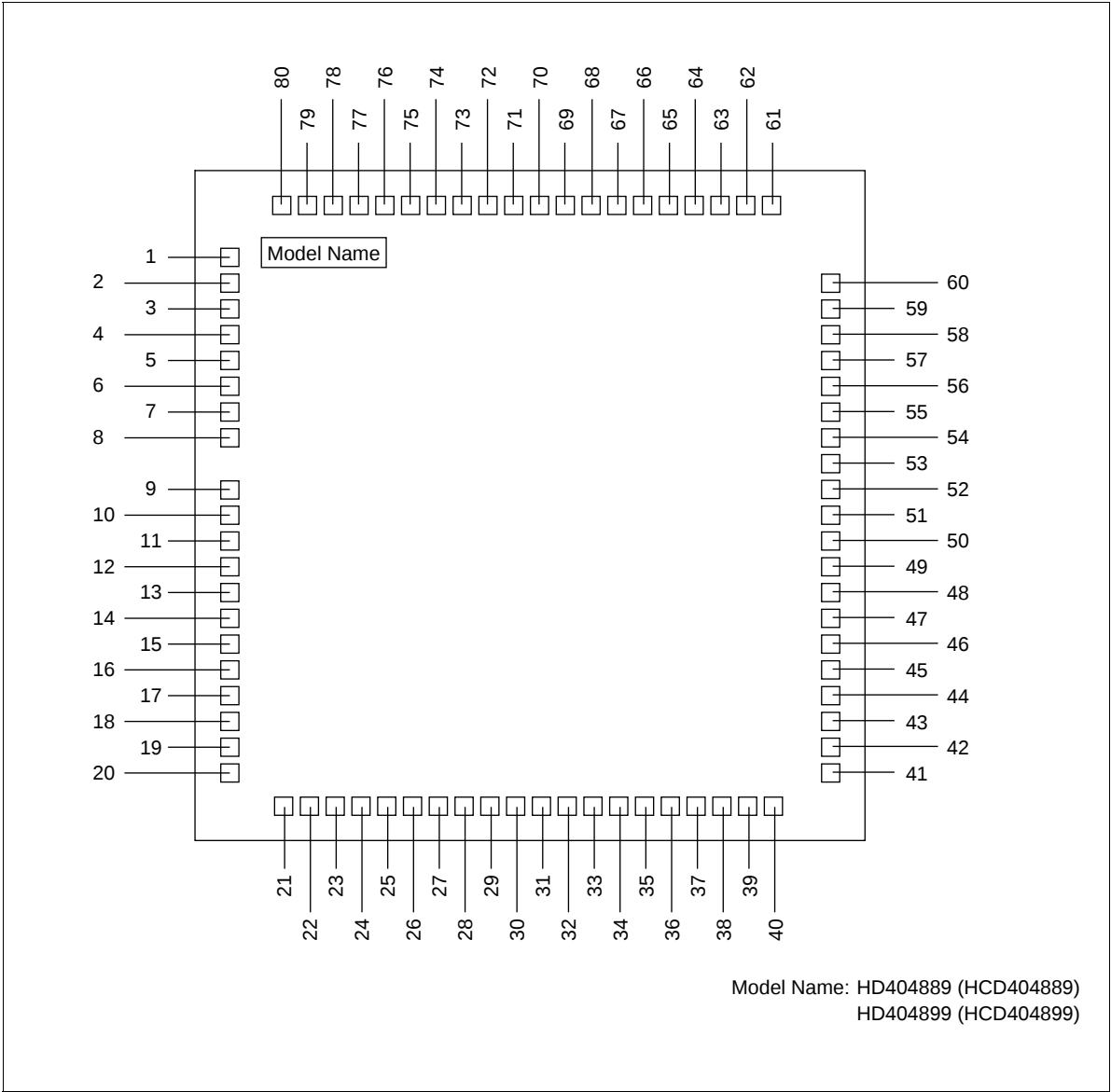
HD404889/HD404899/HD404878/HD404868 Series

HD404868 Series



Pad Arrangement

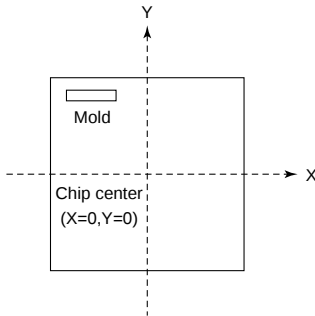
HCD404889, HCD404899



# HD404889/HD404899/HD404878/HD404868 Series

## Pad Coordinates

HCD404889, HCD404899

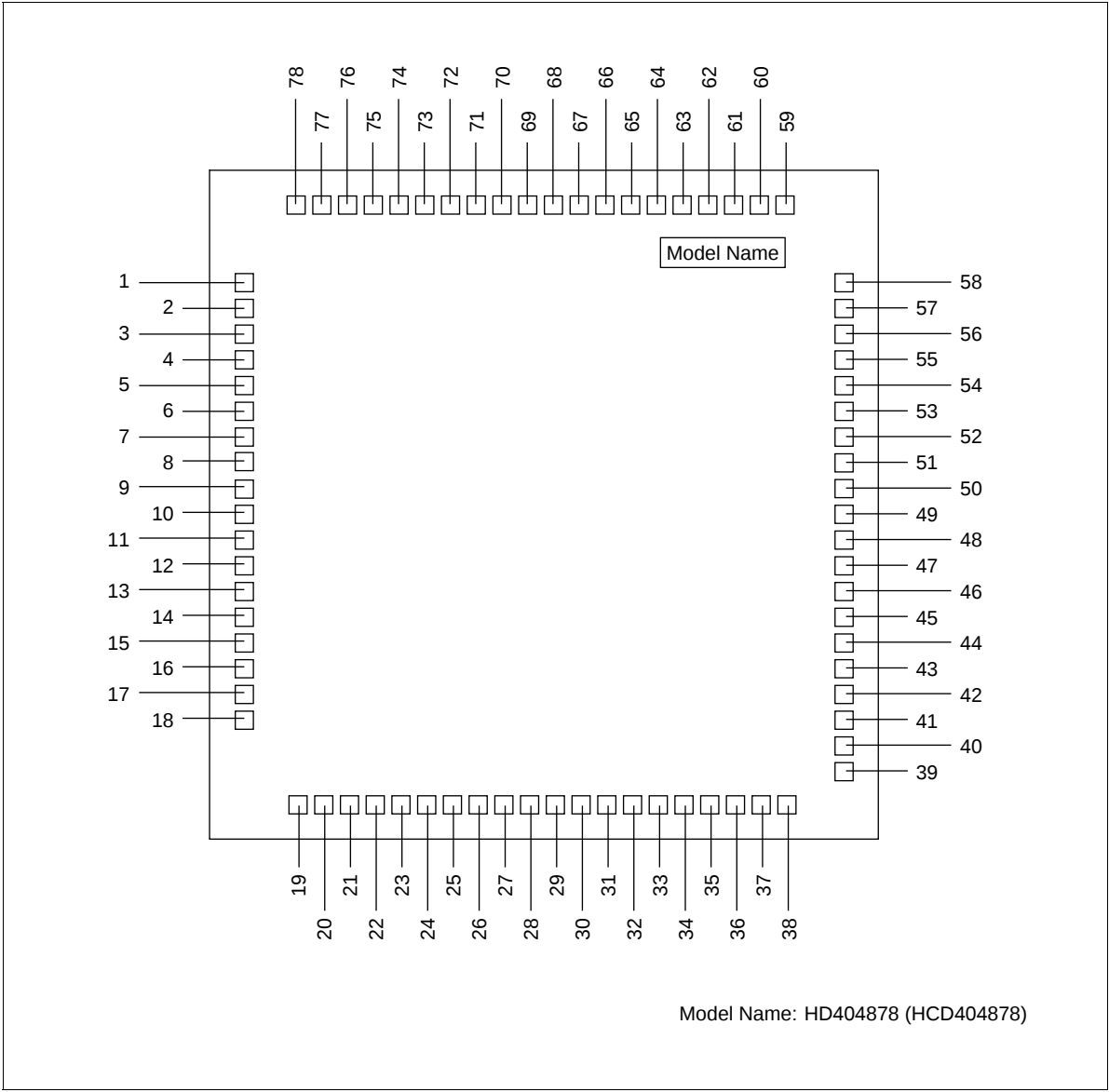


Chip size (X × Y): 4.63 × 4.77 (mm)  
Coordinates: Pad center  
Home point position: Chip center  
Pad size (X × Y): 90 × 90 (μm)  
Chip thickness: 280 (μm)

| Coordinates |                  |        |        | Coordinates |           |        |        |
|-------------|------------------|--------|--------|-------------|-----------|--------|--------|
| Pad No.     | Pad name         | X (μm) | Y (μm) | Pad No.     | Pad name  | X (μm) | Y (μm) |
| 1           | AV <sub>CC</sub> | -2129  | 1779   | 41          | R30/SEG1  | 2129   | -1787  |
| 2           | R70/AN0          | -2129  | 1589   | 42          | R31/SEG2  | 2129   | -1616  |
| 3           | R71/AN1          | -2129  | 1417   | 43          | R32/SEG3  | 2129   | -1445  |
| 4           | R72/AN2          | -2129  | 1246   | 44          | R33/SEG4  | 2129   | -1273  |
| 5           | R73/AN3          | -2129  | 1074   | 45          | R40/SEG5  | 2129   | -1102  |
| 6           | R80/AN4          | -2129  | 903    | 46          | R41/SEG6  | 2129   | -973   |
| 7           | R81/AN5          | -2129  | 732    | 47          | R42/SEG7  | 2129   | -759   |
| 8           | AV <sub>SS</sub> | -2129  | 506    | 48          | R43/SEG8  | 2129   | -588   |
| 9           | TEST             | -2129  | 103    | 49          | R50/SEG9  | 2129   | -417   |
| 10          | OSC1             | -2129  | -68    | 50          | R51/SE10  | 2129   | -245   |
| 11          | OSC2             | -2129  | -240   | 51          | R52/SEG11 | 2129   | -74    |
| 12          | GND              | -2129  | -434   | 52          | R53/SEG12 | 2129   | 98     |
| 13          | X2               | -2129  | -605   | 53          | R60/SEG13 | 2129   | 269    |
| 14          | X1               | -2129  | -776   | 54          | R61/SEG14 | 2129   | 440    |
| 15          | RESETN           | -2129  | -948   | 55          | R62/SEG15 | 2129   | 612    |
| 16          | V <sub>CC</sub>  | -2129  | -1119  | 56          | R63/SEG16 | 2129   | 783    |
| 17          | D0/INT0N         | -2129  | -1290  | 57          | SEG17     | 2129   | 954    |
| 18          | D1/INT1          | -2129  | -1462  | 58          | SEG18     | 2129   | 1126   |
| 19          | D2               | -2129  | -1633  | 59          | SEG19     | 2129   | 1297   |
| 20          | D3               | -2129  | -1804  | 60          | SEG20     | 2129   | 1477   |
| 21          | D4               | -1677  | -2199  | 61          | SEG21     | 1588   | 2199   |
| 22          | D5               | -1506  | -2199  | 62          | SEG22     | 1407   | 2199   |
| 23          | D6               | -1335  | -2199  | 63          | SEG23     | 1236   | 2199   |
| 24          | D7               | -1163  | -2199  | 64          | SEG24     | 1064   | 2199   |
| 25          | D8               | -992   | -2199  | 65          | SEG25     | 893    | 2199   |
| 26          | D9               | -821   | -2199  | 66          | SEG26     | 722    | 2199   |
| 27          | D10              | -649   | -2199  | 67          | SEG27     | 550    | 2199   |
| 28          | D11              | -478   | -2199  | 68          | SEG28     | 379    | 2199   |
| 29          | R00/WU0N         | -307   | -2199  | 69          | SEG29     | 208    | 2199   |
| 30          | R01/WU1N         | -135   | -2199  | 70          | SEG30     | 36     | 2199   |
| 31          | R02/WU2N         | 36     | -2199  | 71          | SEG31     | -135   | 2199   |
| 32          | R03/WU3N         | 208    | -2199  | 72          | SEG32     | -307   | 2199   |
| 33          | R10/EVNB         | 379    | -2199  | 73          | COM1      | -478   | 2199   |
| 34          | R11/EVND         | 550    | -2199  | 74          | COM2      | -649   | 2199   |
| 35          | R12/BUZZ         | 722    | -2199  | 75          | COM3      | -821   | 2199   |
| 36          | R13/TOB          | 893    | -2199  | 76          | COM4      | -992   | 2199   |
| 37          | R20/TOC          | 1064   | -2199  | 77          | V3        | -1163  | 2199   |
| 38          | R21/SCKN         | 1236   | -2199  | 78          | V2        | -1335  | 2199   |
| 39          | R22/SI/SO        | 1407   | -2199  | 79          | V1        | -1506  | 2199   |
| 40          | R23              | 1588   | -2199  | 80          | V0        | -1677  | 2199   |

Pad Arrangement

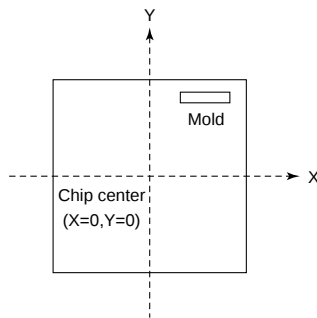
HCD404878



# HD404889/HD404899/HD404878/HD404868 Series

## Pad Coordinates

HCD404878



Chip size (X × Y): 4.13 × 4.26 (mm)  
Coordinates: Pad center  
Home point position: Chip center  
Pad size (X × Y): 90 × 90 (μm)  
Chip thickness: 280 (μm)

| Coordinates |                 |        |        | Coordinates |           |        |        |
|-------------|-----------------|--------|--------|-------------|-----------|--------|--------|
| Pad No.     | Pad name        | X (μm) | Y (μm) | Pad No.     | Pad name  | X (μm) | Y (μm) |
| 1           | R70             | -1879  | 1446   | 40          | R31/SEG2  | 1879   | -1405  |
| 2           | R71             | -1879  | 1280   | 41          | R32/SEG3  | 1879   | -1239  |
| 3           | R72             | -1879  | 1114   | 42          | R33/SEG4  | 1879   | -1072  |
| 4           | R73             | -1879  | 948    | 43          | R40/SEG5  | 1879   | -906   |
| 5           | R80             | -1879  | 781    | 44          | R41/SEG6  | 1879   | -740   |
| 6           | R81             | -1879  | 615    | 45          | R42/SEG7  | 1879   | -573   |
| 7           | TEST            | -1879  | 449    | 46          | R43/SEG8  | 1879   | -407   |
| 8           | OSC1            | -1879  | 282    | 47          | R50/SEG9  | 1879   | -241   |
| 9           | OSC2            | -1879  | 116    | 48          | R51/SE10  | 1879   | -74    |
| 10          | GND             | -1879  | -73    | 49          | R52/SEG11 | 1879   | 92     |
| 11          | X2              | -1879  | -239   | 50          | R53/SEG12 | 1879   | 258    |
| 12          | X1              | -1879  | -406   | 51          | R60/SEG13 | 1879   | 425    |
| 13          | RESETN          | -1879  | -572   | 52          | R61/SEG14 | 1879   | 591    |
| 14          | V <sub>CC</sub> | -1879  | -738   | 53          | R62/SEG15 | 1879   | 757    |
| 15          | D0/INT0N        | -1879  | -905   | 54          | R63/SEG16 | 1879   | 924    |
| 16          | D1/INT1         | -1879  | -1071  | 55          | SEG17     | 1879   | 1087   |
| 17          | D2              | -1879  | -1237  | 56          | SEG18     | 1879   | 1246   |
| 18          | D3              | -1879  | -1404  | 57          | SEG19     | 1879   | 1405   |
| 19          | D4              | -1654  | -1943  | 58          | SEG20     | 1879   | 1564   |
| 20          | D5              | -1488  | -1943  | 59          | SEG21     | 1509   | 1943   |
| 21          | D6              | -1322  | -1943  | 60          | SEG22     | 1351   | 1943   |
| 22          | D7              | -1155  | -1943  | 61          | SEG23     | 1192   | 1943   |
| 23          | D8              | -989   | -1943  | 62          | SEG24     | 1033   | 1943   |
| 24          | D9              | -823   | -1943  | 63          | SEG25     | 874    | 1943   |
| 25          | D10             | -656   | -1943  | 64          | SEG26     | 716    | 1943   |
| 26          | D11             | -490   | -1943  | 65          | SEG27     | 557    | 1943   |
| 27          | R00/WU0N        | -324   | -1943  | 66          | SEG28     | 398    | 1943   |
| 28          | R01/WU1N        | -158   | -1943  | 67          | SEG29     | 239    | 1943   |
| 29          | R02/WU2N        | 9      | -1943  | 68          | SEG30     | 81     | 1943   |
| 30          | R03/WU3N        | 175    | -1943  | 69          | SEG31     | -78    | 1943   |
| 31          | R10/EVNB        | 341    | -1943  | 70          | SEG32     | -237   | 1943   |
| 32          | R11/EVND        | 508    | -1943  | 71          | COM1      | -411   | 1943   |
| 33          | R12/BUZZ        | 674    | -1943  | 72          | COM2      | -570   | 1943   |
| 34          | R13/TOB         | 840    | -1943  | 73          | COM3      | -728   | 1943   |
| 35          | R20/TOC         | 1007   | -1943  | 74          | COM4      | -887   | 1943   |
| 36          | R21/SCKN        | 1173   | -1943  | 75          | V3        | -1038  | 1943   |
| 37          | R22/Si/SO       | 1339   | -1943  | 76          | V2        | -1194  | 1943   |
| 38          | R23             | 1506   | -1943  | 77          | V1        | -1351  | 1943   |
| 39          | R30/SEG1        | 1879   | -1571  | 78          | V0        | -1507  | 1943   |

## Pin Description

HD404889/HD404899/HD404878 Series

| Item             | Symbol                                                                                     | Pin Number        |        | Function                                                                                                                                                                                                         |
|------------------|--------------------------------------------------------------------------------------------|-------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  |                                                                                            | FP-80A<br>TFP-80C | I/O    |                                                                                                                                                                                                                  |
| Power supply     | V <sub>CC</sub>                                                                            | 16                | —      | Apply the power supply voltage to this pin.                                                                                                                                                                      |
|                  | GND                                                                                        | 12                | —      | Connect to ground.                                                                                                                                                                                               |
| Test             | TEST                                                                                       | 9                 | Input  | Not for use by the user application. Connect to GND potential.                                                                                                                                                   |
| Reset            | RESET                                                                                      | 15                | Input  | Used to reset the MCU.                                                                                                                                                                                           |
| Oscillation      | OSC <sub>1</sub>                                                                           | 10                | Input  | Internal oscillator input/output pins. Connect a ceramic resonator, crystal resonator, or external oscillator circuit.                                                                                           |
|                  | OSC <sub>2</sub>                                                                           | 11                | Output |                                                                                                                                                                                                                  |
|                  | X1                                                                                         | 14                | Input  | Realtime clock oscillator input/output pins. Connect a 32.768 kHz crystal. If 32.768 kHz crystal oscillation is not used, fix the ×1 pin to V <sub>CC</sub> and leave the ×2 pin open.                           |
|                  | X2                                                                                         | 13                | Output |                                                                                                                                                                                                                  |
| Port             | D <sub>0</sub> –D <sub>11</sub>                                                            | 17–28             | I/O    | I/O pins addressed bit by bit. D <sub>3</sub> to D <sub>8</sub> are large-current source pins (max. 10 mA), and D <sub>4</sub> to D <sub>11</sub> are large-current sink pins (max. 15 mA).                      |
|                  | R <sub>0</sub> –R <sub>6</sub> <sub>3</sub><br>R <sub>7</sub> –R <sub>8</sub> <sub>1</sub> | 29–56, 2–7        | I/O    | I/O pins, addressed in 4-bit units.                                                                                                                                                                              |
| Interrupt        | INT <sub>0</sub> , INT <sub>1</sub>                                                        | 17, 18            | Input  | External interrupt input pins                                                                                                                                                                                    |
| Wakeup           | WU <sub>0</sub> –WU <sub>3</sub>                                                           | 29–32             | Input  | Input pins used for transition from stop mode to active mode.                                                                                                                                                    |
| Serial interface | SCK                                                                                        | 38                | I/O    | Serial interface clock I/O pin                                                                                                                                                                                   |
|                  | SI                                                                                         | 39                | Input  | Serial interface receive data input pin                                                                                                                                                                          |
|                  | SO                                                                                         | 39                | Output | Serial interface transmit data output pin                                                                                                                                                                        |
| Timer            | TOB, TOC                                                                                   | 36, 37            | Output | Timer output pins                                                                                                                                                                                                |
|                  | EVNB, EVND                                                                                 | 33, 34            | Input  | Event count input pins                                                                                                                                                                                           |
| LCD              | V <sub>0</sub> –V <sub>3</sub>                                                             | 80–77             | —      | LCD driver power supply pins. The on-chip power supply dividing resistor can be disconnected by software. Power supply conditions are: V <sub>CC</sub> ≥ V <sub>1</sub> ≥ V <sub>2</sub> ≥ V <sub>3</sub> ≥ GND. |
|                  | COM1–COM4                                                                                  | 73–76             | Output | LCD common signal pins                                                                                                                                                                                           |
|                  | SEG1–SEG32                                                                                 | 41–72             | Output | LCD segment signal pins                                                                                                                                                                                          |
| A/D converter*1  | AV <sub>CC</sub>                                                                           | 1                 | —      | A/D converter power supply pin. Connect as close as possible to the V <sub>CC</sub> pin so as to be at the same potential as V <sub>CC</sub> .                                                                   |
|                  | AV <sub>SS</sub>                                                                           | 8                 | —      | Ground pin for AV <sub>CC</sub> . Connect as close as possible to the GND pin so as to be at the same potential as GND.                                                                                          |
|                  | AN <sub>0</sub> –AN <sub>5</sub>                                                           | 2–7               | Input  | A/D converter analog input pins                                                                                                                                                                                  |
| Buzzer output    | BUZZ                                                                                       | 35                | Output | Timer overflow toggle output or divided system clock output pin                                                                                                                                                  |
| Other            | NC                                                                                         | 1, 8 <sup>2</sup> | —      | Connect to ground potential.                                                                                                                                                                                     |

Notes: 1. Applies to HD404889 and HD404899 series.

2. Applies to HD404878 series.

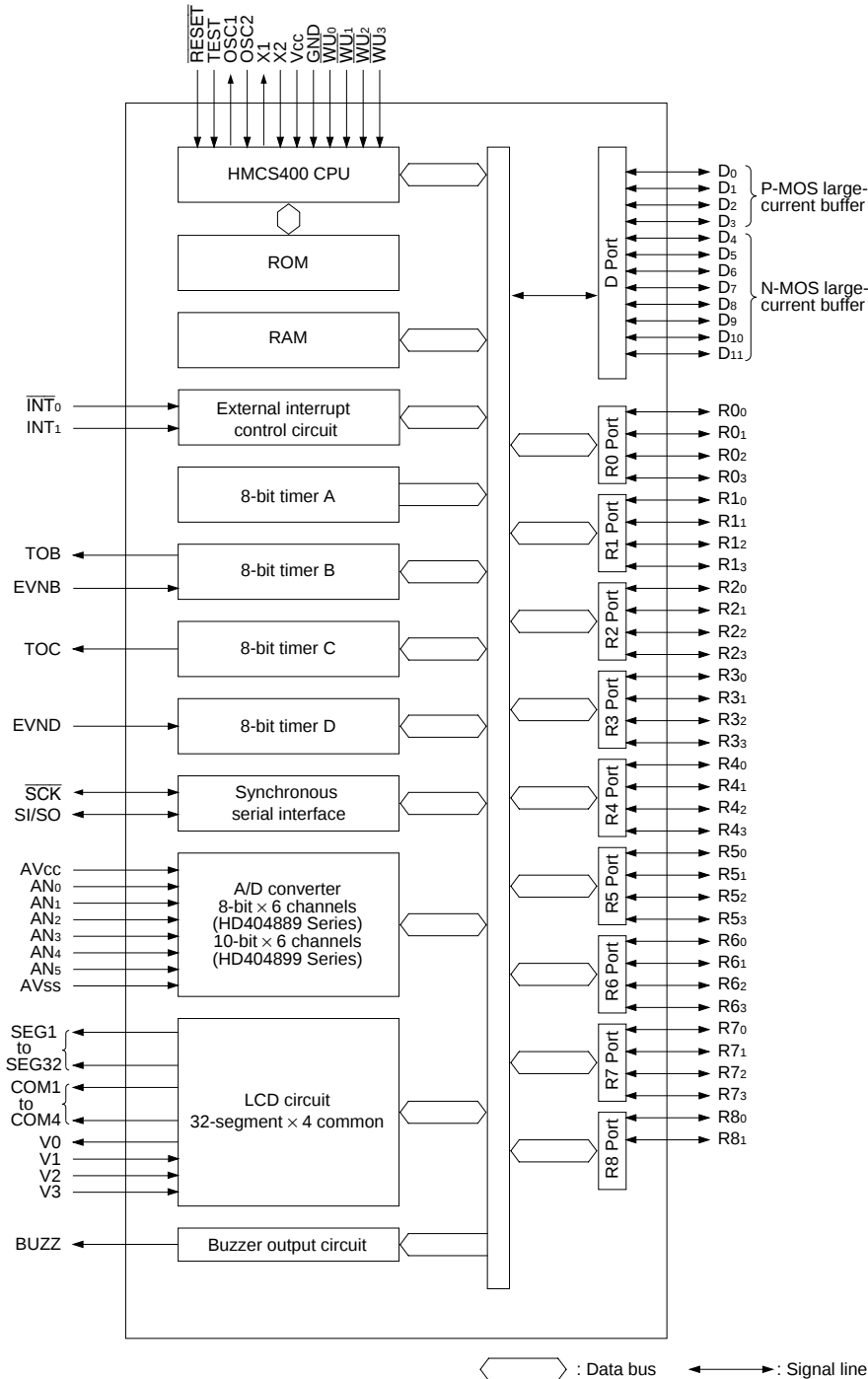
# HD404889/HD404899/HD404878/HD404868 Series

## HD404868 Series

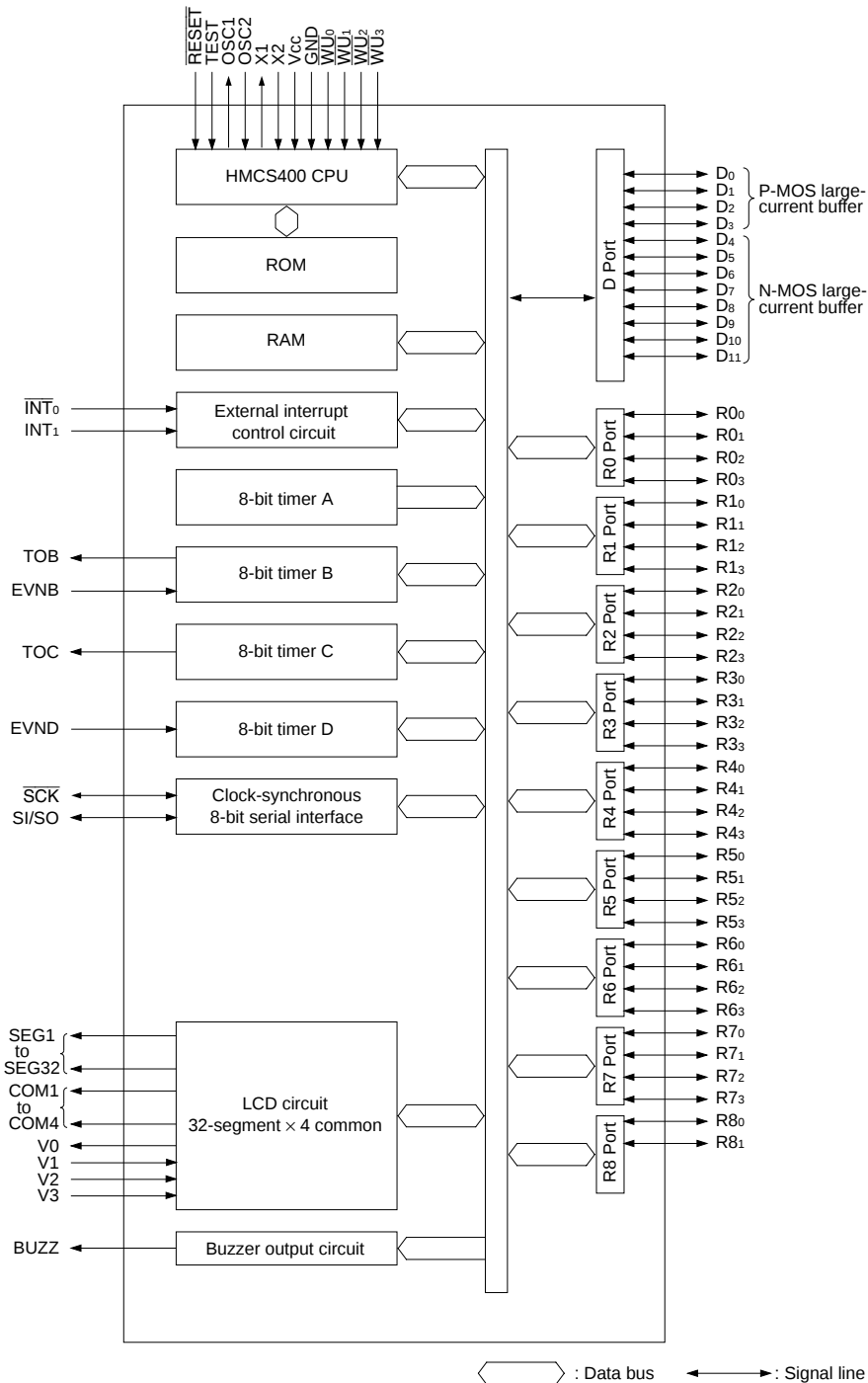
| Item             | Symbol                                                                                                                                    | Pin Number            |                        | I/O    | Function                                                                                                                                                                                                         |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  |                                                                                                                                           | FP-64A                | DP-64S                 |        |                                                                                                                                                                                                                  |
| Power supply     | V <sub>CC</sub>                                                                                                                           | 12                    | 19                     | —      | Apply the power supply voltage to this pin.                                                                                                                                                                      |
|                  | GND                                                                                                                                       | 8                     | 15                     | —      | Connect to ground.                                                                                                                                                                                               |
| Test             | TEST                                                                                                                                      | 5                     | 12                     | Input  | Not for use by the user application. Connect to GND potential.                                                                                                                                                   |
| Reset            | RESET                                                                                                                                     | 11                    | 18                     | Input  | Used to reset the MCU.                                                                                                                                                                                           |
| Oscillation      | OSC <sub>1</sub>                                                                                                                          | 6                     | 13                     | Input  | Internal oscillator input/output pins. Connect a ceramic resonator, crystal resonator, or external oscillator circuit.                                                                                           |
|                  | OSC <sub>2</sub>                                                                                                                          | 7                     | 14                     | Output |                                                                                                                                                                                                                  |
|                  | X1                                                                                                                                        | 10                    | 17                     | Input  | Realtime clock oscillator input/output pins. Connect a 32.768 kHz crystal. If 32.768 kHz crystal oscillation is not used, fix the ×1 pin to V <sub>CC</sub> and leave the ×2 pin open.                           |
|                  | X2                                                                                                                                        | 9                     | 16                     | Output |                                                                                                                                                                                                                  |
| Port             | D <sub>0</sub> –D <sub>9</sub>                                                                                                            | 13–22                 | 20–29                  | I/O    | I/O pins addressed bit by bit. D <sub>0</sub> to D <sub>3</sub> are large-current source pins (max. 10 mA), and D <sub>4</sub> to D <sub>9</sub> are large-current sink pins (max. 15 mA).                       |
|                  | R <sub>0</sub> –R <sub>0</sub> <sub>2</sub><br>R <sub>1</sub> –R <sub>6</sub> <sub>3</sub><br>R <sub>7</sub> –R <sub>7</sub> <sub>3</sub> | 23–25<br>26–49<br>1–4 | 30–32<br>33–56<br>8–11 | I/O    | I/O pins, addressed in 4-bit units.                                                                                                                                                                              |
| Interrupt        | INT <sub>0</sub> , INT <sub>1</sub>                                                                                                       | 13, 14                | 20, 21                 | Input  | External interrupt input pins                                                                                                                                                                                    |
| Wakeup           | WU <sub>0</sub> –WU <sub>2</sub>                                                                                                          | 23–25                 | 30–32                  | Input  | Input pins used for transition from stop mode to active mode.                                                                                                                                                    |
| Serial interface | SCK                                                                                                                                       | 31                    | 38                     | I/O    | Serial interface clock I/O pin                                                                                                                                                                                   |
|                  | SI                                                                                                                                        | 32                    | 39                     | Input  | Serial interface receive data input pin                                                                                                                                                                          |
|                  | SO                                                                                                                                        | 32                    | 39                     | Output | Serial interface transmit data output pin                                                                                                                                                                        |
| Timer            | TOB, TOC                                                                                                                                  | 29, 30                | 36, 37                 | Output | Timer output pins                                                                                                                                                                                                |
|                  | EVNB                                                                                                                                      | 26                    | 33                     | Input  | Event count input pins                                                                                                                                                                                           |
| LCD              | V <sub>1</sub> –V <sub>3</sub>                                                                                                            | 64–62                 | 7–5                    | —      | LCD driver power supply pins. The on-chip power supply dividing resistor can be disconnected by software. Power supply conditions are: V <sub>CC</sub> ≥ V <sub>1</sub> ≥ V <sub>2</sub> ≥ V <sub>3</sub> ≥ GND. |
|                  | COM1–COM4                                                                                                                                 | 58–61                 | 1–4                    | Output | LCD common signal pins                                                                                                                                                                                           |
|                  | SEG1–SEG24                                                                                                                                | 34–57                 | 41–64                  | Output | LCD segment signal pins                                                                                                                                                                                          |
| A/D converter    | AN <sub>0</sub> –AN <sub>3</sub>                                                                                                          | 1–4                   | 8–11                   | Input  | A/D converter analog input pins                                                                                                                                                                                  |
| Buzzer output    | BUZZ                                                                                                                                      | 28                    | 35                     | Output | Timer overflow toggle output or divided system clock output pin                                                                                                                                                  |

Block DiagramG

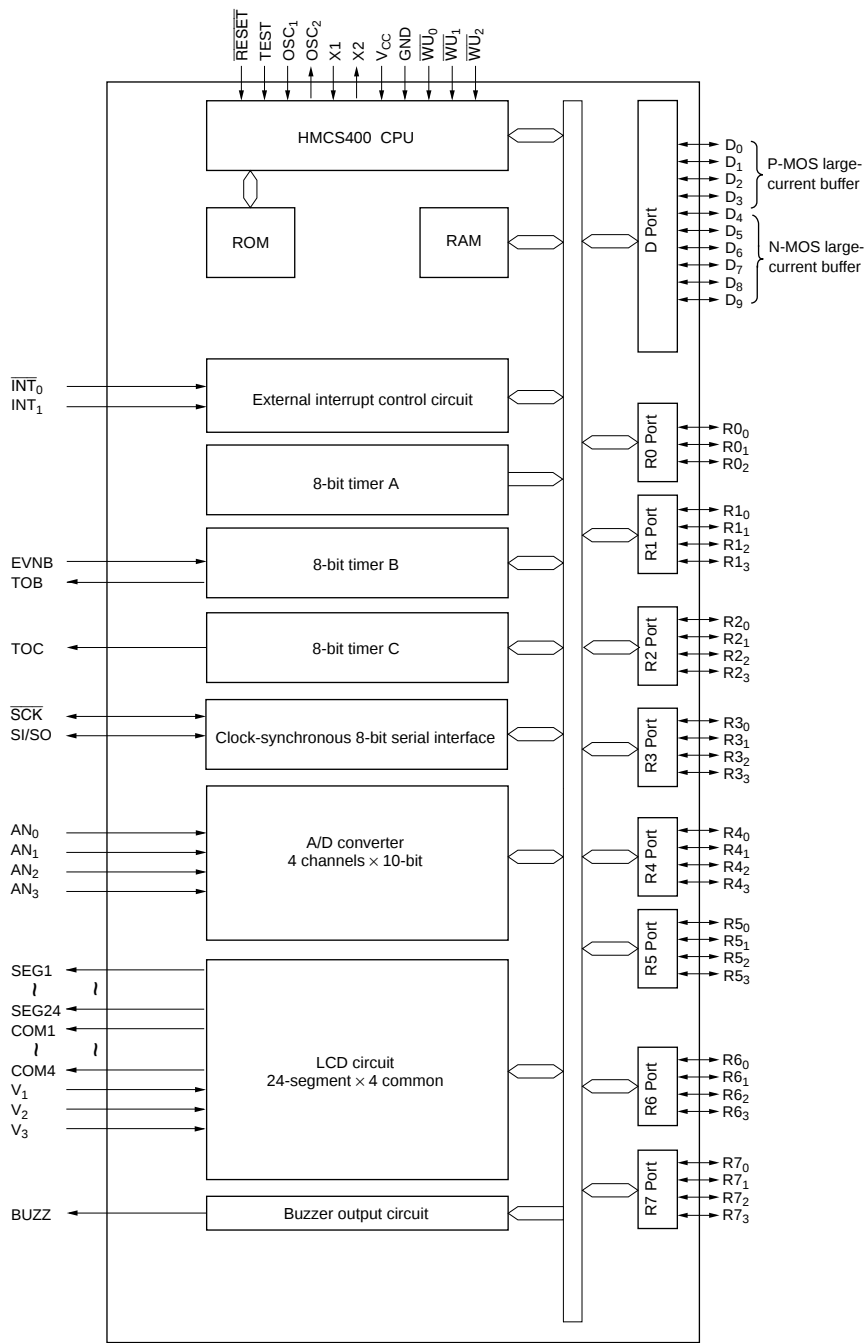
HD404889/HD404899 Series



HD404878 Series



HD404868 Series



## Memory Map

### ROM Memory Map

The ROM memory map is shown in figure 1 and is described below.

**Vector address area** (\$0000 to \$000F): When an MCU reset or interrupt handling is performed, the program is executed from the vector address. A JMPL instruction should be used to branch to the start address of the reset routine or the interrupt routine.

**Zero page subroutine area** (\$0000 to \$003F): A branch can be made to a subroutine in the area \$0000 to \$003F with the CAL instruction.

**Pattern area** (\$0000 to \$0FFF): ROM data in the area \$0000 to \$0FFF can be referenced as pattern data with the P instruction.

**Program area** (\$0000 to \$0FFF (HD404874, HD404864)), (\$0000 to \$1FFF (HD404888, HD404898, HD404878, HD404868, HCD404878)), (\$0000 to \$2FFF (HD4048812, HD4048912)), (\$0000 to \$3FFF (HD404889, HD404899, HCD404889, HCD404899, HD4074899, HD4074889, HD4074869))

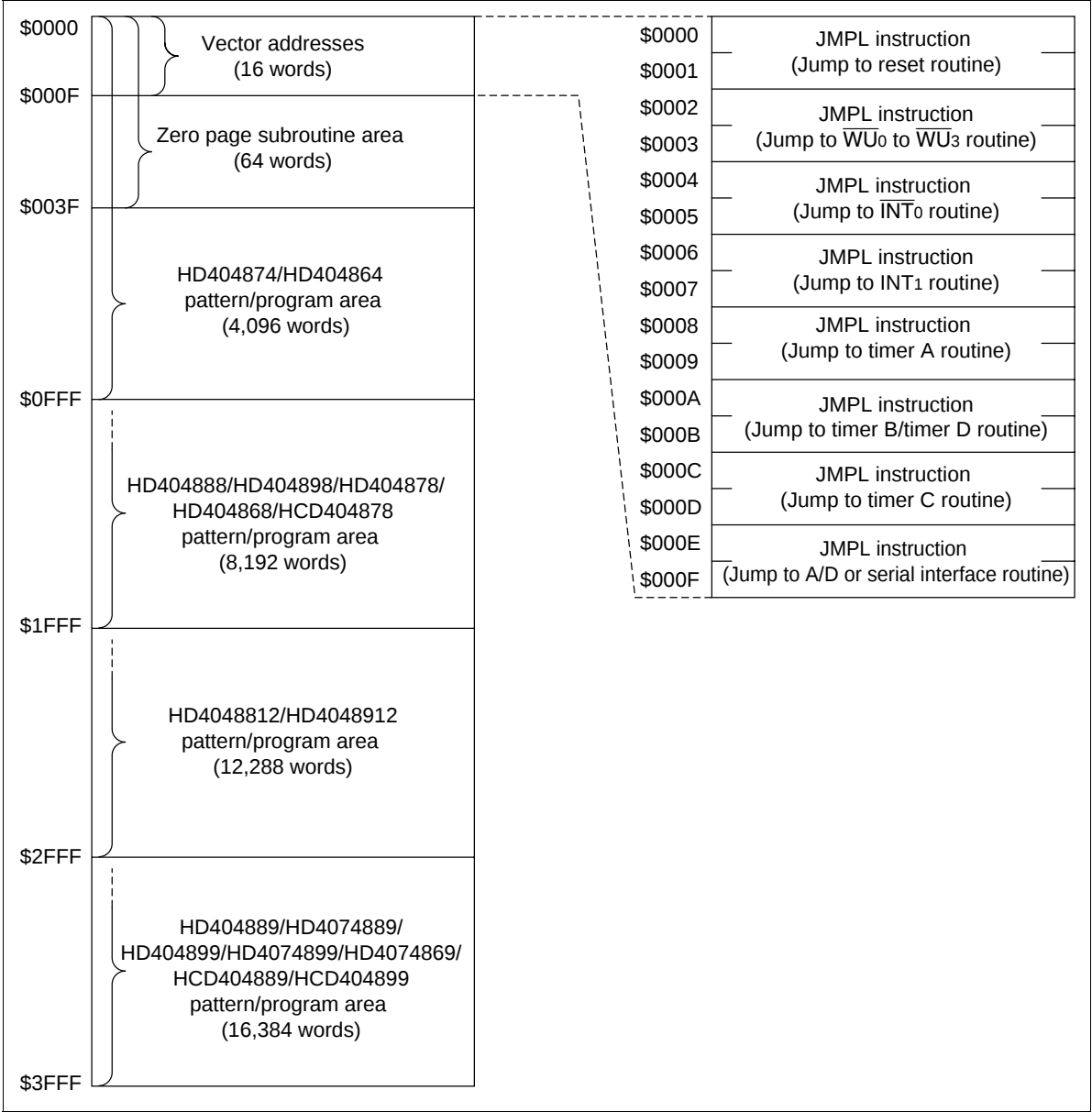


Figure 1 ROM Memory Map

RAM Memory Map

The MCU has on-chip RAM comprising a memory register area, LCD data area, data area, and stack area. In addition to these areas, an interrupt control bit area, special register area, and register flag area are mapped onto RAM memory space as a RAM-mapped register area. The RAM memory map is shown in figure 2 and described below.

**Memory register, LCD data area, data area, and stack area values are unstable immediately after power is turned on. They must be initialized before use.**

HD404889/HD404899/HD404878/HD404868 Series

HD404889 Series

|       |                                          |                                       |       |                                          |                 |
|-------|------------------------------------------|---------------------------------------|-------|------------------------------------------|-----------------|
| \$000 | RAM-mapped<br>register area              |                                       | \$000 | Interrupt control bit area               |                 |
| \$001 |                                          |                                       | \$001 |                                          |                 |
| \$002 |                                          |                                       | \$002 |                                          |                 |
| \$003 | Memory register (MR) area<br>(16 digits) |                                       | \$003 |                                          |                 |
| \$004 |                                          |                                       | \$004 | Speed Select Reg.                        | (SSR) W         |
| \$005 |                                          |                                       | \$005 | Miscellaneous Reg.                       | (MIS) W         |
| \$006 | LCD data area<br>(32 digits)             |                                       | \$006 | Edge Select Reg.                         | (ESR) W         |
| \$007 |                                          |                                       | \$007 | Not used                                 |                 |
| \$008 |                                          |                                       | \$008 | Port Mode Reg.0                          | (PMR0) W        |
| \$009 | Not used                                 |                                       | \$009 | Port Mode Reg.1                          | (PMR1) W        |
| \$00A |                                          |                                       | \$00A | Port Mode Reg.2                          | (PMR2) W        |
| \$00B |                                          |                                       | \$00B | Port Mode Reg.3                          | (PMR3) W        |
| \$00C | Not used                                 |                                       | \$00C | Port Mode Reg.4                          | (PMR4) W        |
| \$00D |                                          |                                       | \$00D | Module Standby Reg.1                     | (MSR1) W        |
| \$00E |                                          |                                       | \$00E | Module Standby Reg.2                     | (MSR2) W        |
| \$00F | Data (464 digits)<br>V = 0 (bank = 0)    | Data (464 digits)<br>V = 1 (bank = 1) | \$00F | Timer Mode Reg.A                         | (TMA) W         |
| \$010 |                                          |                                       | \$010 | Timer Mode Reg.B1                        | (TMB1) W        |
| \$011 |                                          |                                       | \$011 | Timer Mode Reg.B2                        | (TMB2) W        |
| \$012 | Data (304 digits)                        |                                       | \$012 | Timer-B                                  | (TRBL/TWBL) R/W |
| \$013 |                                          |                                       | \$013 |                                          | (TRBU/TWBU) R/W |
| \$014 |                                          |                                       | \$014 | Timer Mode Reg.C1                        | (TMC1) W        |
| \$015 | Not used                                 |                                       | \$015 | Timer Mode Reg.C2                        | (TMC2) W        |
| \$016 |                                          |                                       | \$016 | Timer-C                                  | (TRCL/TWCL) R/W |
| \$017 |                                          |                                       | \$017 |                                          | (TRCU/TWCU) R/W |
| \$018 | Data (304 digits)                        |                                       | \$018 | Timer Mode Reg.D1                        | (TMD1) W        |
| \$019 |                                          |                                       | \$019 | Timer Mode Reg.D2                        | (TMD2) W        |
| \$01A |                                          |                                       | \$01A | Timer-D                                  | (TRDL/TWDL) R/W |
| \$01B | Data (304 digits)                        |                                       | \$01B |                                          | (TRDU/TWDU) R/W |
| \$01C |                                          |                                       | \$01C | Not used                                 |                 |
| \$01D |                                          |                                       | \$01D |                                          |                 |
| \$01E | Not used                                 |                                       | \$01E |                                          |                 |
| \$01F |                                          |                                       | \$01F |                                          |                 |
| \$020 |                                          |                                       | \$020 | Register flag area                       |                 |
| \$021 | Data (304 digits)                        |                                       | \$021 |                                          |                 |
| \$022 |                                          |                                       | \$022 |                                          |                 |
| \$023 |                                          |                                       | \$023 |                                          |                 |
| \$024 | Data (304 digits)                        |                                       | \$024 | Serial Mode Reg.1                        | (SMR1) W        |
| \$025 |                                          |                                       | \$025 | Serial Mode Reg.2                        | (SMR2) W        |
| \$026 |                                          |                                       | \$026 | Serial Data Reg.Lower                    | (SRL) R/W       |
| \$027 | Data (304 digits)                        |                                       | \$027 | Serial Data Reg.Upper                    | (SRU) R/W       |
| \$028 |                                          |                                       | \$028 | A/D Mode reg.                            | (AMR) W         |
| \$029 |                                          |                                       | \$029 | Not used                                 |                 |
| \$02A | Data (304 digits)                        |                                       | \$02A | A/D Data Reg.Lower                       | (ADRL) R        |
| \$02B |                                          |                                       | \$02B | A/D Data Reg.Upper                       | (ADRU) R        |
| \$02C |                                          |                                       | \$02C | LCD Control Reg.                         | (LCR) W         |
| \$02D | Data (304 digits)                        |                                       | \$02D | LCD Mode Reg.                            | (LMR) W         |
| \$02E |                                          |                                       | \$02E | Buzzer Mode Reg.                         | (BMR) W         |
| \$02F |                                          |                                       | \$02F | Not used                                 |                 |
| \$030 | Data (304 digits)                        |                                       | \$030 | Port D <sub>0</sub> ~D <sub>3</sub> DCR  | (DCD0) W        |
| \$031 |                                          |                                       | \$031 | Port D <sub>4</sub> ~D <sub>7</sub> DCR  | (DCD1) W        |
| \$032 |                                          |                                       | \$032 | Port D <sub>8</sub> ~D <sub>11</sub> DCR | (DCD2) W        |
| \$033 | Not used                                 |                                       | \$033 | Not used                                 |                 |
| \$034 |                                          |                                       | \$034 | Port R0 DCR                              | (DCR0) W        |
| \$035 |                                          |                                       | \$035 | Port R1 DCR                              | (DCR1) W        |
| \$036 | Data (304 digits)                        |                                       | \$036 | Port R2 DCR                              | (DCR2) W        |
| \$037 |                                          |                                       | \$037 | Port R3 DCR                              | (DCR3) W        |
| \$038 |                                          |                                       | \$038 | Port R4 DCR                              | (DCR4) W        |
| \$039 | Data (304 digits)                        |                                       | \$039 | Port R5 DCR                              | (DCR5) W        |
| \$03A |                                          |                                       | \$03A | Port R6 DCR                              | (DCR6) W        |
| \$03B |                                          |                                       | \$03B | Port R7 DCR                              | (DCR7) W        |
| \$03C | Stack area<br>(64 digits)                |                                       | \$03C | Port R8 DCR                              | (DCR8) W        |
| \$03D |                                          |                                       | \$03D | Not used                                 |                 |
| \$03E |                                          |                                       | \$03E |                                          |                 |
| \$03F | Stack area<br>(64 digits)                |                                       | \$03F | Vreg.                                    | (V) R/W         |
|       |                                          |                                       |       |                                          |                 |
|       |                                          |                                       |       |                                          |                 |

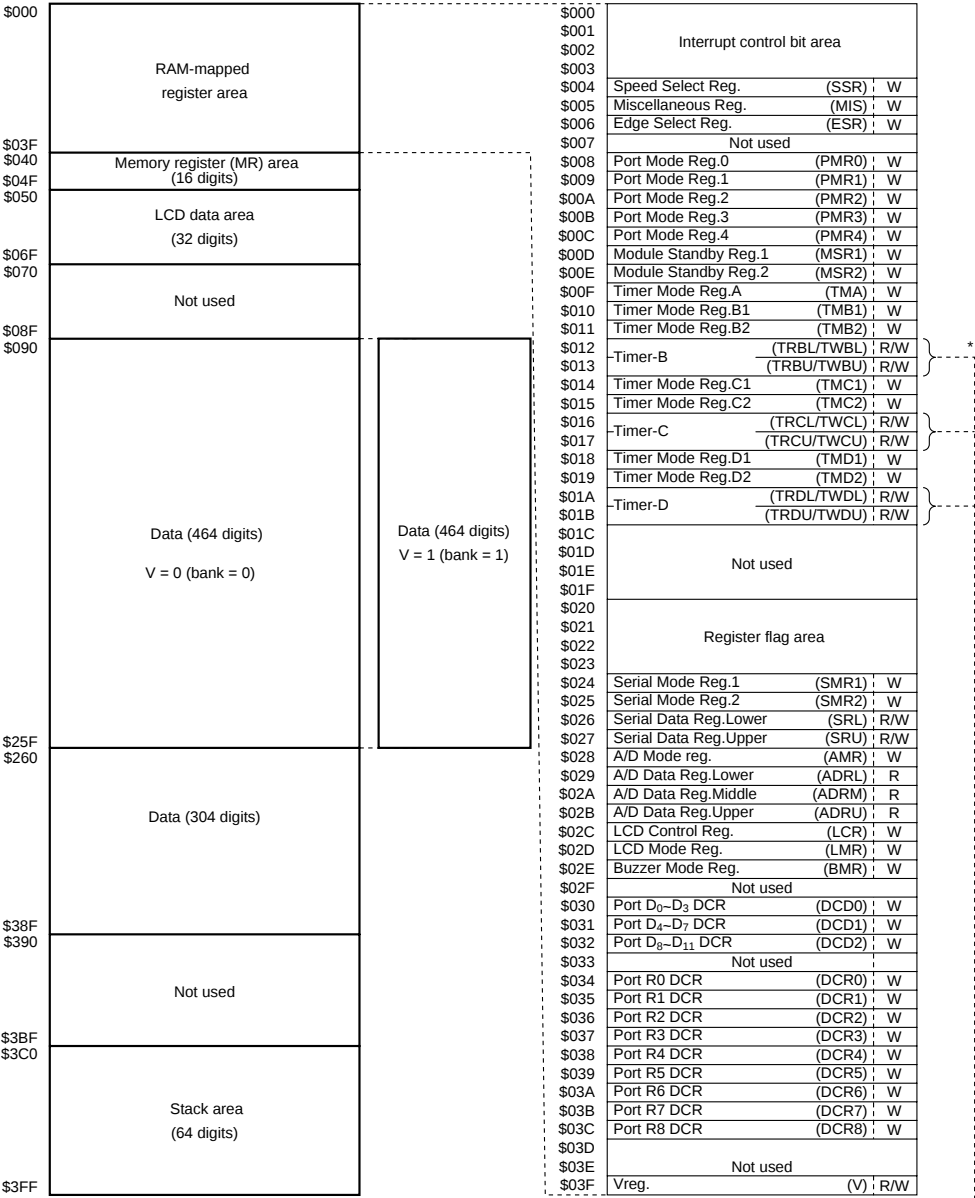
Notes: R : Read  
W : Write  
R/W : Read/Write

\*Two registers are mapped onto the same address (\$012, \$013, \$016, \$017, \$01A, \$01B).

|       |                        |            |                         |            |
|-------|------------------------|------------|-------------------------|------------|
| \$012 | Timer Read Reg.B Lower | (TRBL) ; R | Timer Write Reg.B Lower | (TWBL) ; W |
| \$013 | Timer Read Reg.B Upper | (TRBU) ; R | Timer Write Reg.B Upper | (TWBU) ; W |
| \$016 | Timer Read Reg.C Lower | (TRCL) ; R | Timer Write Reg.C Lower | (TWCL) ; W |
| \$017 | Timer Read Reg.C Upper | (TRCU) ; R | Timer Write Reg.C Upper | (TWCU) ; W |
| \$01A | Timer Read Reg.D Lower | (TRDL) ; R | Timer Write Reg.D Lower | (TWDL) ; W |
| \$01B | Timer Read Reg.D Upper | (TRDU) ; R | Timer Write Reg.D Upper | (TWDU) ; W |

Figure 2 RAM Memory Map

HD404899 Series



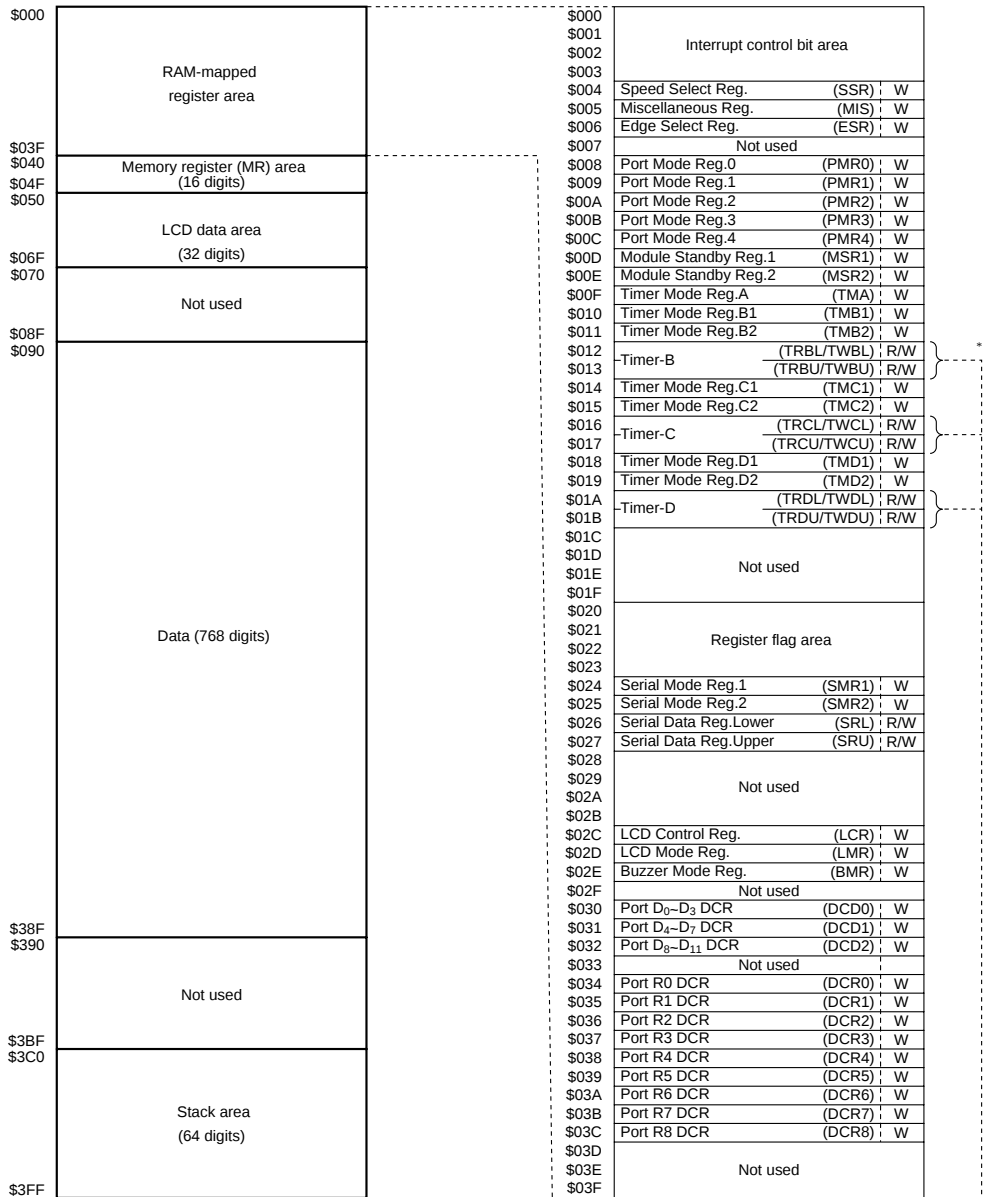
Notes: R : Read  
W : Write  
R/W : Read/Write  
\*Two registers are mapped onto the same address (\$012, \$013, \$016, \$017, \$01A, \$01B).

|       |                                   |                                    |
|-------|-----------------------------------|------------------------------------|
| \$012 | Timer Read Reg.B Lower (TRBL) : R | Timer Write Reg.B Lower (TWBL) : W |
| \$013 | Timer Read Reg.B Upper (TRBU) : R | Timer Write Reg.B Upper (TWBU) : W |
| \$016 | Timer Read Reg.C Lower (TRCL) : R | Timer Write Reg.C Lower (TWCL) : W |
| \$017 | Timer Read Reg.C Upper (TRCU) : R | Timer Write Reg.C Upper (TWCU) : W |
| \$01A | Timer Read Reg.D Lower (TRDL) : R | Timer Write Reg.D Lower (TWDL) : W |
| \$01B | Timer Read Reg.D Upper (TRDU) : R | Timer Write Reg.D Upper (TWDU) : W |

Figure 2 RAM Memory Map (cont)

# HD404889/HD404899/HD404878/HD404868 Series

## HD404878 Series



Notes: R : Read  
W : Write  
R/W : Read/Write  
\*Two registers are mapped onto the same address (\$012, \$013, \$016, \$017, \$01A, \$01B).

|       |                        |           |                         |           |
|-------|------------------------|-----------|-------------------------|-----------|
| \$012 | Timer Read Reg.B Lower | (TRBL); R | Timer Write Reg.B Lower | (TWBL); W |
| \$013 | Timer Read Reg.B Upper | (TRBU); R | Timer Write Reg.B Upper | (TWBU); W |
| \$016 | Timer Read Reg.C Lower | (TRCL); R | Timer Write Reg.C Lower | (TWCL); W |
| \$017 | Timer Read Reg.C Upper | (TRCU); R | Timer Write Reg.C Upper | (TWCU); W |
| \$01A | Timer Read Reg.D Lower | (TRDL); R | Timer Write Reg.D Lower | (TWDL); W |
| \$01B | Timer Read Reg.D Upper | (TRDU); R | Timer Write Reg.D Upper | (TWDU); W |

Figure 2 RAM Memory Map (cont)

HD404868 Series

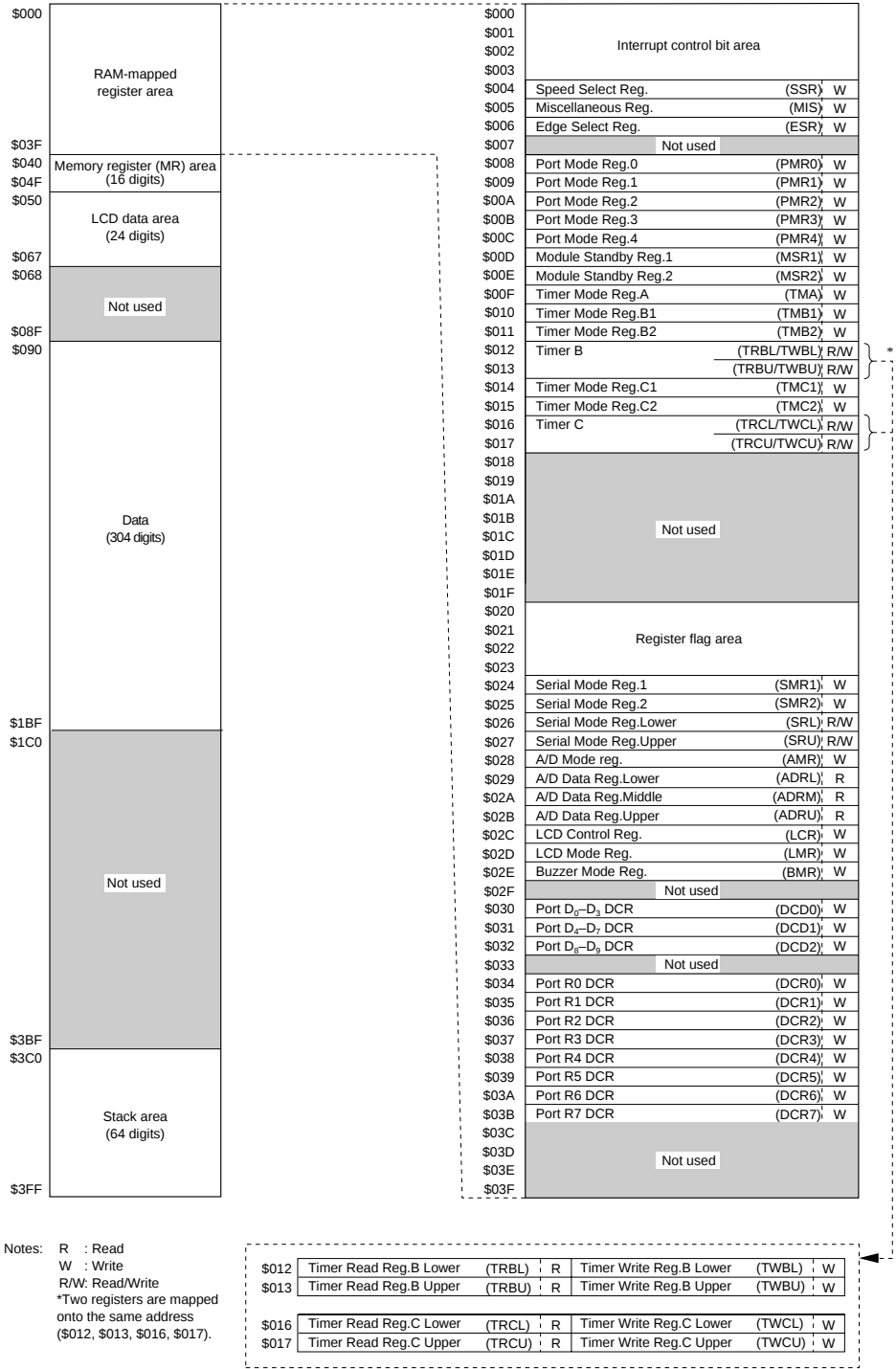


Figure 2 RAM Memory Map (cont)

### RAM-mapped register area (\$000 to \$03F):

- Interrupt control bit area (\$000 to \$003)

This area consists of bits used for interrupt control. Its configuration is shown in figure 3. Individual bits can only be accessed by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, TM/TMD). There are restrictions on access to certain bits. The individual bits and instruction restrictions are shown in figure 4.

- Special register area (\$004 to \$01F, \$024 to \$03F)

This area comprises mode registers and data registers for external interrupts, the serial interface, timers, LCD, A/D converter, etc., and I/O pin data control registers. Its configuration is shown in figures 2 and 5. These registers are of three kinds: write-only (W), read-only (R), and read/write (R/W). The SEM/SEMD and REM/REMD instructions can be used on the LCD control register (LCR: \$02C) and the third bit of buzzer mode register (BMR3: \$02E, 3), but RAM bit manipulation instructions cannot be used on the other registers.

- Register flag area (\$020 to \$023)

This area consists of the DTON and WDON flags and interrupt control bits. Its configuration is shown in figure 3. Individual bits can only be accessed by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, TM/TMD). There are restrictions on access to certain bits. The individual bits and instruction restrictions are shown in figure 4.

### Memory register (MR) area (\$040 to \$04F):

In this data area, the 16 memory register digits (MR(0) to MR(15)) can also be accessed by the register-register instructions LAMR and XMRA. The configuration of this area is shown in figure 6.

### LCD data area: \$050 to \$06F (HD404889/HD404899/HD404878 Series) \$050 to \$067 (HD404868 Series)

This 32-digit data area stores data to be displayed on an LCD. Data written in this area is automatically outputted to segments as display data. "1" data indicates "on" and "0" data "off" (see the section of the LCD circuit for details).

### Data area: \$090 to \$38F (HD404889/HD404899/HD404878 Series) \$090 to \$1BF (HD404868 Series)

For the 464 digits from \$090 to \$25F, the bank can be switched according to the value of the bank register (V: \$03F) (figure 7). The bank register value must always be set when accessing the area from \$090 to \$25F. The data area from \$260 to \$38F can be addressed without a bank register setting.

### Stack area (\$3C0 to \$3FF):

This is the stack area used to save the contents of the program counter (PC), status flag (ST), and carry flag (CA) when a subroutine call (CAL or CALL instruction) or interrupt handling is performed. As four digits are used for one level, the area can be used as a subroutine stack with a maximum of 16 levels. The saved data and saved status information are shown in figure 6. The program counter is restored by the RTN and RTNI instructions. The status and carry flags are restored by the RTNI instruction, but are not affected by the RTN instruction. Any part of the area not used for saving can be used as a data area.

| RAM address | Bit 3                                                                             | Bit 2                                                                                     | Bit 1                                          | Bit 0                                                  |
|-------------|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|------------------------------------------------|--------------------------------------------------------|
| \$000       | IMWU* <sup>1</sup><br>( $\overline{WU}_0$ to $\overline{WU}_3$<br>interrupt mask) | IFWU* <sup>2</sup><br>( $\overline{WU}_0$ to $\overline{WU}_3$<br>interrupt request flag) | RSP<br>(Stack pointer reset)                   | IE<br>(Interrupt enable flag)                          |
| \$001       | IM1<br>(INT1 interrupt mask)                                                      | IF1<br>(INT1 interrupt<br>request flag)                                                   | IM0<br>( $\overline{INT}_0$ interrupt<br>mask) | IF0<br>( $\overline{INT}_0$ interrupt<br>request flag) |
| \$002       | IMTB<br>(Timer B interrupt<br>mask)                                               | IFTB<br>(Timer B interrupt<br>request flag)                                               | IMTA<br>(Timer A interrupt<br>mask)            | IFTA<br>(Timer A interrupt<br>request flag)            |
| \$003       | IMAD* <sup>3</sup><br>(A/D converter<br>interrupt mask)                           | IFAD* <sup>3</sup><br>(A/D converter interrupt<br>request flag)                           | IMTC<br>(Timer C interrupt<br>mask)            | IFTC<br>(Timer C interrupt<br>request flag)            |
|             |                                                                                   |                                                                                           |                                                |                                                        |
| \$020       | DTON<br>(DTON flag)                                                               | ADSF* <sup>3</sup><br>(A/D start flag)                                                    | WDON<br>(Watchdog on flag)                     | LSON<br>(Low speed on flag)                            |
| \$021       | GEF<br>(Gear enable flag)                                                         | Not used                                                                                  | ICEF<br>(Input capture error<br>flag)          | ICSF<br>(Input capture status<br>flag)                 |
| \$022       | IMTD* <sup>4</sup><br>(Timer D interrupt mask)                                    | IFTD* <sup>4</sup><br>(Timer D interrupt<br>request flag)                                 | Not used                                       | Not used                                               |
| \$023       | IMS<br>(Serial interrupt<br>mask)                                                 | IFS<br>(Serial interrupt<br>request flag)                                                 | Not used                                       | Not used                                               |

IF : Interrupt Request Flag  
IM : Interrupt Mask  
IE : Interrupt Enable Flag  
SP : Stack Pointer

Notes: 1.  $\overline{WU}_0$  to  $\overline{WU}_2$  interrupt mask in the HD404868 Series  
2.  $\overline{WU}_0$  to  $\overline{WU}_2$  interrupt request flag in the HD404868 Series  
3. Applies to the HD404889, HD404899, and HD404868 Series.  
4. Applies to the HD404889, HD404899, and HD404878 Series.

Figure 3 Interrupt Control Bit and Register Flag Area Configuration

Bits in the interrupt control bit area and register flag area can be set and reset by the SEM or SEMD instruction and the REM or REMD instruction, and tested by the TM or TMD instruction. They are not affected by any other instructions.  
The following restrictions apply to individual bits.

|          | SEM/SEMD                    | REM/REMD     | TM/TMD    |
|----------|-----------------------------|--------------|-----------|
| IE       | Allowed                     | Allowed      | Allowed   |
| IM       |                             |              |           |
| LSON     |                             |              |           |
| IF       | Not executed                | Allowed      | Allowed   |
| ICSF     |                             |              |           |
| ICEF     |                             |              |           |
| GEF      | Allowed                     | Allowed      | Inhibited |
| RSP      | Not executed                | Allowed      | Inhibited |
| WDON     | Allowed                     | Not executed | Inhibited |
| ADSF*    | Allowed                     | Inhibited    | Allowed   |
| DTON     | Not executed in active mode | Allowed      | Allowed   |
|          | Used in subactive mode      |              |           |
| Not Used | Not executed                | Not executed | Inhibited |

Notes : The WDON bit is reset only by stop mode clearance by means of an MCU reset.  
Do not use the REM or REMD instruction on the ADSF bit during A/D conversion.  
The DTON bit is always in the reset state in active mode.  
If the TM or TMD instruction is used on a bit for which its use is prohibited, or on a nonexistent bit, the status flag value will be undetermined.  
\* Applies to HD404889, HD404899, and HD404868 Series.

Figure 4 Instruction Restrictions

## HD404889 Series

| RAM address     | Bit 3                                 | Bit 2                                     | Bit 1                            | Bit 0                                           |
|-----------------|---------------------------------------|-------------------------------------------|----------------------------------|-------------------------------------------------|
| \$000           | Interrupt control bit area            |                                           |                                  |                                                 |
| \$003           |                                       |                                           |                                  |                                                 |
| SSR \$004       | 32 kHz oscillation stop setting       | 32 kHz frequency division ratio selection | System clock selection           | System clock frequency division ratio switching |
| MIS \$005       | Pull-up MOS control                   | Not used                                  | Interrupt frame period selection |                                                 |
| ESR \$006       | Not used                              |                                           | INT1 edge detection selection    |                                                 |
| \$007           | Not used                              |                                           |                                  |                                                 |
| PMR0 \$008      | Not used                              |                                           | D <sub>1</sub> /INT <sub>1</sub> | D <sub>0</sub> /INT <sub>0</sub>                |
| PMR1 \$009      | R0 <sub>3</sub> /WU <sub>3</sub>      | R0 <sub>2</sub> /WU <sub>2</sub>          | R0 <sub>1</sub> /WU <sub>1</sub> | R0 <sub>0</sub> /WU <sub>0</sub>                |
| PMR2 \$00A      | R1 <sub>3</sub> /TOB                  | R1 <sub>2</sub> /BUZZ                     | R1 <sub>1</sub> /EVND            | R1 <sub>0</sub> /EVNB                           |
| PMR3 \$00B      | R2 <sub>2</sub> /SI/SO                |                                           | R2 <sub>1</sub> /SCK             | R2 <sub>0</sub> /TOC                            |
| PMR4 \$00C      | R6/SEG13~16                           | R5/SEG9~12                                | R4/SEG5~8                        | R3/SEG1~4                                       |
| MSR1 \$00D      | Not used                              | Timer D clock on/off                      | Timer C clock on/off             | Timer B lock on/off                             |
| MSR2 \$00E      | Not used                              |                                           | A/D clock on/off                 | Serial clock on/off                             |
| TMA \$00F       | TimerA/Timer base                     | Timer A clock source selection            |                                  |                                                 |
| TMB1 \$010      | Reload on/off                         | Timer B clock source selection            |                                  |                                                 |
| TMB2 \$011      | Not used                              | Timer B output mode setting               | EVNB edge detection selection    |                                                 |
| TRBL/TWBL \$012 | Timer B register (lower)              |                                           |                                  |                                                 |
| TRBU/TWBU \$013 | Timer B register (upper)              |                                           |                                  |                                                 |
| TMC1 \$014      | Reload on/off                         | Timer C clock source selection            |                                  |                                                 |
| TMC2 \$015      | Not used                              | Timer C output mode selection             | Not used                         |                                                 |
| TRCL/TWCL \$016 | Timer C register (lower)              |                                           |                                  |                                                 |
| TRCU/TWCU \$017 | Timer C register (upper)              |                                           |                                  |                                                 |
| TMD1 \$018      | Reload on/off                         | Timer D clock source selection            |                                  |                                                 |
| TMD2 \$019      | Not used                              | Input capture selection                   | EVND edge detection selection    |                                                 |
| TRDL/TWDL \$01A | Timer D register (lower)              |                                           |                                  |                                                 |
| TRDU/TWDU \$01B | Timer D register (upper)              |                                           |                                  |                                                 |
| \$01C           | Not used                              |                                           |                                  |                                                 |
| \$01F           |                                       |                                           |                                  |                                                 |
| \$020           |                                       |                                           |                                  |                                                 |
| \$023           | Register flag area                    |                                           |                                  |                                                 |
| SMR1 \$024      | Serial transfer clock speed selection |                                           |                                  |                                                 |
| SMR2 \$025      | Not used                              | R2 <sub>2</sub> /SI/SO PMOS control       | SO idle H/L setting              | Not used                                        |
| SRL \$026       | Serial data register (lower)          |                                           |                                  |                                                 |
| SRU \$027       | Serial data register (upper)          |                                           |                                  |                                                 |
| AMR \$028       | Analog channel selection              |                                           |                                  | A/D conversion time                             |
| \$029           | Not used                              |                                           |                                  |                                                 |
| ADRL \$02A      | A/D data register (lower)             |                                           |                                  |                                                 |
| ADRU \$02B      | A/D data register (upper)             |                                           |                                  |                                                 |
| LCR \$02C       | Power supply dividing resistor switch | Realtime clock mode display selection     | On-chip power supply switch      | Display on/off                                  |
| LMR \$02D       | Input clock selection                 |                                           | Duty selection                   |                                                 |
| BMR \$02E       | Clock output on/off                   | Buzzer/clock selection                    | Buzzer/clock source selection    |                                                 |
| \$02F           | Not used                              |                                           |                                  |                                                 |
| DCD0 \$030      | PortD <sub>3</sub> DCR                | PortD <sub>2</sub> DCR                    | PortD <sub>1</sub> DCR           | PortD <sub>0</sub> DCR                          |
| DCD1 \$031      | PortD <sub>7</sub> DCR                | PortD <sub>6</sub> DCR                    | PortD <sub>5</sub> DCR           | PortD <sub>4</sub> DCR                          |
| DCD2 \$032      | PortD <sub>11</sub> DCR               | PortD <sub>10</sub> DCR                   | PortD <sub>9</sub> DCR           | PortD <sub>8</sub> DCR                          |
| \$033           | Not used                              |                                           |                                  |                                                 |
| DCR0 \$034      | PortR0 <sub>3</sub> DCR               | PortR0 <sub>2</sub> DCR                   | PortR0 <sub>1</sub> DCR          | PortR0 <sub>0</sub> DCR                         |
| DCR1 \$035      | PortR1 <sub>3</sub> DCR               | PortR1 <sub>2</sub> DCR                   | PortR1 <sub>1</sub> DCR          | PortR1 <sub>0</sub> DCR                         |
| DCR2 \$036      | PortR2 <sub>3</sub> DCR               | PortR2 <sub>2</sub> DCR                   | PortR2 <sub>1</sub> DCR          | PortR2 <sub>0</sub> DCR                         |
| DCR3 \$037      | PortR3 <sub>3</sub> DCR               | PortR3 <sub>2</sub> DCR                   | PortR3 <sub>1</sub> DCR          | PortR3 <sub>0</sub> DCR                         |
| DCR4 \$038      | PortR4 <sub>3</sub> DCR               | PortR4 <sub>2</sub> DCR                   | PortR4 <sub>1</sub> DCR          | PortR4 <sub>0</sub> DCR                         |
| DCR5 \$039      | PortR5 <sub>3</sub> DCR               | PortR5 <sub>2</sub> DCR                   | PortR5 <sub>1</sub> DCR          | PortR5 <sub>0</sub> DCR                         |
| DCR6 \$03A      | PortR6 <sub>3</sub> DCR               | PortR6 <sub>2</sub> DCR                   | PortR6 <sub>1</sub> DCR          | PortR6 <sub>0</sub> DCR                         |
| DCR7 \$03B      | PortR7 <sub>3</sub> DCR               | PortR7 <sub>2</sub> DCR                   | PortR7 <sub>1</sub> DCR          | PortR7 <sub>0</sub> DCR                         |
| DCR8 \$03C      | Not used                              |                                           | PortR8 <sub>1</sub> DCR          | PortR8 <sub>0</sub> DCR                         |
| \$03D           | Not used                              |                                           |                                  |                                                 |
| \$03E           | Not used                              |                                           |                                  |                                                 |
| V \$03F         | Not used                              |                                           |                                  | Bank setting                                    |

Figure 5 Special Function Register Area

HD404899 Series

| RAM address     | Bit 3                                 | Bit 2                                     | Bit 1                            | Bit 0                                           |
|-----------------|---------------------------------------|-------------------------------------------|----------------------------------|-------------------------------------------------|
| \$000           | Interrupt control bit area            |                                           |                                  |                                                 |
| \$003           |                                       |                                           |                                  |                                                 |
| SSR \$004       | 32 kHz oscillation stop setting       | 32 kHz frequency division ratio selection | System clock selection           | System clock frequency division ratio switching |
| MIS \$005       | Pull-up MOS control                   | Not used                                  | Interrupt frame period selection |                                                 |
| ESR \$006       | Not used                              |                                           | INT1 edge detection selection    |                                                 |
| \$007           | Not used                              |                                           |                                  |                                                 |
| PMR0 \$008      | Not used                              |                                           | D <sub>1</sub> /INT <sub>1</sub> | D <sub>0</sub> /INT <sub>0</sub>                |
| PMR1 \$009      | R0 <sub>3</sub> /WU <sub>3</sub>      | R0 <sub>2</sub> /WU <sub>2</sub>          | R0 <sub>1</sub> /WU <sub>1</sub> | R0 <sub>0</sub> /WU <sub>0</sub>                |
| PMR2 \$00A      | R1 <sub>3</sub> /TOB                  | R1 <sub>2</sub> /BUZZ                     | R1 <sub>1</sub> /EVND            | R1 <sub>0</sub> /EVNB                           |
| PMR3 \$00B      | R2 <sub>2</sub> /SI/SO                |                                           | R2 <sub>1</sub> /SCK             | R2 <sub>0</sub> /TOC                            |
| PMR4 \$00C      | R6/SEG13~16                           | R5/SEG9~12                                | R4/SEG5~8                        | R3/SEG1~4                                       |
| MSR1 \$00D      | Not used                              | Timer D clock on/off                      | Timer C clock on/off             | Timer B lock on/off                             |
| MSR2 \$00E      | Not used                              |                                           | A/D clock on/off                 | Serial clock on/off                             |
| TMA \$00F       | TimerA/Timer base                     | Timer A clock source selection            |                                  |                                                 |
| TMB1 \$010      | Reload on/off                         | Timer B clock source selection            |                                  |                                                 |
| TMB2 \$011      | Not used                              | Timer B output mode setting               | EVNB edge detection selection    |                                                 |
| TRBL/TWBL \$012 | Timer B register (lower)              |                                           |                                  |                                                 |
| TRBU/TWBU \$013 | Timer B register (upper)              |                                           |                                  |                                                 |
| TMC1 \$014      | Reload on/off                         | Timer C clock source selection            |                                  |                                                 |
| TMC2 \$015      | Not used                              | Timer C output mode selection             | Not used                         |                                                 |
| TRCL/TWCL \$016 | Timer C register (lower)              |                                           |                                  |                                                 |
| TRCU/TWCU \$017 | Timer C register (upper)              |                                           |                                  |                                                 |
| TMD1 \$018      | Reload on/off                         | Timer D clock source selection            |                                  |                                                 |
| TMD2 \$019      | Not used                              | Input capture selection                   | EVND edge detection selection    |                                                 |
| TRDL/TWDL \$01A | Timer D register (lower)              |                                           |                                  |                                                 |
| TRDU/TWDU \$01B | Timer D register (upper)              |                                           |                                  |                                                 |
| \$01C           | Not used                              |                                           |                                  |                                                 |
| \$01F           |                                       |                                           |                                  |                                                 |
| \$020           |                                       |                                           |                                  |                                                 |
| \$023           | Register flag area                    |                                           |                                  |                                                 |
| SMR1 \$024      | Serial transfer clock speed selection |                                           |                                  |                                                 |
| SMR2 \$025      | Not used                              | R2 <sub>2</sub> /SI/SO PMOS control       | SO idle H/L setting              | Not used                                        |
| SRL \$026       | Serial data register (lower)          |                                           |                                  |                                                 |
| SRU \$027       | Serial data register (upper)          |                                           |                                  |                                                 |
| AMR \$028       | Analog channel selection              |                                           |                                  | A/D conversion time                             |
| ADRL \$029      | A/D data register (lower)             |                                           | Not used                         |                                                 |
| ADRM \$02A      | A/D data register (middle)            |                                           |                                  |                                                 |
| ADRU \$02B      | A/D data register (upper)             |                                           |                                  |                                                 |
| LCR \$02C       | Power supply dividing resistor switch | Realtime clock mode display selection     | On-chip power supply switch      | Display on/off                                  |
| LMR \$02D       | Input clock selection                 |                                           | Duty selection                   |                                                 |
| BMR \$02E       | Clock output on/off                   | Buzzer/clock selection                    | Buzzer/clock source selection    |                                                 |
| \$02F           | Not used                              |                                           |                                  |                                                 |
| DCD0 \$030      | PortD <sub>3</sub> DCR                | PortD <sub>2</sub> DCR                    | PortD <sub>1</sub> DCR           | PortD <sub>0</sub> DCR                          |
| DCD1 \$031      | PortD <sub>7</sub> DCR                | PortD <sub>6</sub> DCR                    | PortD <sub>5</sub> DCR           | PortD <sub>4</sub> DCR                          |
| DCD2 \$032      | PortD <sub>11</sub> DCR               | PortD <sub>10</sub> DCR                   | PortD <sub>9</sub> DCR           | PortD <sub>8</sub> DCR                          |
| \$033           | Not used                              |                                           |                                  |                                                 |
| DCR0 \$034      | PortR0 <sub>3</sub> DCR               | PortR0 <sub>2</sub> DCR                   | PortR0 <sub>1</sub> DCR          | PortR0 <sub>0</sub> DCR                         |
| DCR1 \$035      | PortR1 <sub>3</sub> DCR               | PortR1 <sub>2</sub> DCR                   | PortR1 <sub>1</sub> DCR          | PortR1 <sub>0</sub> DCR                         |
| DCR2 \$036      | PortR2 <sub>3</sub> DCR               | PortR2 <sub>2</sub> DCR                   | PortR2 <sub>1</sub> DCR          | PortR2 <sub>0</sub> DCR                         |
| DCR3 \$037      | PortR3 <sub>3</sub> DCR               | PortR3 <sub>2</sub> DCR                   | PortR3 <sub>1</sub> DCR          | PortR3 <sub>0</sub> DCR                         |
| DCR4 \$038      | PortR4 <sub>3</sub> DCR               | PortR4 <sub>2</sub> DCR                   | PortR4 <sub>1</sub> DCR          | PortR4 <sub>0</sub> DCR                         |
| DCR5 \$039      | PortR5 <sub>3</sub> DCR               | PortR5 <sub>2</sub> DCR                   | PortR5 <sub>1</sub> DCR          | PortR5 <sub>0</sub> DCR                         |
| DCR6 \$03A      | PortR6 <sub>3</sub> DCR               | PortR6 <sub>2</sub> DCR                   | PortR6 <sub>1</sub> DCR          | PortR6 <sub>0</sub> DCR                         |
| DCR7 \$03B      | PortR7 <sub>3</sub> DCR               | PortR7 <sub>2</sub> DCR                   | PortR7 <sub>1</sub> DCR          | PortR7 <sub>0</sub> DCR                         |
| DCR8 \$03C      | Not used                              |                                           | PortR8 <sub>1</sub> DCR          | PortR8 <sub>0</sub> DCR                         |
| \$03D           | Not used                              |                                           |                                  |                                                 |
| \$03E           | Not used                              |                                           |                                  |                                                 |
| V \$03F         | Not used                              |                                           |                                  | Bank setting                                    |

Figure 5 Special Function Register Area (cont)

## HD404878 Series

| RAM address     | Bit 3                                 | Bit 2                                     | Bit 1                            | Bit 0                                           |
|-----------------|---------------------------------------|-------------------------------------------|----------------------------------|-------------------------------------------------|
| \$000           | Interrupt control bit area            |                                           |                                  |                                                 |
| \$003           |                                       |                                           |                                  |                                                 |
| SSR \$004       | 32 kHz oscillation stop setting       | 32 kHz frequency division ratio selection | System clock selection           | System clock frequency division ratio switching |
| MIS \$005       | Pull-up MOS control                   | Not used                                  | Interrupt frame period selection |                                                 |
| ESR \$006       | Not used                              |                                           | INT1 edge detection selection    |                                                 |
| \$007           | Not used                              |                                           |                                  |                                                 |
| PMR0 \$008      | Not used                              |                                           | D <sub>1</sub> /INT <sub>1</sub> | D <sub>0</sub> /INT <sub>0</sub>                |
| PMR1 \$009      | R0 <sub>3</sub> /WU <sub>3</sub>      | R0 <sub>2</sub> /WU <sub>2</sub>          | R0 <sub>1</sub> /WU <sub>1</sub> | R0 <sub>0</sub> /WU <sub>0</sub>                |
| PMR2 \$00A      | R1 <sub>3</sub> /TOB                  | R1 <sub>2</sub> /BUZZ                     | R1 <sub>1</sub> /EVND            | R1 <sub>0</sub> /EVNB                           |
| PMR3 \$00B      | R2 <sub>2</sub> /SI/SO                |                                           | R2 <sub>1</sub> /SCK             | R2 <sub>0</sub> /TOC                            |
| PMR4 \$00C      | R6/SEG13~16                           | R5/SEG9~12                                | R4/SEG5~8                        | R3/SEG1~4                                       |
| MSR1 \$00D      | Not used                              | Timer D clock on/off                      | Timer C clock on/off             | Timer B lock on/off                             |
| MSR2 \$00E      | Not used                              |                                           |                                  | Serial clock on/off                             |
| TMA \$00F       | TimerA/Timer base                     | Timer A clock source selection            |                                  |                                                 |
| TMB1 \$010      | Reload on/off                         | Timer B clock source selection            |                                  |                                                 |
| TMB2 \$011      | Not used                              | Timer B output mode setting               | EVNB edge detection selection    |                                                 |
| TRBL/TWBL \$012 | Timer B register (lower)              |                                           |                                  |                                                 |
| TRBU/TWBU \$013 | Timer B register (upper)              |                                           |                                  |                                                 |
| TMC1 \$014      | Reload on/off                         | Timer C clock source selection            |                                  |                                                 |
| TMC2 \$015      | Not used                              | Timer C output mode selection             | Not used                         |                                                 |
| TRCL/TWCL \$016 | Timer C register (lower)              |                                           |                                  |                                                 |
| TRCU/TWCU \$017 | Timer C register (upper)              |                                           |                                  |                                                 |
| TMD1 \$018      | Reload on/off                         | Timer D clock source selection            |                                  |                                                 |
| TMD2 \$019      | Not used                              | Input capture selection                   | EVND edge detection selection    |                                                 |
| TRDL/TWDL \$01A | Timer D register (lower)              |                                           |                                  |                                                 |
| TRDU/TWDU \$01B | Timer D register (upper)              |                                           |                                  |                                                 |
| \$01C           | Not used                              |                                           |                                  |                                                 |
| \$01F           |                                       |                                           |                                  |                                                 |
| \$020           |                                       |                                           |                                  |                                                 |
| \$023           | Register flag area                    |                                           |                                  |                                                 |
| SMR1 \$024      | Serial transfer clock speed selection |                                           |                                  |                                                 |
| SMR2 \$025      | Not used                              | R2 <sub>2</sub> /SI/SO PMOS control       | SO idle H/L setting              | Not used                                        |
| SRL \$026       | Serial data register (lower)          |                                           |                                  |                                                 |
| SRU \$027       | Serial data register (upper)          |                                           |                                  |                                                 |
| \$028           | Not used                              |                                           |                                  |                                                 |
| \$029           |                                       |                                           |                                  |                                                 |
| \$02A           |                                       |                                           |                                  |                                                 |
| \$02B           |                                       |                                           |                                  |                                                 |
| LCR \$02C       | Power supply dividing resistor switch | Realtime clock mode display selection     | On-chip power supply switch      | Display on/off                                  |
| LMR \$02D       | Input clock selection                 |                                           | Duty selection                   |                                                 |
| BMR \$02E       | Clock output on/off                   | Buzzer/clock selection                    | Buzzer/clock source selection    |                                                 |
| \$02F           | Not used                              |                                           |                                  |                                                 |
| DCD0 \$030      | PortD <sub>3</sub> DCR                | PortD <sub>2</sub> DCR                    | PortD <sub>1</sub> DCR           | PortD <sub>0</sub> DCR                          |
| DCD1 \$031      | PortD <sub>7</sub> DCR                | PortD <sub>6</sub> DCR                    | PortD <sub>5</sub> DCR           | PortD <sub>4</sub> DCR                          |
| DCD2 \$032      | PortD <sub>11</sub> DCR               | PortD <sub>10</sub> DCR                   | PortD <sub>9</sub> DCR           | PortD <sub>8</sub> DCR                          |
| \$033           | Not used                              |                                           |                                  |                                                 |
| DCR0 \$034      | PortR0 <sub>3</sub> DCR               | PortR0 <sub>2</sub> DCR                   | PortR0 <sub>1</sub> DCR          | PortR0 <sub>0</sub> DCR                         |
| DCR1 \$035      | PortR1 <sub>3</sub> DCR               | PortR1 <sub>2</sub> DCR                   | PortR1 <sub>1</sub> DCR          | PortR1 <sub>0</sub> DCR                         |
| DCR2 \$036      | PortR2 <sub>3</sub> DCR               | PortR2 <sub>2</sub> DCR                   | PortR2 <sub>1</sub> DCR          | PortR2 <sub>0</sub> DCR                         |
| DCR3 \$037      | PortR3 <sub>3</sub> DCR               | PortR3 <sub>2</sub> DCR                   | PortR3 <sub>1</sub> DCR          | PortR3 <sub>0</sub> DCR                         |
| DCR4 \$038      | PortR4 <sub>3</sub> DCR               | PortR4 <sub>2</sub> DCR                   | PortR4 <sub>1</sub> DCR          | PortR4 <sub>0</sub> DCR                         |
| DCR5 \$039      | PortR5 <sub>3</sub> DCR               | PortR5 <sub>2</sub> DCR                   | PortR5 <sub>1</sub> DCR          | PortR5 <sub>0</sub> DCR                         |
| DCR6 \$03A      | PortR6 <sub>3</sub> DCR               | PortR6 <sub>2</sub> DCR                   | PortR6 <sub>1</sub> DCR          | PortR6 <sub>0</sub> DCR                         |
| DCR7 \$03B      | PortR7 <sub>3</sub> DCR               | PortR7 <sub>2</sub> DCR                   | PortR7 <sub>1</sub> DCR          | PortR7 <sub>0</sub> DCR                         |
| DCR8 \$03C      | Not used                              |                                           | PortR8 <sub>1</sub> DCR          | PortR8 <sub>0</sub> DCR                         |
| \$03D           | Not used                              |                                           |                                  |                                                 |
| \$03E           | Not used                              |                                           |                                  |                                                 |
| \$03F           | Not used                              |                                           |                                  |                                                 |

**Figure 5 Special Function Register Area (cont)**

## HD404868 Series

| RAM address     | Bit 3                                 | Bit 2                                     | Bit 1                            | Bit 0                                           |
|-----------------|---------------------------------------|-------------------------------------------|----------------------------------|-------------------------------------------------|
| \$000           | Interrupt control bit area            |                                           |                                  |                                                 |
| \$003           |                                       |                                           |                                  |                                                 |
| SSR \$004       | 32 kHz oscillation stop setting       | 32 kHz frequency division ratio selection | System clock selection           | System clock frequency division ratio switching |
| MIS \$005       | Pull-up MOS control                   | Not used                                  | Interrupt frame period selection |                                                 |
| ESR \$006       | Not used                              |                                           | INT1 edge detection selection    |                                                 |
| \$007           | Not used                              |                                           |                                  |                                                 |
| PMR0 \$008      | Not used                              |                                           | D <sub>1</sub> /INT <sub>1</sub> | D <sub>0</sub> /INT <sub>0</sub>                |
| PMR1 \$009      | Not used                              | R0 <sub>2</sub> /WU <sub>2</sub>          | R0 <sub>1</sub> /WU <sub>1</sub> | R0 <sub>0</sub> /WU <sub>0</sub>                |
| PMR2 \$00A      | R1 <sub>3</sub> /TOB                  | R1 <sub>2</sub> /BUZZ                     | Not used                         | R1 <sub>0</sub> /EVNB                           |
| PMR3 \$00B      | R2 <sub>2</sub> /SI/SO                |                                           | R2 <sub>1</sub> /SCK             | R2 <sub>0</sub> /TOC                            |
| PMR4 \$00C      | R6/SEG13~16                           | R5/SEG9~12                                | R4/SEG5~8                        | R3/SEG1~4                                       |
| MSR1 \$00D      | Not used                              |                                           | Timer C clock on/off             | Timer B lock on/off                             |
| MSR2 \$00E      | Not used                              |                                           | A/D clock on/off                 | Serial clock on/off                             |
| TMA \$00F       | TimerA/Timer base                     | Timer A clock source selection            |                                  |                                                 |
| TMB1 \$010      | Reload on/off                         | Timer B clock source selection            |                                  |                                                 |
| TMB2 \$011      | Not used                              | Timer B output mode selection             | EVNB edge detection selection    |                                                 |
| TRBL/TWBL \$012 | Timer B register (lower)              |                                           |                                  |                                                 |
| TRBU/TWBU \$013 | Timer B register (upper)              |                                           |                                  |                                                 |
| TMC1 \$014      | Reload on/off                         | Timer C clock source selection            |                                  |                                                 |
| TMC2 \$015      | Not used                              | Timer C output mode selection             | Not used                         |                                                 |
| TRCL/TWCL \$016 | Timer C register (lower)              |                                           |                                  |                                                 |
| TRCU/TWCU \$017 | Timer C register (upper)              |                                           |                                  |                                                 |
| \$018           | Not used                              |                                           |                                  |                                                 |
| \$019           | Not used                              |                                           |                                  |                                                 |
| \$01A           | Not used                              |                                           |                                  |                                                 |
| \$01B           | Not used                              |                                           |                                  |                                                 |
| \$01C           | Not used                              |                                           |                                  |                                                 |
| \$01F           |                                       |                                           |                                  |                                                 |
| \$020           | Register flag area                    |                                           |                                  |                                                 |
| \$023           |                                       |                                           |                                  |                                                 |
| SMR1 \$024      | Serial transfer clock speed selection |                                           |                                  |                                                 |
| SMR2 \$025      | Not used                              | R2 <sub>2</sub> /SI/SO PMOS control       | SO idle H/L setting              | Not used                                        |
| SRL \$026       | Serial data register (lower)          |                                           |                                  |                                                 |
| SRU \$027       | Serial data register (upper)          |                                           |                                  |                                                 |
| AMR \$028       | Analog channel selection              |                                           |                                  | A/D conversion time                             |
| ADRL \$029      | A/D data register (lower)             |                                           | Not used                         |                                                 |
| ADRM \$02A      | A/D data register (middle)            |                                           |                                  |                                                 |
| ADRU \$02B      | A/D data register (upper)             |                                           |                                  |                                                 |
| LCR \$02C       | Power supply dividing resistor switch | Realtime clock mode display selection     | On-chip power supply switch      | Display on/off                                  |
| LMR \$02D       | Input clock selection                 |                                           | Duty selection                   |                                                 |
| BMR \$02E       | Clock output on/off                   | Buzzer/clock selection                    | Buzzer/clock source selection    |                                                 |
| \$02F           | Not used                              |                                           |                                  |                                                 |
| DCD0 \$030      | PortD <sub>3</sub> DCR                | PortD <sub>2</sub> DCR                    | PortD <sub>1</sub> DCR           | PortD <sub>0</sub> DCR                          |
| DCD1 \$031      | PortD <sub>7</sub> DCR                | PortD <sub>6</sub> DCR                    | PortD <sub>5</sub> DCR           | PortD <sub>4</sub> DCR                          |
| DCD2 \$032      | Not used                              |                                           | PortD <sub>9</sub> DCR           | PortD <sub>8</sub> DCR                          |
| \$033           | Not used                              |                                           |                                  |                                                 |
| DCR0 \$034      | Not used                              | PortR0 <sub>2</sub> DCR                   | PortR0 <sub>1</sub> DCR          | PortR0 <sub>0</sub> DCR                         |
| DCR1 \$035      | PortR1 <sub>3</sub> DCR               | PortR1 <sub>2</sub> DCR                   | PortR1 <sub>1</sub> DCR          | PortR1 <sub>0</sub> DCR                         |
| DCR2 \$036      | PortR2 <sub>3</sub> DCR               | PortR2 <sub>2</sub> DCR                   | PortR2 <sub>1</sub> DCR          | PortR2 <sub>0</sub> DCR                         |
| DCR3 \$037      | PortR3 <sub>3</sub> DCR               | PortR3 <sub>2</sub> DCR                   | PortR3 <sub>1</sub> DCR          | PortR3 <sub>0</sub> DCR                         |
| DCR4 \$038      | PortR4 <sub>3</sub> DCR               | PortR4 <sub>2</sub> DCR                   | PortR4 <sub>1</sub> DCR          | PortR4 <sub>0</sub> DCR                         |
| DCR5 \$039      | PortR5 <sub>3</sub> DCR               | PortR5 <sub>2</sub> DCR                   | PortR5 <sub>1</sub> DCR          | PortR5 <sub>0</sub> DCR                         |
| DCR6 \$03A      | PortR6 <sub>3</sub> DCR               | PortR6 <sub>2</sub> DCR                   | PortR6 <sub>1</sub> DCR          | PortR6 <sub>0</sub> DCR                         |
| DCR7 \$03B      | PortR7 <sub>3</sub> DCR               | PortR7 <sub>2</sub> DCR                   | PortR7 <sub>1</sub> DCR          | PortR7 <sub>0</sub> DCR                         |
| \$03C           | Not used                              |                                           |                                  |                                                 |
| \$03D           | Not used                              |                                           |                                  |                                                 |
| \$03E           | Not used                              |                                           |                                  |                                                 |
| \$03F           | Not used                              |                                           |                                  |                                                 |

Figure 5 Special Function Register Area (cont)

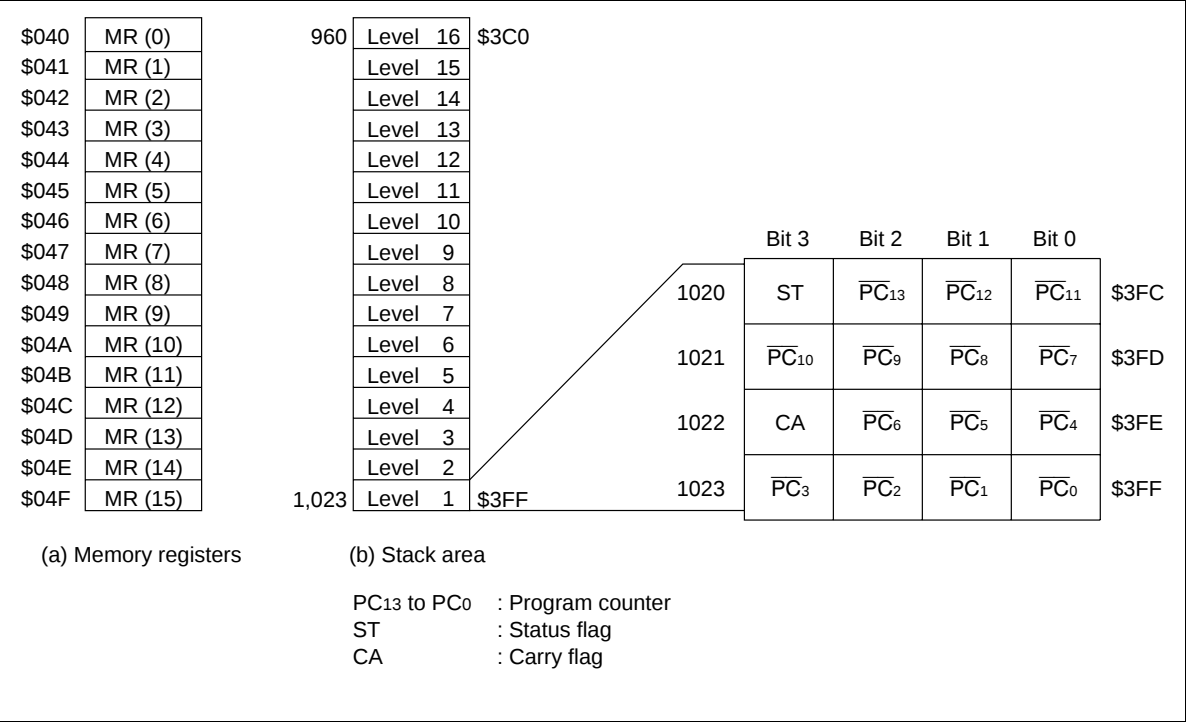


Figure 6 Configuration of Memory Registers and Stack Area, and Stack Position

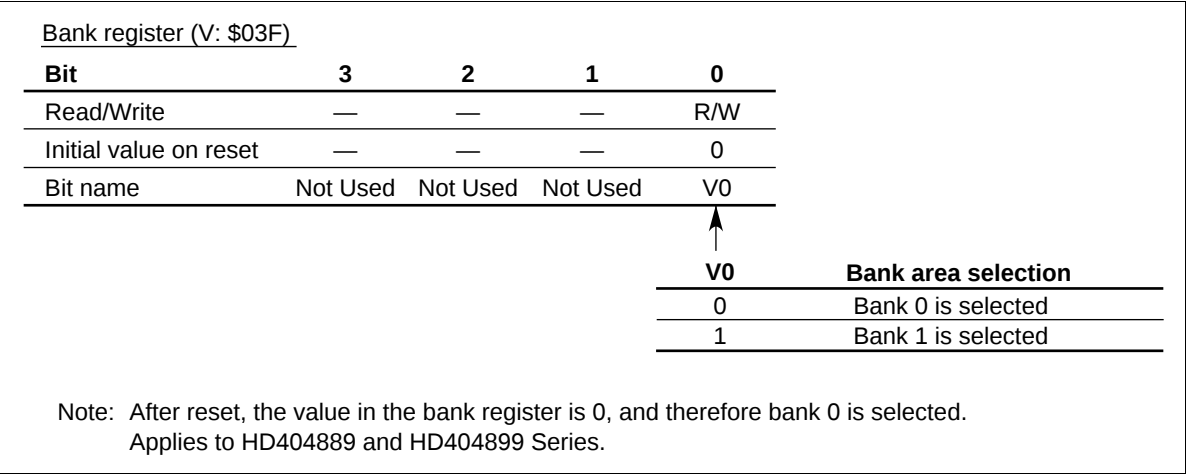


Figure 7 Bank Register (V)

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations. they are shown in figure 8 and described below.

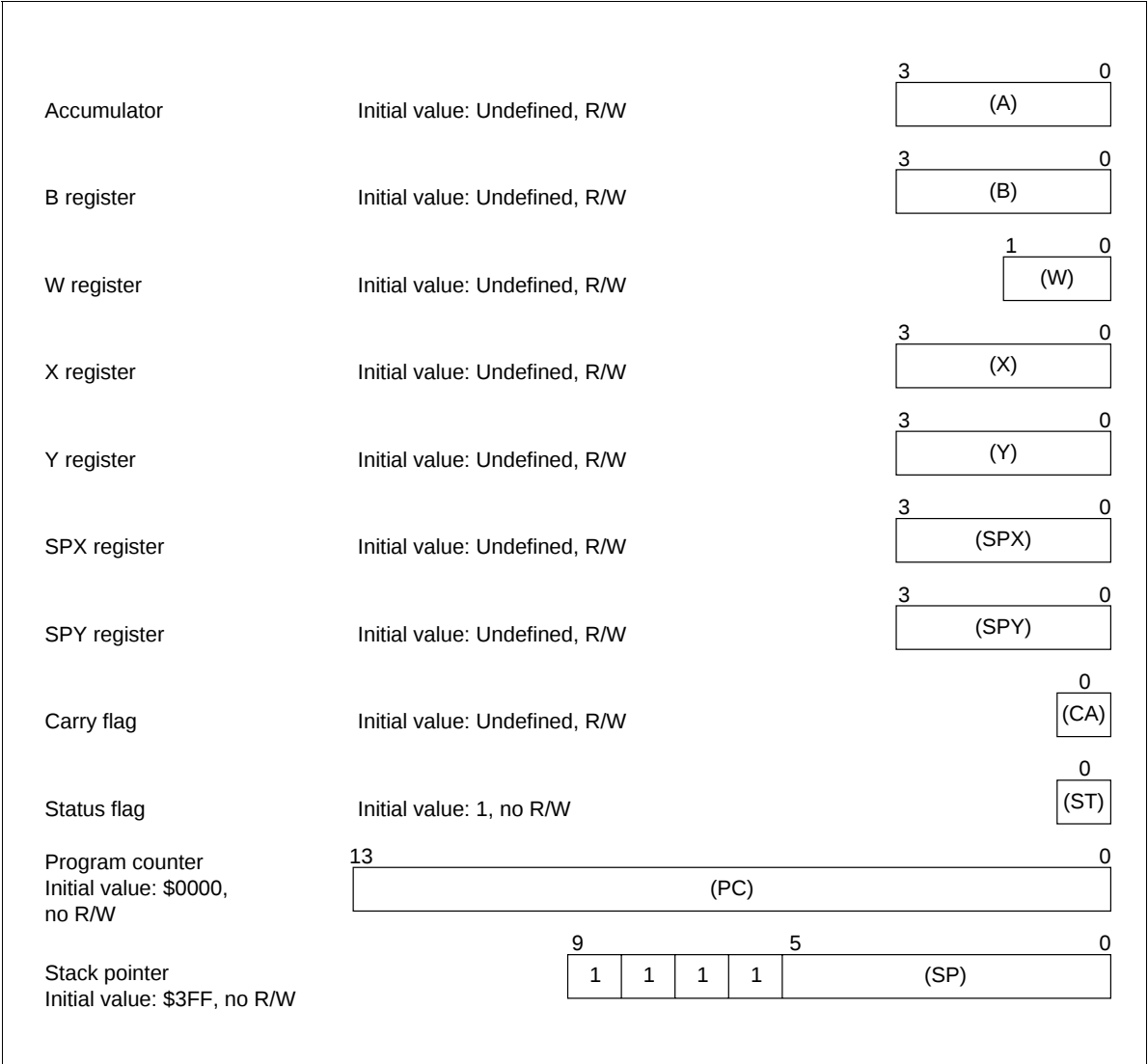


Figure 8 Registers and Flags

Accumulator (A) and B register (B):

The accumulator and B register are 4-bit registers used to hold the result of an ALU operation, and for data transfer to or from memory, an I/O area, or another register.

**W register (W), X register (X) and Y register (Y):**

The W register is a 2-bit register, and the X and Y registers are 4-bit registers, used for RAM register indirect addressing. The Y register is also used for D port addressing.

**SPX register (SPX) and SPY register (SPY):**

The SPX and SPY registers are 4-bit registers used as X register and Y register auxiliary registers, respectively.

**Carry flag (CA):**

This flag holds ALU overflow when an arithmetic/logic instruction is executed. It is also affected by the SEC, REC, ROTL, and ROTR instructions. The contents of the carry flag are saved to the stack when interrupt handling is performed, and are restored from the stack by the RTNI instruction (but are not affected by the RTN instruction).

**Status flag (ST):**

This flag holds ALU overflow when an arithmetic/logic or compare instruction is executed, and the result of an ALU non-zero or bit test instruction. It is used as the branch condition for the BR, BRL, CAL, and CALL instructions. The status flag is a latch-type flag, and does not change until the next arithmetic/logic, compare, or bit test instruction is executed. After a BR, BRL, CAL, or CALL instruction, the status flag is set to 1 regardless of whether the instruction is executed or skipped. The contents of the status flag are saved to the stack when interrupt handling is performed, and are restored from the stack by the RTNI instruction (but are not affected by the RTN instruction).

**Program counter (PC):**

This is a 14-bit binary counter that holds ROM address information.

**Stack pointer (SP):**

The stack pointer is a 10-bit register that holds the address of the next save space in the stack area. The stack pointer is initialized to \$3FF by an MCU reset. The stack pointer is decremented by 4 each time data is saved, and incremented by 4 each time data is restored. The upper 4 bits of the stack pointer are fixed at 1111, so that a maximum of 16 stack levels can be used.

There are two ways in which the stack pointer is initialized to \$3FF: by an MCU reset as mentioned above, or by resetting the RSP bit with the REM or REMD instruction.

**Reset**

An MCU reset is performed by driving the  $\overline{\text{RESET}}$  pin low. At power-on, and when subactive mode, watch mode, or stop mode is cleared,  $\overline{\text{RESET}}$  should be input for at least  $t_{RC}$  to provide the oscillation settling time for the oscillator. In other cases, the MCU is reset by inputting  $\overline{\text{RESET}}$  for at least two instruction cycles.

Table 1 shows the areas initialized by an MCU reset, and their initial values.

Table 1 (1) Initial Values after MCU Reset

| Item                  |                                | Abbr.                     | Initial value | Contents                                            |
|-----------------------|--------------------------------|---------------------------|---------------|-----------------------------------------------------|
| Program counter       |                                | (PC)                      | \$0000        | Program executed from ROM start address             |
| Status flag           |                                | (ST)                      | 1             | Branching by conditional branch instruction enabled |
| Stack pointer         |                                | (SP)                      | \$3FF         | Stack level is 0                                    |
| Interrupt flags/ mask | Interrupt enable flag          | (IE)                      | 0             | All interrupts disabled                             |
|                       | Interrupt request flag         | (IF)                      | 0             | No interrupt requests                               |
|                       | Interrupt mask                 | (IM)                      | 1             | Interrupt requests masked                           |
| I/O                   | Port data register             | (PDR)                     | All bits 1    | "1" level output possible                           |
|                       | Data control registers         | (DCD0 to 2)               | All bits 0    | Output buffer off (high impedance)                  |
|                       | Data control registers         | (DCR0 to 7, DCR80, DCR81) | All bits 0    |                                                     |
|                       | Port mode register 0           | (PMR0)                    | --00          | See port mode register 0 section                    |
|                       | Port mode register 1           | (PMR1)                    | 0000          | See port mode register 1 section                    |
|                       | Port mode register 2           | (PMR2)                    | 0000          | See port mode register 2 section                    |
|                       | Port mode register 3           | (PMR3)                    | 0000          | See port mode register 3 section                    |
|                       | Port mode register 4           | (PMR4)                    | 0000          | See port mode register 4 section                    |
|                       | Edge detection select register | (ESR)                     | --00          | See edge detection select register section          |
| Timers                | Timer mode register A          | (TMA)                     | 0000          | See timer mode register A section                   |
|                       | Timer mode register B1         | (TMB1)                    | 0000          | See timer mode register B1 section                  |
|                       | Timer mode register B2         | (TMB2)                    | -000          | See timer mode register B2 section                  |
|                       | Timer mode register C1         | (TMC1)                    | 0000          | See timer mode register C1 section                  |
|                       | Timer mode register C2         | (TMC2)                    | -0--          | See timer mode register C2 section                  |
|                       | Timer mode register D1         | (TMD1)                    | 0000          | See timer mode register D1 section                  |
|                       | Timer mode register D2         | (TMD2)                    | -000          | See timer mode register D2 section                  |
|                       | Prescaler S                    | (PSS)                     | \$000         |                                                     |
|                       | Prescaler W                    | (PSW)                     | \$00          |                                                     |
|                       | Timer/counter A                | (TCA)                     | \$00          |                                                     |
|                       | Timer/counter B                | (TCB)                     | \$00          |                                                     |
|                       | Timer/counter C                | (TCC)                     | \$00          |                                                     |
|                       | Timer/counter D                | (TCD)                     | \$00          |                                                     |
|                       | Timer write register B         | (TWBU,L)                  | \$X0          |                                                     |
|                       | Timer write register C         | (TWCU,L)                  | \$X0          |                                                     |
|                       | Timer write register D         | (TWDU,L)                  | \$X0          |                                                     |

**Table 1 (1) (cont) Initial Values after MCU Reset**

| Item             |                                     | Abbr.      | Initial value | Contents                                           |
|------------------|-------------------------------------|------------|---------------|----------------------------------------------------|
| Serial interface | Serial mode register 1              | (SMR1)     | 0000          | See serial mode register 1 section                 |
|                  | Serial mode register 2              | (SMR2)     | -0X-          | See serial mode register 2 section                 |
|                  | Serial data register                | (SRU,L)    | \$XX          |                                                    |
|                  | Octal counter                       |            | 000           |                                                    |
| A/D converter    | A/D mode register                   | (AMR)      | 0000          | See A/D mode register section                      |
|                  | A/D data register (HD404889 Series) | (ADRU,L)   | \$7F          | See A/D data register section                      |
|                  | A/D data register (HD404899 Series) | (ADRU,M,L) | \$1FF         | See A/D data register section                      |
| LCD              | LCD control register                | (LCR)      | 0000          | See LCD control register section                   |
|                  | LCD mode register                   | (LMR)      | 0000          | See LCD duty/clock control register section        |
| Bit registers    | Low speed on flag                   | (LSON)     | 0             | See low-power mode section                         |
|                  | Watchdog timer on flag              | (WDON)     | 0             | See timer C section                                |
|                  | A/D start flag                      | (ADSF)     | 0             | See A/D converter section                          |
|                  | Direct transfer on flag             | (DTON)     | 0             | See low-power mode section                         |
|                  | Input capture status flag           | (ICSF)     | 0             | See timer D section                                |
|                  | Input capture error flag            | (ICEF)     | 0             | See timer D section                                |
|                  | Gear enable flag                    | (GEF)      | 0             | See system clock gear function                     |
| Others           | Miscellaneous register              | (MIS)      | 0-00          | See low-power mode and input/output sections       |
|                  | System clock select register        | (SSR)      | 0000          | See low-power mode and oscillator circuit sections |
|                  | Module standby register 1           | (MSR1)     | -000          | See timer section                                  |
|                  | Module standby register 2           | (MSR2)     | --00          | See serial interface and A/D converter sections    |
|                  | Buzzer mode register                | (BMR)      | 0000          | See Buzzer mode register section                   |

- Notes: 1. The state of registers and flags other than those listed above after an MCU reset is shown in table 1 (2).
2. X: Indicates invalid value, - indicates that the bit does not exist.

Table 1 (2) Initial Values after MCU Reset

| Item           | Abbr.   | After Stop Mode Clearance by $\overline{WU}_0$ to $\overline{WU}_3$ Input | After Other MCU Reset                                                                   |
|----------------|---------|---------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| Carry flag     | (CA)    | Retain value immediately prior to entering stop mode                      | Value immediately prior to MCU reset is not guaranteed. Must be initialized by program. |
| Accumulator    | (A)     |                                                                           |                                                                                         |
| B register     | (B)     |                                                                           |                                                                                         |
| W register     | (W)     |                                                                           |                                                                                         |
| X/SPX register | (X/SPX) |                                                                           |                                                                                         |
| Y/SPY register | (Y/SPY) |                                                                           |                                                                                         |
| RAM            |         |                                                                           |                                                                                         |

Interrupts

There are a total of nine interrupt sources, comprising wakeup input ( $\overline{WU}_0$  to  $\overline{WU}_3$ ), external interrupts ( $\overline{INT}_0$ ,  $INT_1$ ), timer/counter (timer A, timer B, timer C, timer D) interrupts, a serial interface interrupt, and an A/D converter interrupt.

Each interrupt source is provided with an interrupt request flag, interrupt mask, and vector address, used for storing and controlling interrupt requests. In addition, an interrupt enable flag is provided to control interrupts as a whole.

Of the interrupt sources, timers B and D share the same vector address, and the A/D converter and serial interface also share the same vector address. Software must therefore determine which of the interrupt sources is requesting an interrupt at the start of interrupt handling.

Interrupt control bits and interrupt handling:

The interrupt control bits are mapped onto RAM addresses \$000 to \$003 and \$022 to \$023, and can be accessed by RAM bit manipulation instructions. However, the interrupt request flags (IF) cannot be set by software. When the MCU is reset, the interrupt enable flag (IE) and interrupt request flags (IF) are initialized to 0, and the interrupt masks (IM) are initialized to 1.

Figure 9 shows a block diagram of the interrupt control circuit, table 2 shows interrupt priorities and vector addresses, and table 3 lists the conditions for executing interrupt handling for each of the nine kinds of interrupt source. When the interrupt request flag is set to 1 and the interrupt mask is cleared to 0, an interrupt is requested. If the interrupt enable flag is set to 1 at this time, interrupt handling is started. The vector address corresponding to the interrupt source is generated by the priority control circuit.

The interrupt handling sequence is shown in figure 10, and the interrupt handling flowchart in figure 11. When an interrupt is accepted, execution of the previous instruction is completed in the first cycle. In the second cycle, the interrupt enable flag (IE) is reset. In the second and third cycles, the contents of the carry flag, status flag, and program counter are saved on the stack. In the third cycle, a jump is made to the vector address and instruction execution is resumed from that address.

In each vector address area, a JMPL instruction should be written that branches to the start address of the interrupt routine. In the interrupt routine, the interrupt request flag that caused interrupt handling must be reset by software.

Table 2      Vector Addresses and Interrupt Priorities

| Interrupt Source                       | Priority | Vector Address |
|----------------------------------------|----------|----------------|
| RESET                                  | —        | \$0000         |
| $\overline{WU}_0$ to $\overline{WU}_3$ | 1        | \$0002         |
| $\overline{INT}_0$                     | 2        | \$0004         |
| $INT_1$                                | 3        | \$0006         |
| Timer A                                | 4        | \$0008         |
| Timer B, D                             | 5        | \$000A         |
| Timer C                                | 6        | \$000C         |
| Serial interface, A/D converter        | 7        | \$000E         |

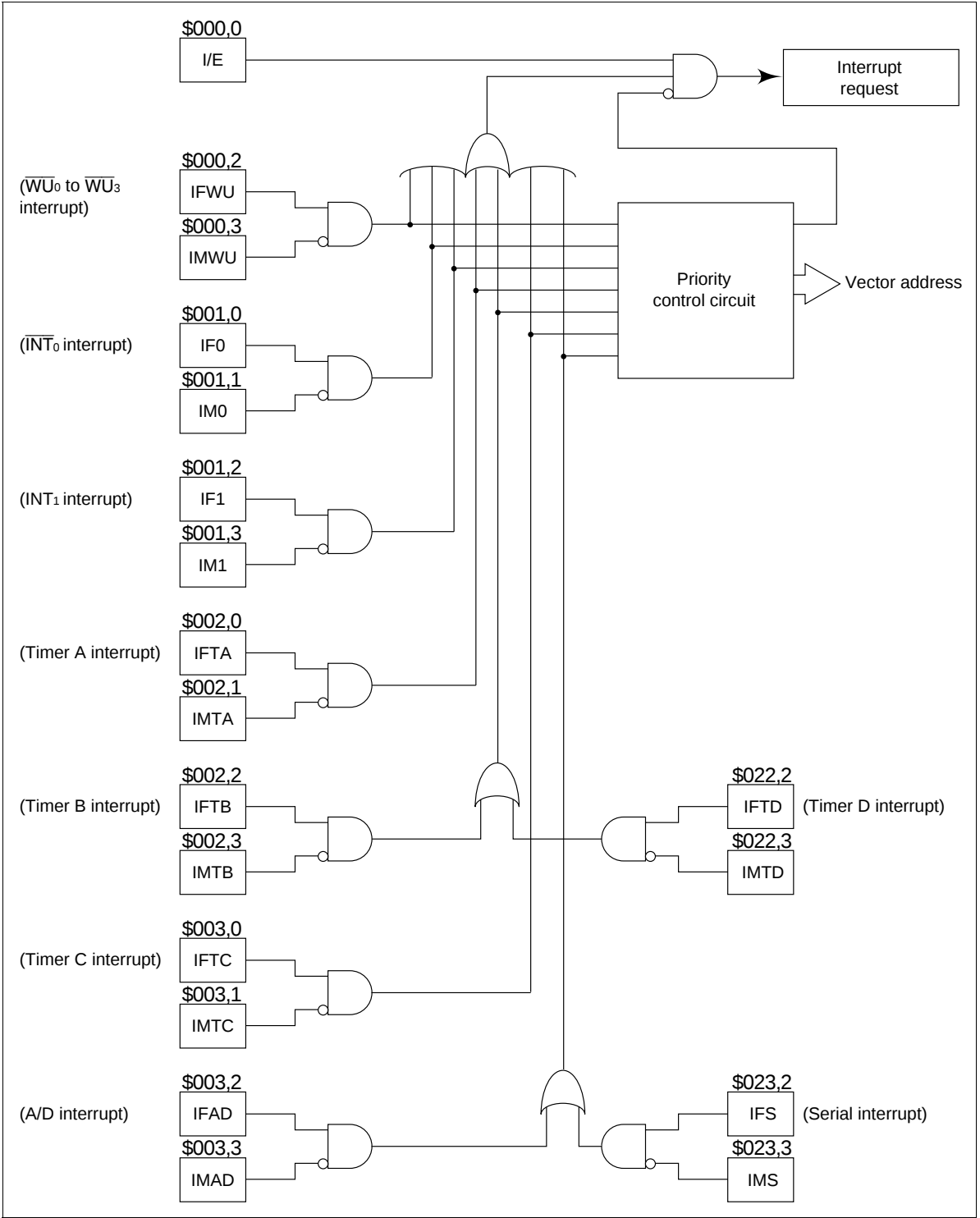


Figure 9 Block Diagram of Interrupt Control Circuit

Table 3 Interrupt Processing and Activation Conditions

| Interrupt Control Bit                            | Interrupt Source                       |                    |         |         |                       |         |                  |
|--------------------------------------------------|----------------------------------------|--------------------|---------|---------|-----------------------|---------|------------------|
|                                                  | $\overline{WU}_0$ to $\overline{WU}_3$ | $\overline{INT}_0$ | $INT_1$ | Timer A | Timer B or<br>Timer D | Timer C | A/D or<br>Serial |
| IE                                               | 1                                      | 1                  | 1       | 1       | 1                     | 1       | 1                |
| IFWU· $\overline{IMWU}$                          | 1                                      | 0                  | 0       | 0       | 0                     | 0       | 0                |
| IF0· $\overline{IM0}$                            | *                                      | 1                  | 0       | 0       | 0                     | 0       | 0                |
| IF1· $\overline{IM1}$                            | *                                      | *                  | 1       | 0       | 0                     | 0       | 0                |
| IFTA· $\overline{IMTA}$                          | *                                      | *                  | *       | 1       | 0                     | 0       | 0                |
| IFTB· $\overline{IMTB}$ +IFTD· $\overline{IMTD}$ | *                                      | *                  | *       | *       | 1                     | 0       | 0                |
| IFTC· $\overline{IMTC}$                          | *                                      | *                  | *       | *       | *                     | 1       | 0                |
| IFAD· $\overline{IMAD}$ +IFS· $\overline{IMS}$   | *                                      | *                  | *       | *       | *                     | *       | 1                |

Note: \* Operation is not affected whether the value is 0 or 1.

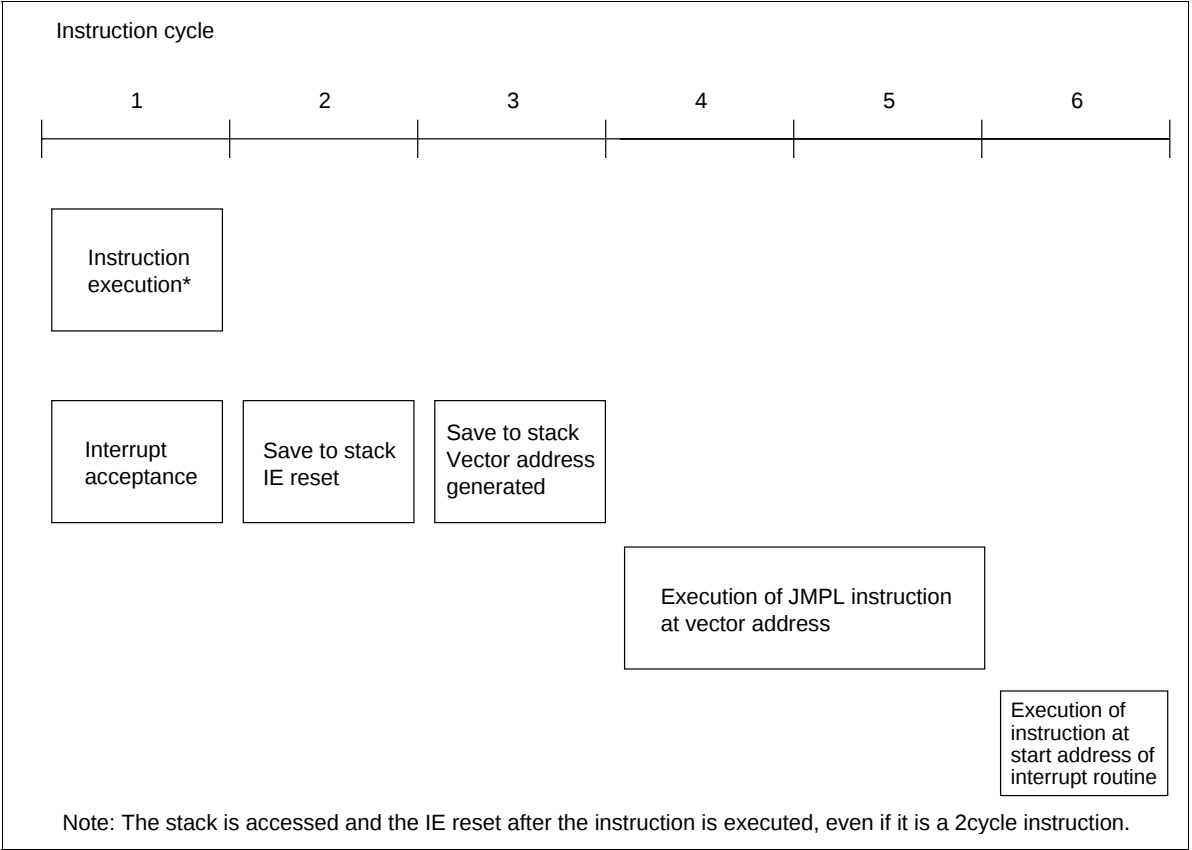


Figure 10 Interrupt Sequence

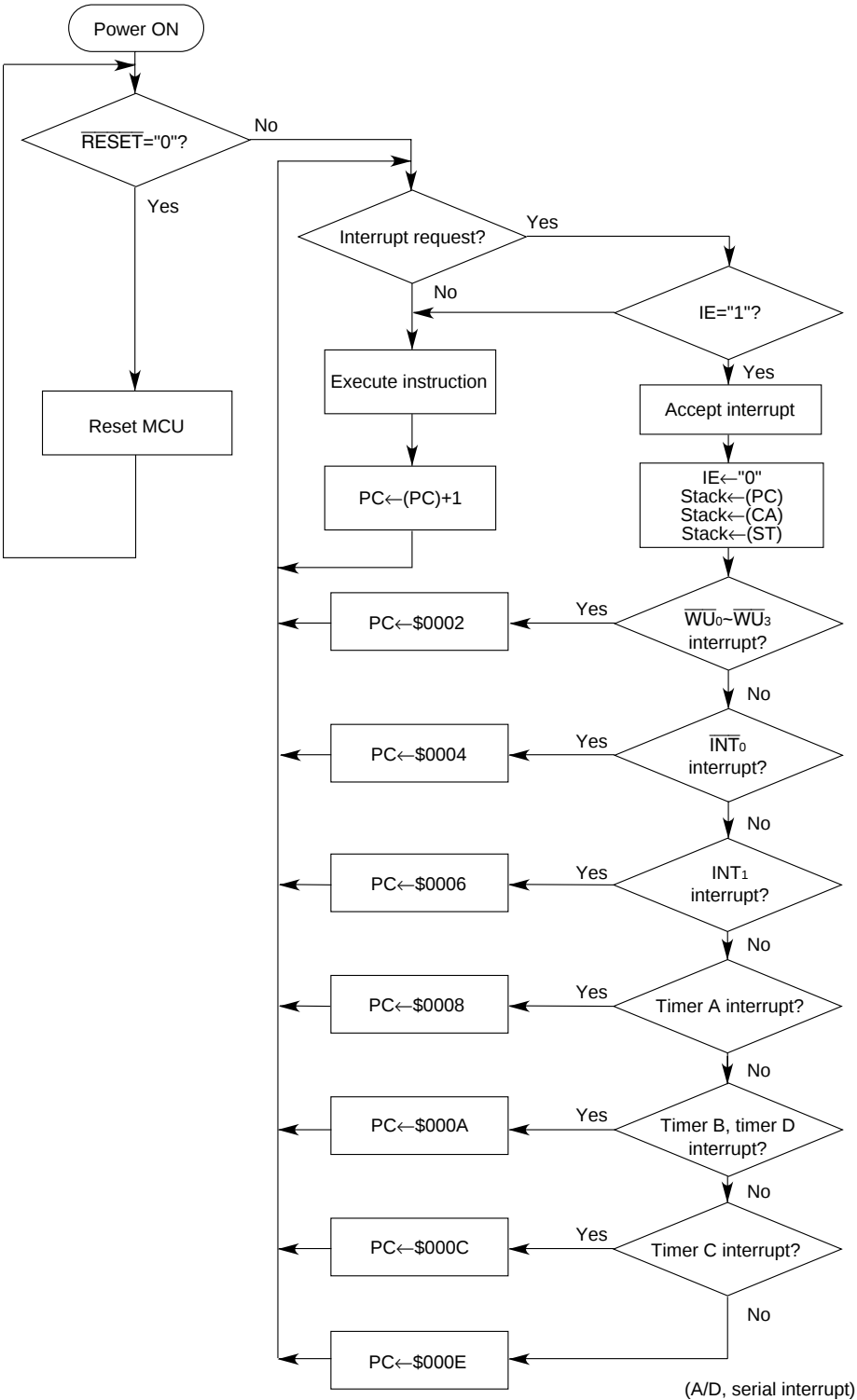


Figure 11 Interrupt Handling Flowchart

**Interrupt enable flag (IE: \$000,0):**

The interrupt enable flag controls interrupt enabling/disabling of all interrupt requests as shown in table 4. The interrupt enable flag is reset by interrupt handling and set by the RTNI instruction.

**Table 4      Interrupt Enable Flag (IE: \$000,0)**

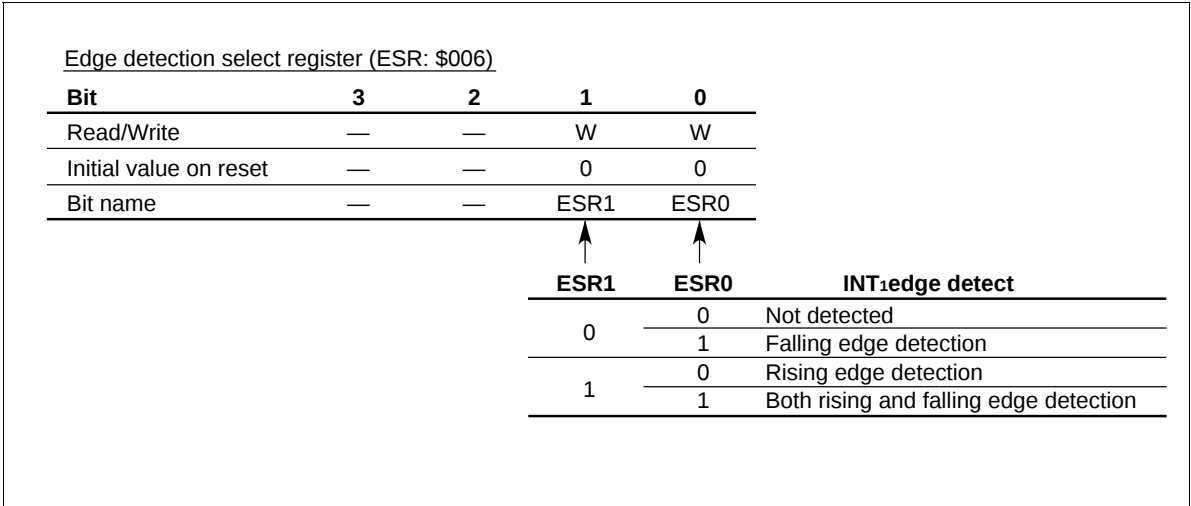
| Interrupt Enable Flag(IE) | Interrupt Enabling/Disabling |
|---------------------------|------------------------------|
| 0                         | Interrupts disabled          |
| 1                         | Interrupts enabled           |

**Wakeup interrupt request flag (IFWU: \$000,2):**

The wakeup interrupt request flag (IFWU) is set by the detection of a falling edge in  $\overline{WU}_0$  to  $\overline{WU}_3$  input in active mode, subactive mode, watch mode, or standby mode. In stop mode, when a falling edge is detected at the wakeup pin, the MCU waits for the oscillation settling time, then switches to active mode. The wakeup interrupt request flag (IFWU) is not set in this case.

**Wakeup interrupt mask (IMWU: \$000,3):**

This bit masks an interrupt request by the wakeup interrupt request flag.



**Figure 12   Edge Detection Select Register (ESR)**

**External interrupt request flags (IF0, IF1: \$001):**

IF0 is set by a falling edge in the  $\overline{\text{INT}}_0$  input, and IF1 is set by a rising edge, falling edge, or both edges in the  $\text{INT}_1$  input (table 5).

Interrupt edge selection is performed by means of the edge detection select register (ESR: \$006) (figure 12).

**Table 5 External Interrupt Request Flags (IF0, IF1: \$001)**

| External Interrupt Request Flags<br>(IF0, IF1) | Interrupt Request                    |
|------------------------------------------------|--------------------------------------|
| 0                                              | No external interrupt request        |
| 1                                              | External interrupt request generated |

**External interrupt masks (IM0, IM1: \$001):**

These bits mask interrupt requests by the external interrupt request flags (table 6).

**Table 6 External Interrupt Mask (IM: \$001)**

| External Interrupt Masks<br>(IM0, IM1) | Interrupt Request                                |
|----------------------------------------|--------------------------------------------------|
| 0                                      | External interrupt request enabled               |
| 1                                      | External interrupt request masked (held pending) |

**Timer A interrupt request flag (IFTA: \$002,0):**

The timer A interrupt request flag is set by timer A overflow output (table 7).

**Table 7 Timer A Interrupt Request Flag (IFTA: \$002,0)**

| Timer A Interrupt Request<br>Flag(IFTA) | Interrupt Request                   |
|-----------------------------------------|-------------------------------------|
| 0                                       | No timer A interrupt request        |
| 1                                       | Timer A interrupt request generated |

**Timer A interrupt mask (IMTA: \$002,1):**

This bit masks an interrupt request by the timer A interrupt request flag (table 8).

**Table 8 Timer A Interrupt Mask (IMTA: \$002,1)**

| Timer A Interrupt Mask (IMTA) | Interrupt Request                               |
|-------------------------------|-------------------------------------------------|
| 0                             | Timer A interrupt request enabled               |
| 1                             | Timer A interrupt request masked (held pending) |

**Timer B interrupt request flag (IFTB: \$002,2):**

The timer B interrupt request flag is set by timer B overflow output (table 9).

**Table 9      Timer B Interrupt Request Flag (IFTB: \$002,2)**

| Timer B Interrupt Request Flag (IFTB) | Interrupt Request                   |
|---------------------------------------|-------------------------------------|
| 0                                     | No timer B interrupt request        |
| 1                                     | Timer B interrupt request generated |

**Timer B interrupt mask (IMTB: \$002,3):**

This bit masks an interrupt request by the timer B interrupt request flag (table 10).

**Table 10     Timer B Interrupt Mask (IMTB: \$002,3)**

| Timer B Interrupt Mask (IMTB) | Interrupt Request                               |
|-------------------------------|-------------------------------------------------|
| 0                             | Timer B interrupt request enabled               |
| 1                             | Timer B interrupt request masked (held pending) |

**Timer C interrupt request flag (IFTC: \$003,0):**

The timer C interrupt request flag is set by timer C overflow output (table 11).

**Table 11     Timer C Interrupt Request Flag (IFTC: \$003,0)**

| Timer C Interrupt Request Flag (IFTC) | Interrupt Request                                  |
|---------------------------------------|----------------------------------------------------|
| 0                                     | No timer C interrupt request                       |
| 1                                     | Timer C interrupt request generated (held pending) |

**Timer C interrupt mask (IMTC: \$003,1):**

This bit masks an interrupt request by the timer C interrupt request flag (table 12).

**Table 12     Timer C Interrupt Mask (IMTC: \$003,1)**

| Timer C Interrupt Mask (IMTC) | Interrupt Request                               |
|-------------------------------|-------------------------------------------------|
| 0                             | Timer C interrupt request enabled               |
| 1                             | Timer C interrupt request masked (held pending) |

**Timer D interrupt request flag (IFTD: \$022,2): (Applies to HD404889, HD404899, and HD404878 Series)**

The timer D interrupt request flag is set by timer D overflow output, or by an EVND input edge when used as an input capture timer (table 13).

**Table 13     Timer D Interrupt Request Flag (IFTD: \$022,2)**

| Timer D Interrupt Request Flag (IFTD) | Interrupt Request                   |
|---------------------------------------|-------------------------------------|
| 0                                     | No timer D interrupt request        |
| 1                                     | Timer D interrupt request generated |

**Timer D interrupt mask (IMTD: \$022,3): (Applies to HD404889, HD404899, and HD404878 Series)**

This bit masks an interrupt request by the timer D interrupt request flag (table 14).

**Table 14     Timer D Interrupt Mask (IMTD: \$022,3)**

| Timer D Interrupt Mask (IMTD) | Interrupt Request                               |
|-------------------------------|-------------------------------------------------|
| 0                             | Timer D interrupt request enabled               |
| 1                             | Timer D interrupt request masked (held pending) |

**Serial interrupt request flag (IFS: \$023,2):**

The serial interrupt request flag is set on completion of serial data transfer, or if data transfer is halted midway (table 15).

**Table 15     Serial Interrupt Request Flag (IFS: \$023,2)**

| Serial Interrupt Request Flag (IFS) | Interrupt Request                  |
|-------------------------------------|------------------------------------|
| 0                                   | No serial interrupt request        |
| 1                                   | Serial interrupt request generated |

**Serial interrupt mask (IMS: \$023,3):**

This bit masks an interrupt request by the serial interrupt request flag (table 16).

**Table 16     Serial Interrupt Mask (IMS: \$023,3)**

| Serial Interrupt Mask (IMS) | Interrupt Request                              |
|-----------------------------|------------------------------------------------|
| 0                           | Serial interrupt request enabled               |
| 1                           | Serial interrupt request masked (held pending) |

**A/D interrupt request flag (IFAD: \$003,2): (Applies to HD404889, HD404899, and HD404868 Series)**  
The A/D interrupt request flag is set on completion of A/D conversion (table 17).

**Table 17     A/D Interrupt Request Flag (IFAD: \$003,2)**

| A/D Interrupt Request Flag (IFAD) | Interrupt Request               |
|-----------------------------------|---------------------------------|
| 0                                 | No A/D interrupt request        |
| 1                                 | A/D interrupt request generated |

**A/D interrupt mask (IMAD: \$003,3): (Applies to HD404889, HD404899, and HD404868 Series)**  
This bit masks an interrupt request by the A/D interrupt request flag (table 18).

**Table 18     A/D Interrupt Mask (IMAD: \$003,3)**

| Serial Interrupt Mask (IMAD) | Interrupt Request                           |
|------------------------------|---------------------------------------------|
| 0                            | A/D interrupt request enabled               |
| 1                            | A/D interrupt request masked (held pending) |

Operating Modes

The five operating modes shown in table 19 can be used for the MCU.

The function of each mode is shown in table 20, and the state transition diagram among each mode in figure 13.

Table 19     Operating Modes and Clock Status

|                     |                      | Mode Name                                                                                                                                                                                                      |                                         |                                                                    |                                                                                                                        |                                                                                                                      |
|---------------------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|--------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|
|                     |                      | Active                                                                                                                                                                                                         | Standby                                 | Stop                                                               | Watch                                                                                                                  | Subactive*2                                                                                                          |
| Activation method   |                      | RESET<br>cancellation,<br>interrupt<br>request, $\overline{WU}_0$<br>to $\overline{WU}_3$ input<br>in stop mode<br>STOP/SBY<br>instruction in<br>subactive<br>mode (when<br>direct<br>transfer is<br>selected) | SBY<br>instruction                      | STOP<br>instruction<br>when<br>TMA3 = 0                            | STOP<br>instruction<br>when<br>TMA3 = 1                                                                                | $\overline{INT}_0$ /timer A<br>or $\overline{WU}_0$ to<br>$\overline{WU}_3$<br>interrupt<br>request in<br>watch mode |
| Status              | System oscillator    | OP                                                                                                                                                                                                             | OP                                      | Stopped                                                            | Stopped                                                                                                                | Stopped                                                                                                              |
|                     | Subsystem oscillator | OP                                                                                                                                                                                                             | OP                                      | OP *1                                                              | OP                                                                                                                     | OP                                                                                                                   |
| Cancellation method |                      | RESET<br>input,<br>STOP/SBY<br>instruction                                                                                                                                                                     | RESET<br>input,<br>interrupt<br>request | RESET<br>input,<br>$\overline{WU}_0$ to $\overline{WU}_3$<br>input | RESET<br>input,<br>$\overline{INT}_0$ /timer A<br>or $\overline{WU}_0$ to<br>$\overline{WU}_3$<br>interrupt<br>request | RESET<br>input,<br>STOP/SBY<br>instruction                                                                           |

Notes: OP: implies in operation.

- 1. Operating or stopping the oscillator can be selected by setting bit 3 of the system clock select register (SSR: \$004)
- 2. Subactive mode is an optional function; specify it on the fnction option list.

**Table 20     Operation in Low-Power Dissipation Modes**

| Function               | Stop Mode              | Watch mode             | Standby Mode | Subactive Mode* <sup>3</sup> |
|------------------------|------------------------|------------------------|--------------|------------------------------|
| CPU                    | Retained               | Retained               | Retained     | OP                           |
| RAM                    | Retained               | Retained               | Retained     | OP                           |
| Timer A                | Stopped                | OP                     | OP           | OP                           |
| Timer B                | Stopped                | Stopped                | OP           | OP                           |
| Timer C                | Stopped                | Stopped                | OP           | OP                           |
| Timer D * <sup>4</sup> | Stopped                | Stopped                | OP           | OP                           |
| Serial interface       | Stopped * <sup>1</sup> | Stopped * <sup>1</sup> | OP           | OP                           |
| A/D * <sup>5</sup>     | Stopped                | Stopped                | OP           | Stopped                      |
| LCD                    | Stopped                | OP * <sup>2</sup>      | OP           | OP                           |
| I/O                    | Retained               | Retained               | Retained     | OP                           |

Notes: OP: implies in operation.

1. Transmission/Reception is activated if a clock is input in external clock mode. However, interrupts stop.
2. When a 32 kHz clock source is used.
3. Subactive mode is an optional function specified on the function option list.
4. Applies to HD404889, HD404899, and HD404878 Series.
5. Applies to HD404889, HD404899, and HD404868 Series.

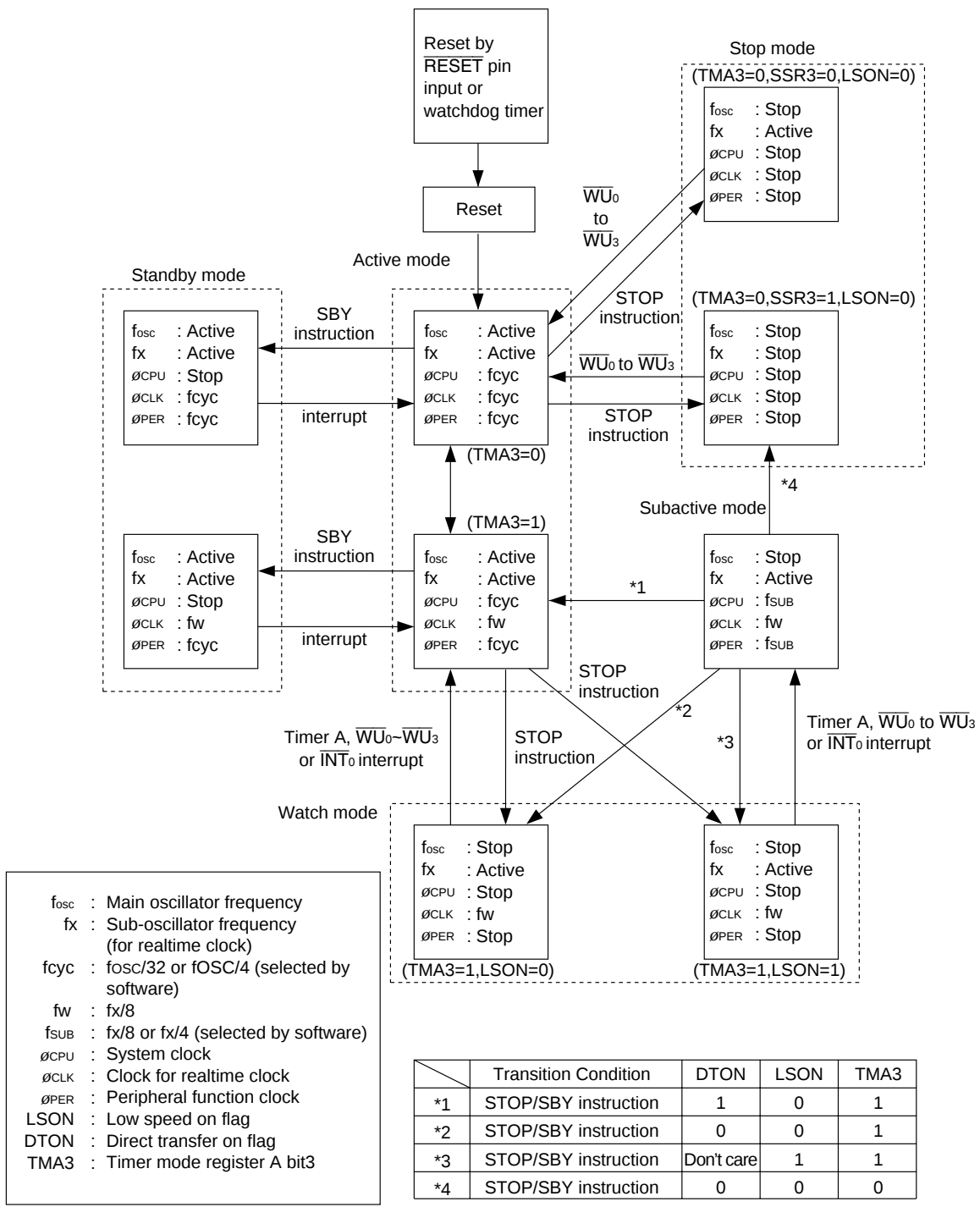


Figure 13 MCU Status Transitions

**Active mode:**

In active mode all functions operate. In this mode, the MCU operates on clocks generated by the OSC<sub>1</sub> and OSC<sub>2</sub> oscillator circuits.

**Standby mode:**

In standby mode the oscillators continue to operate but clocks relating to instruction execution halt. As a result, CPU operation stops, and registers, RAM, and the D port/R port set for output retain their state immediately prior to entering standby mode. Interrupts, timers, the serial interface, and other peripheral functions continue to operate.

Power consumption is lower than in active mode due to the halting of the CPU.

The MCU is switched to standby mode by executing the SBY instruction in active mode. Standby mode is cleared by  $\overline{\text{RESET}}$  input or an interrupt request. When standby mode is cleared by  $\overline{\text{RESET}}$  input, an MCU reset is performed. When standby mode is cleared by an interrupt request, the MCU enters active mode and executes a instruction following the SBY instruction. After executing the instruction, if the interrupt enable flag is set to 1, interrupt handling is executed; if the interrupt enable flag is cleared to 0, the interrupt request is held pending and normal instruction execution is continued.

MCU operation flowchart is shown in figure 14.

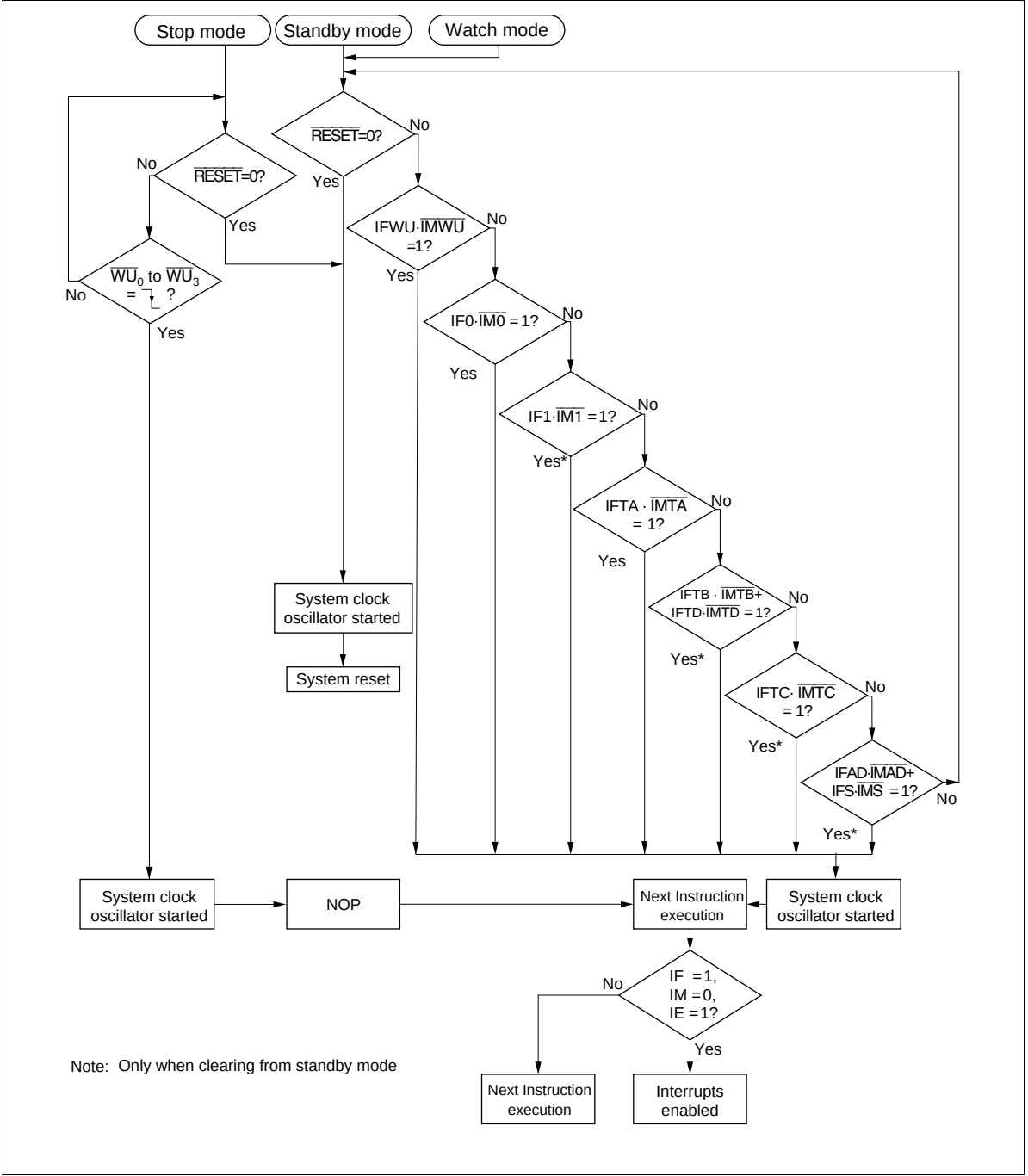


Figure 14 MCU Operation Flowchart

### Stop mode:

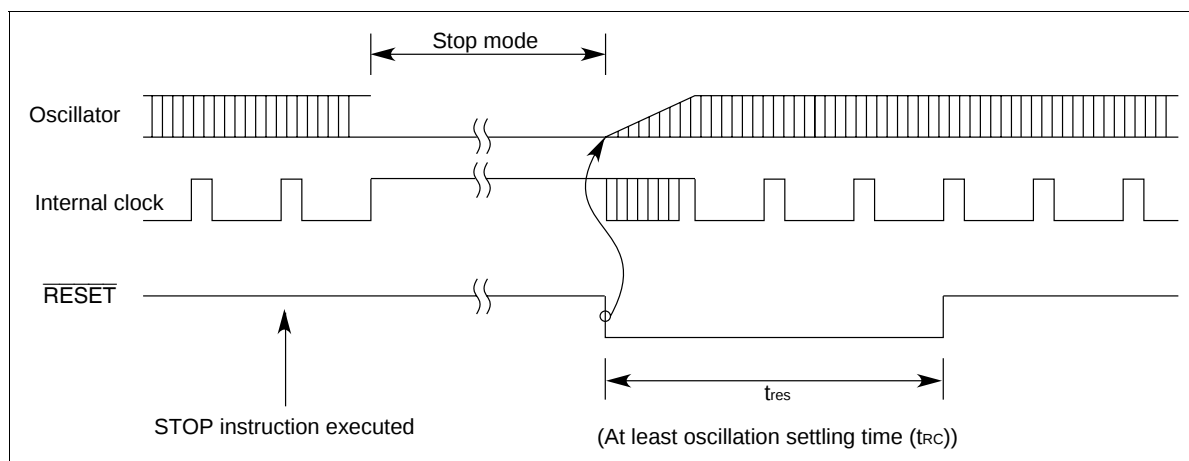
In stop mode, all MCU function stop except that states prior to entry into stop mode are retained. This mode thus has the lowest power consumption of all operating mode.

In stop mode, the  $OSC_1$  and  $OSC_2$  oscillators stop. Bit 3 (SSR3) of the system clock select register (SSR: \$004) (figure 24) can be used to select the active (= 0) or stopped (= 1) state for the X1 and X2 oscillators.

The MCU is switched to stop mode by executing a STOP instruction while bit 3 (TMA3) of timer mode register A (TMA: \$00F) is cleared to 0 in active mode. Stop mode is cleared by  $\overline{RESET}$  or  $\overline{WU}_0$  to  $\overline{WU}_3$  input. When stop mode is cleared by  $\overline{RESET}$ , the RESET signal should be input for at least the oscillation settling time ( $t_{RC}$ ) (see "AC Characteristics") shown in figure 15. Then, the MCU is initialized and starts instruction execution from the start (address 0) of the program.

When the MCU detects a falling edge at  $\overline{WU}_0$  to  $\overline{WU}_3$  in stop mode, it automatically waits for the oscillation settling time, then switches to active mode. After the transition to active mode, the MCU resumes program execution from the instruction following the STOP instruction.

If stop mode is cleared by wakeup input, RAM data and registers retain their values prior to entering stop mode.



**Figure 15 Timing Chart for Clearing Stop Mode by RESET Input**

Note: If stop mode is cleared by wakeup input when an external clock is used as the system clock ( $OSC_1$ ), the subclock should not be stopped in stop mode.

### Watch mode:

In watch mode, the realtime clock function (timer A) and LCD function using the X1 and X2 oscillators operate, but other functions stop. This mode thus has the second lowest power consumption after stop mode, and is useful for performing realtime clock display only.

In watch mode, the  $OSC_1$  and  $OSC_2$  oscillators stop but the X1 and X2 oscillators continue to operate.

The MCU is switched to watch mode by executing a STOP instruction while TMA3 = 1 in active mode, or by executing a STOP/SBY instruction in subactive mode.

Watch mode is cleared by  $\overline{\text{RESET}}$  input or an  $\overline{\text{INT}}_0$ , timer A or  $\overline{\text{WU}}_0$  to  $\overline{\text{WU}}_3$  interrupt request. For  $\overline{\text{RESET}}$  input, refer to the section on stop mode. When watch mode is cleared by an  $\overline{\text{INT}}_0$ , timer A or  $\overline{\text{WU}}_0$  to  $\overline{\text{WU}}_3$  interrupt request, the mode transition depends on the value of the LSON bit: the MCU enters active mode if LSON = 0, and enters subactive mode if LSON = 1. In the case of a transition to active mode, interrupt request generation is delayed to secure the oscillation settling time: the delay is the tRC set time for the timer A interrupt, and, for the  $\overline{\text{INT}}_0$  interrupt or  $\overline{\text{WU}}_0$  to  $\overline{\text{WU}}_3$  interrupt,  $T_x (T + t_{\text{RC}} < T_x < 2T + t_{\text{RC}})$  if bit 1 and 0 (MIS1, MIS0) of the miscellaneous register are set to 00, or  $T_x (t_{\text{RC}} < T_x < T + t_{\text{RC}})$  if MIS1 and MIS0 are set to 01 or 10 (figures 16 and 17). Other operations when the transition is made are the same as when watch mode is cleared (figure 14).

#### **Subactive mode:**

In subactive mode, the OSC<sub>1</sub> and OSC<sub>2</sub> oscillator circuits stop and the MCU operates on clocks generated by the X1 and X2 oscillator circuits. In this mode, functions other than the A/D converter operate, but since the operating clocks are slow, power consumption is the lowest after watch mode.

A CPU instruction processing speed of 244  $\mu\text{s}$  or 122  $\mu\text{s}$  can be selected according to whether bit 2 (SSR2) of the system clock select register (SSR: \$004) is set to 1 or cleared to 0. The value of the SSR2 bit should be changed (0→1 or 1→0) only in active mode. If the value is changed in subactive mode, the MCU may operate incorrectly.

Subactive mode is cleared by executing a STOP/SBY instruction. A transition is then made to either watch mode or active mode according to the value of the low speed on flag (LSON: \$020,0) and the direct transfer on flag (DTON: \$020,3).

Subactive mode is a function option, and should be specified in the function option list.

#### **Interrupt frame:**

In watch mode and subactive mode,  $\phi_{\text{CLK}}$  is supplied to the timer A,  $\overline{\text{WU}}_0$  to  $\overline{\text{WU}}_3$ , and  $\overline{\text{INT}}_0$  acceptance circuits. Prescaler W and timer A operate as time bases, and generate interrupt frame timing. Either of two values can be selected for the interrupt frame period, T, by means of the miscellaneous register (MIS: \$005) (figure 17).

In watch mode and subactive mode, the timing for generation of timer A,  $\overline{\text{INT}}_0$  and  $\overline{\text{WU}}_0$  to  $\overline{\text{WU}}_3$  interrupts is synchronized with the interrupt frame. Except for the case of an active mode transition, the interrupt strobe timing is used for interrupt request generation. Timer A generates overflow and interrupt requests at the interrupt strobe timing.

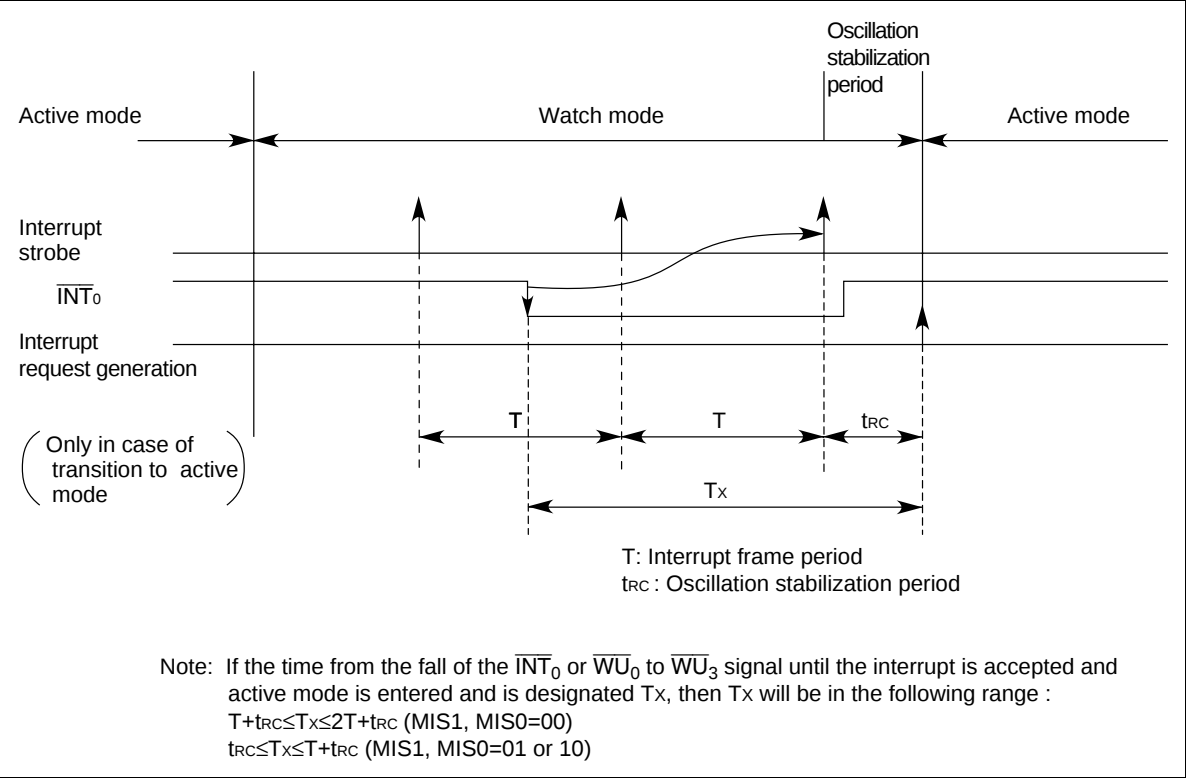


Figure 16 Interrupt Frame

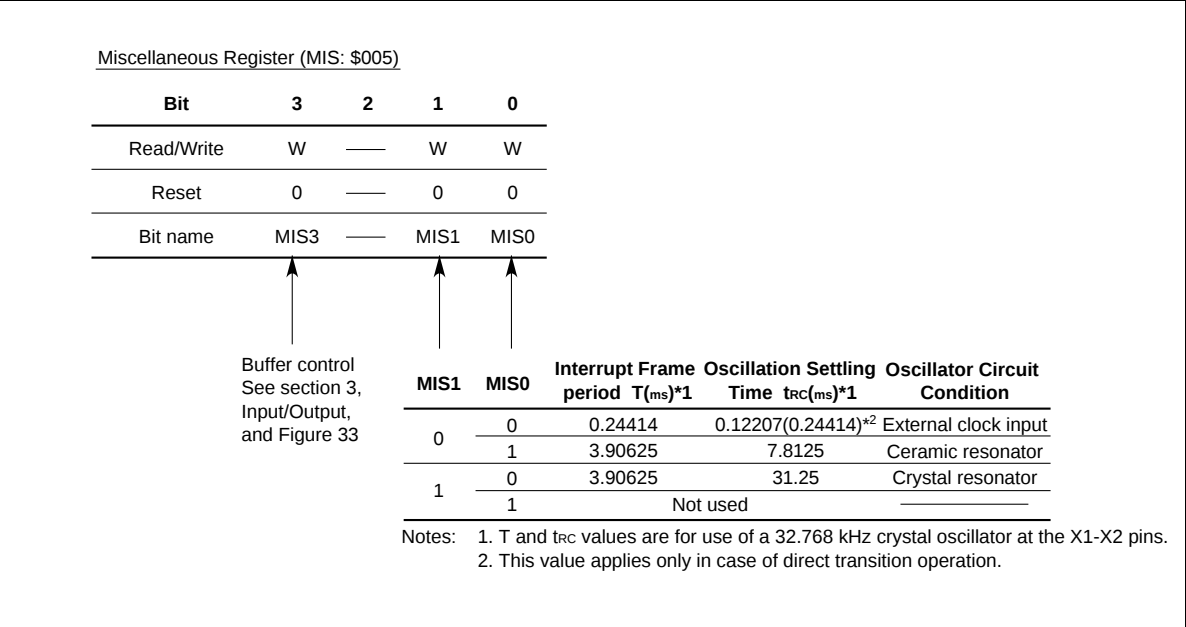


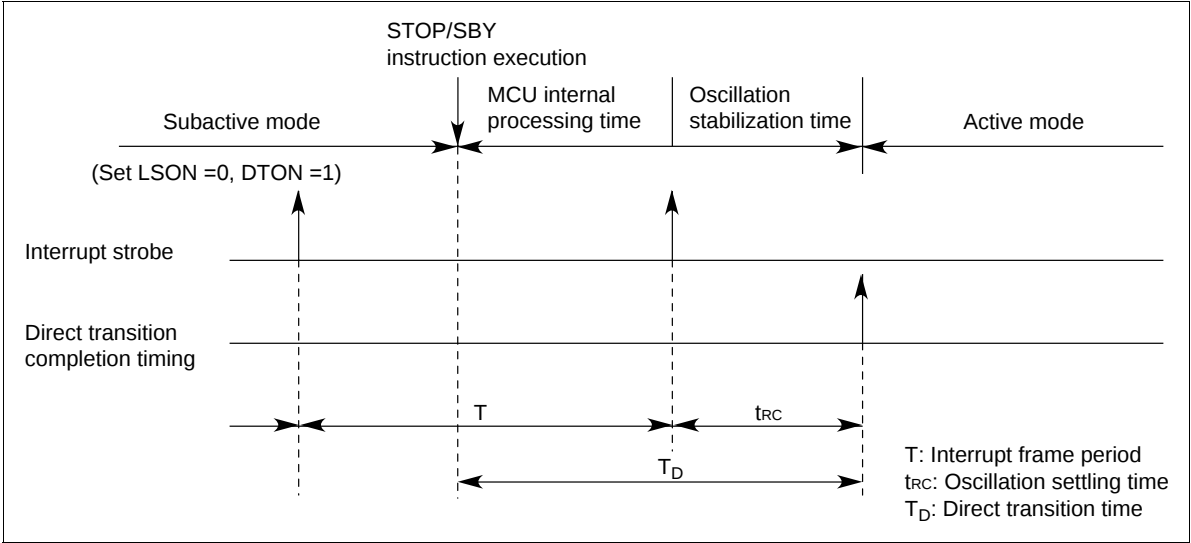
Figure 17 Miscellaneous Register (MIS)

**Direct transition from subactive to active mode:**

A direct transition can be made from subactive mode to active mode by controlling the direct transfer on flag (DTON: \$020,3) and low speed on flag (LSON: \$020,0). The procedure is shown below.

- (a) Set LSON = 0 and DTON = 1 in subactive mode.
- (b) Execute a STOP or SBY instruction.
- (c) After the lapse of the MCU internal processing time and the oscillation settling time, the MCU automatically switches from subactive mode to active mode (figure 18).

- Notes: 1. The DTON flag (\$020,3) can be set in only subactive mode. It is always in the reset state in active mode.
2. The condition for transition time  $T_D$  from the subactive mode to active mode is as follows:  
 $t_{RC} < T_D < T + t_{RC}$ .

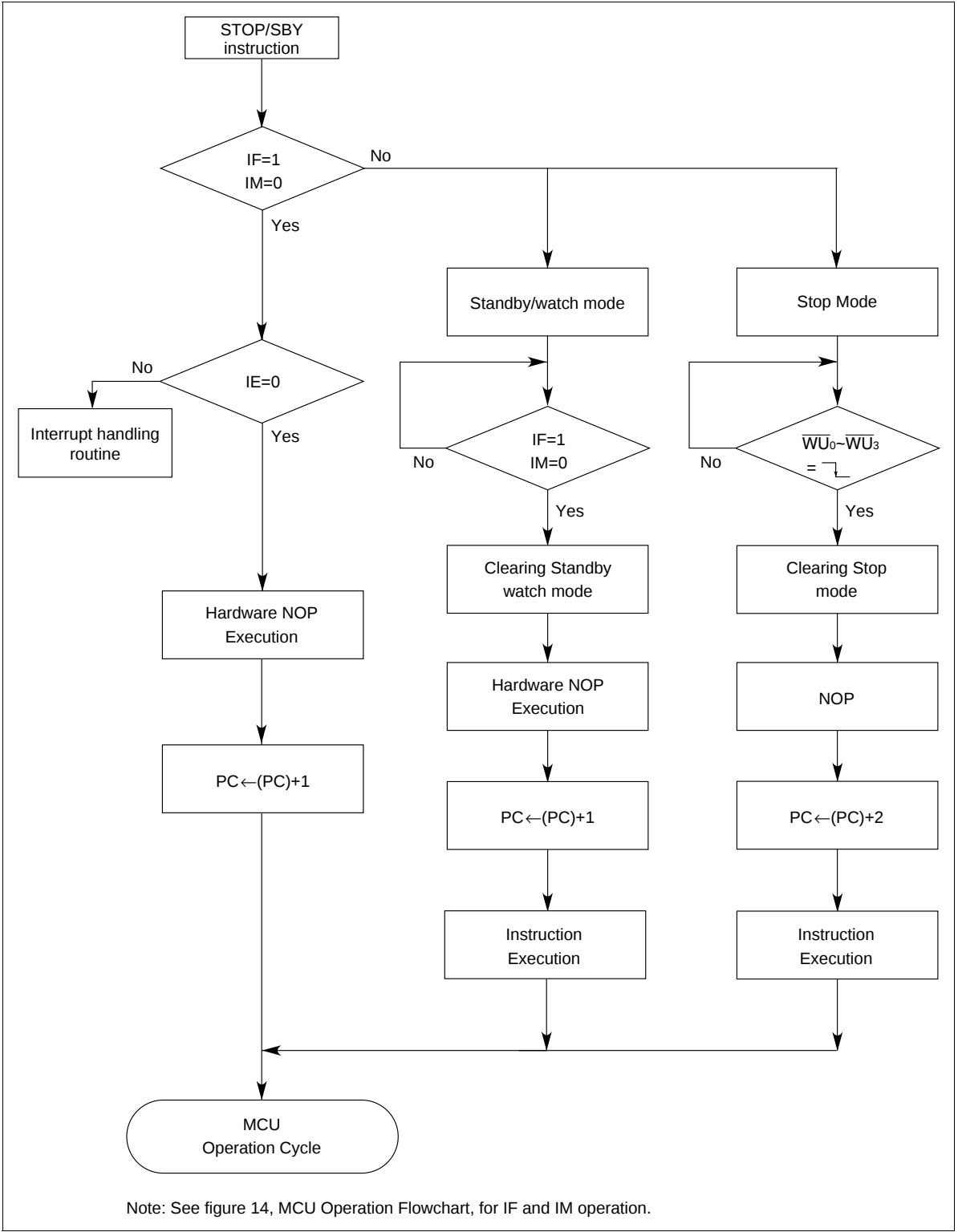


**Figure 18 Direct Transition Timing**

**MCU operation sequence:**

The MCU operates in accordance with the flowchart shown in figure 19.  $\overline{\text{RESET}}$  input is asynchronous input, and the MCU immediately enters the reset state upon  $\overline{\text{RESET}}$  input, regardless of its current state.

In the low-power mode operation sequence, if a STOP/SBY instruction is executed while the IE flag is cleared and the interrupt flag is set, releasing the relevant interrupt mask, the STOP/SBY instruction is canceled (regarded as NOP) and the next instruction is executed. Therefore, when executing a STOP/SBY instruction, all interrupt flags must be cleared, or interrupts masked, beforehand.



Note: See figure 14, MCU Operation Flowchart, for IF and IM operation.

Figure 19 MCU Operating Sequence (Low-Power Mode Operation)

Usage notes:

In watch mode and subactive mode, an interrupt will not be detected correctly if the  $\overline{\text{INT}}_0$  or  $\overline{\text{WU}}_0$  to  $\overline{\text{WU}}_3$  high or low-level period is shorter than the interrupt frame period.

The MCU's edge sensing method is shown in figure 20. The MCU samples the  $\overline{\text{INT}}_0$  and  $\overline{\text{WU}}_0$  to  $\overline{\text{WU}}_3$  signals at regular intervals, and if consecutive sampled values change from high to low, it determines that a falling edge has been generated.

Interrupt detection errors occur since this sampling is performed at the interrupt frame period. If the high-level period of the  $\overline{\text{INT}}_0$  or  $\overline{\text{WU}}_0$  to  $\overline{\text{WU}}_3$  signal is within an interrupt frame, as shown in figure 21 (a), the signal will be low at point A and point B, with the result that the falling edge will not be recognized. Similarly, If the low-level period of the  $\overline{\text{INT}}_0$  or  $\overline{\text{WU}}_0$  to  $\overline{\text{WU}}_3$  signal is within an interrupt frame, as shown in figure 21 (b), the signal will be high at point A and point B, with the result that the falling edge will not be recognized.

In watch mode and subactive mode, therefore, ensure that the high-level and low-level periods of the  $\overline{\text{INT}}_0$  and  $\overline{\text{WU}}_0$  to  $\overline{\text{WU}}_3$  signals is at least as long as the interrupt frame period.

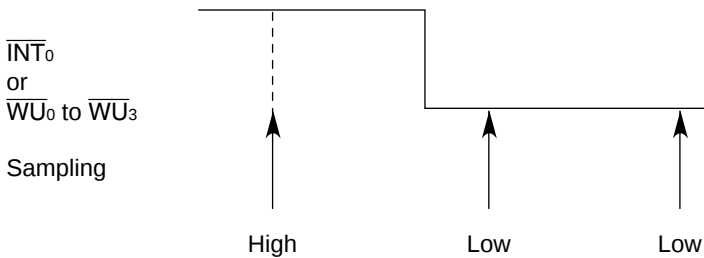


Figure 20 Edge Sensing Method

(a) High-level mode

(b) Low-level mode

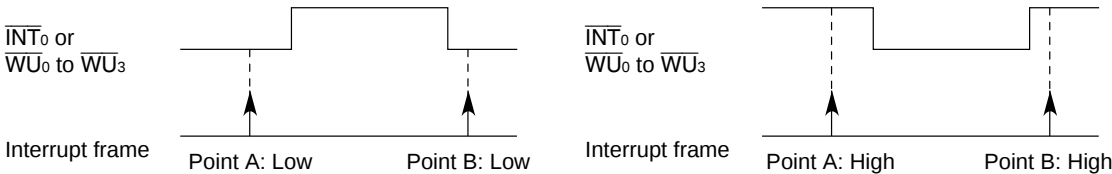


Figure 21 Sampling Examples

Internal Oscillator Circuit

Figure 22 shows the clock pulse generator circuit. As shown in table 21, a ceramic oscillator or crystal oscillator can be connected to OSC1 and OSC2, and a 32.768 kHz crystal oscillator can be connected to X1 and X2. External clock operation is possible for the system oscillator. Set bit 1 (SSR1) of the system clock select register (SSR: \$004) according to the frequency of the oscillator connected to OSC1 and OSC2 (figure 24).

Note: If the setting of bit 1 in the system clock select register does not match the frequency of the system oscillator, the subsystem using 32.768 kHz oscillation will not operate correctly.

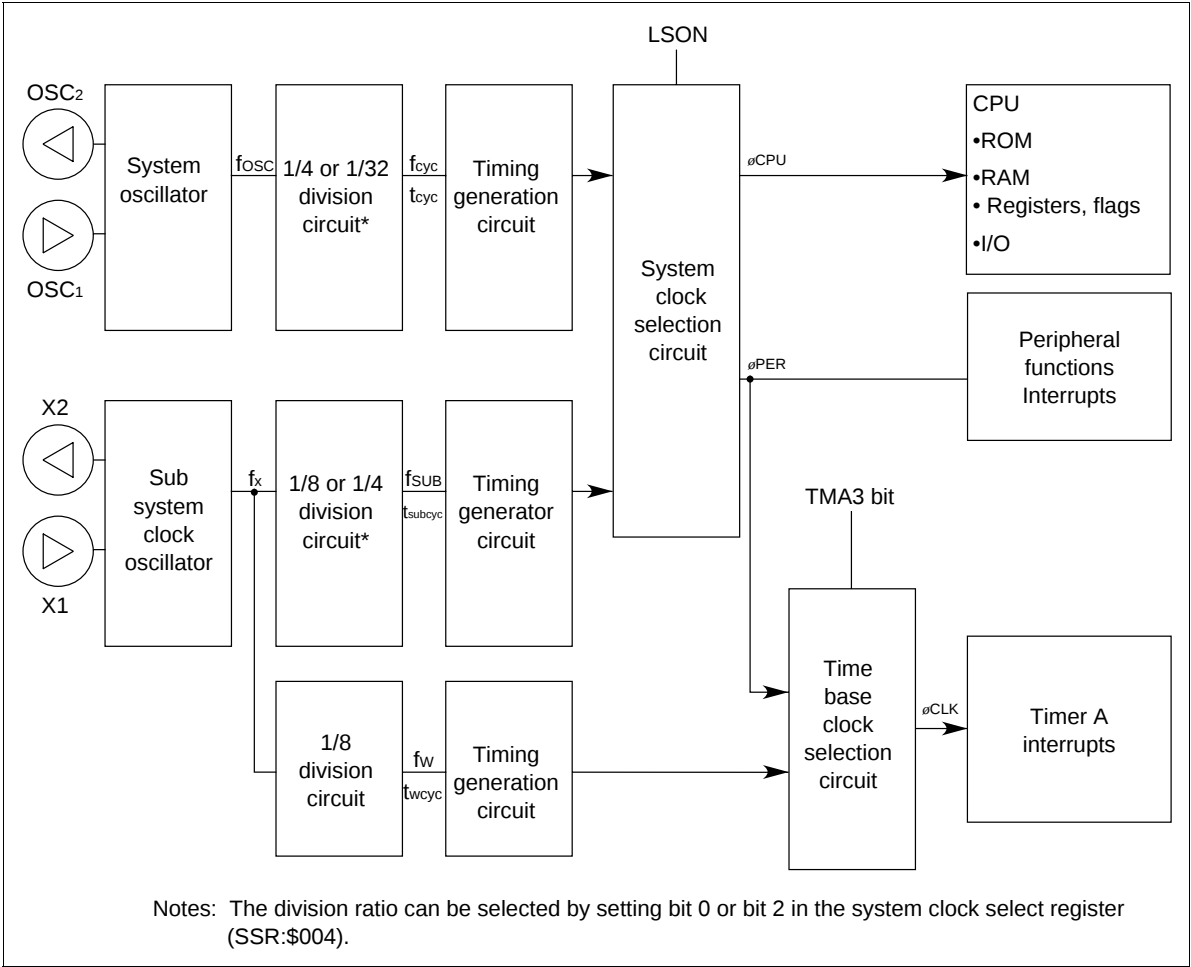


Figure 22 Clock Pulse Generator Circuit

## **System Clock Gear Function**

The MCU has a built-in system clock gear function that allows the system clock divided by 4 or by 32 to be selected by software for the instruction execution time. Efficient power consumption can be achieved by operating at the divided-by-4 rate when high-speed processing is needed, and at the divided-by-32 rate at the other times. Figure 23 shows the system clock conversion method.

System clock conversion from division-by-4 to division-by-32 is performed as follows. First, make the division-by-32 setting (SSR0 write), then set the gear enable flag (GEF: \$021,3). This flag is used to distinguish between gear conversion and a transition to standby mode. Next, execute an SBY instruction. When the gear enable flag is not set, standby mode is entered; when this flag is set, gear conversion mode is entered. In this case a transition is made to standby mode for the duration of the gear conversion, but after the synchronization time has elapsed, a transition is made automatically to active mode. As soon as the transition is made to active mode, the gear enable flag is reset.

The same procedure is used for conversion from division-by-32 to division-by-4.

Clear all interrupts, then disable interrupts, before carrying out gear conversion. Incorrect operation may result if an interrupt is generated during gear conversion.

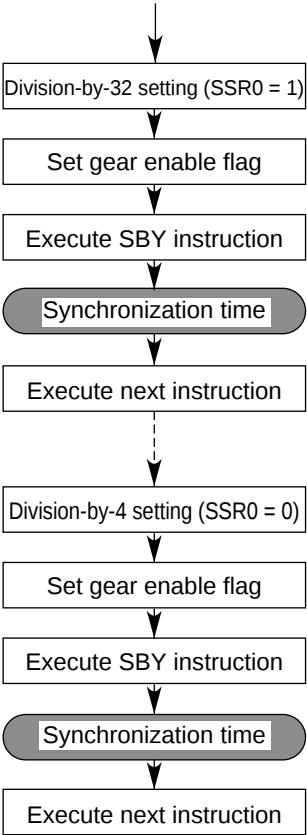


Figure 23 System Clock Division Ratio Conversion Flowchart

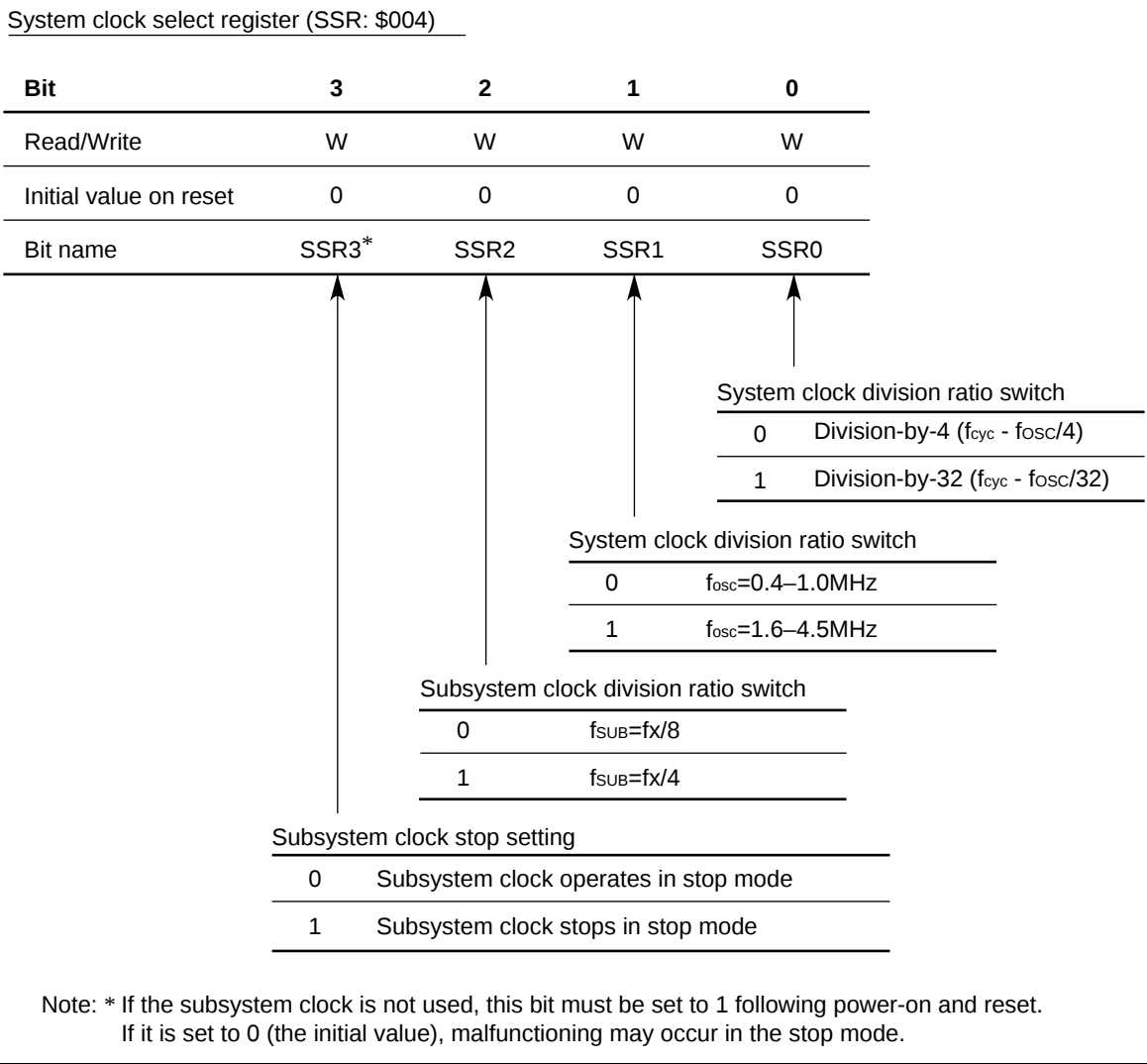
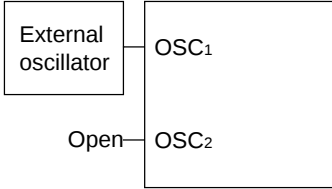
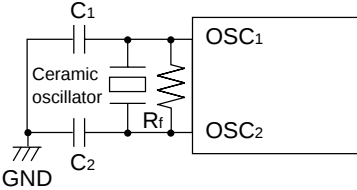
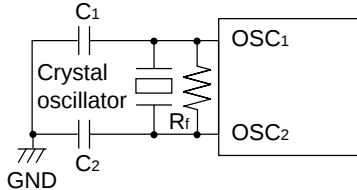
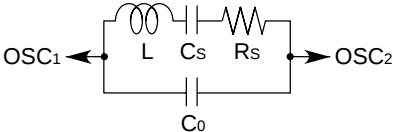
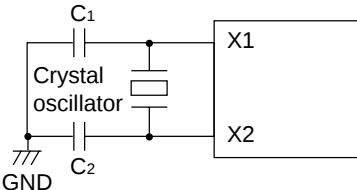
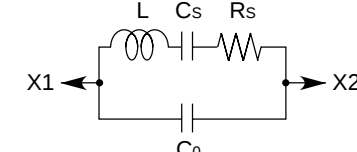


Figure 24 System Clock Select Register

Table 21 Oscillator Circuit Examples

| Circuit Structure                                                                                                                                                                                                                    | Circuit Constants                                                                                                                                                                                                              |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>External clock operation</p>                                                                                                                     |                                                                                                                                                                                                                                |
| <p>Ceramic oscillator (OSC<sub>1</sub>, OSC<sub>2</sub>)</p>                                                                                        | <p>Ceramic oscillator: CSA4.00MG (Murata)</p> <p><math>R_f=1\text{M}\Omega\pm20\%</math><br/><math>C_1=C_2=30\text{pF}\pm20\%</math></p>                                                                                       |
| <p>Crystal oscillator (OSC<sub>1</sub>, OSC<sub>2</sub>)</p> <br> | <p><math>R_f=1\text{M}\Omega\pm20\%</math><br/><math>C_1=C_2=10\text{--}22\text{pF}\pm20\%</math></p> <p>Crystal: Equivalent circuit at left<br/><math>C_0=7\text{pFmax.}</math><br/><math>R_s=100\Omega\text{max.}</math></p> |
| <p>Crystal oscillator (X1, X2)</p> <br>                        | <p>Crystal: 32.768 kHz: MX38T (Nihon Denpa Kogyo)</p> <p><math>C_1=C_2=20\text{pF}\pm20\%</math><br/><math>R_s=14\text{k}\Omega</math><br/><math>C_0=1.5\text{pF}</math></p>                                                   |

Notes: 1. With a crystal or ceramic oscillator, circuit constants will differ depending on the resonator, stray capacitance in the interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator manufacturer.

2. Make the connections between the OSC<sub>1</sub> and OSC<sub>2</sub> pins (X1 and X2 pins) and external components as short as possible, and ensure that no other lines cross these lines (see layout example in figure 25).

3. When 32.768 kHz crystal oscillation is not used, fix the X1 pin at V<sub>cc</sub> and leave the X2 pin open.

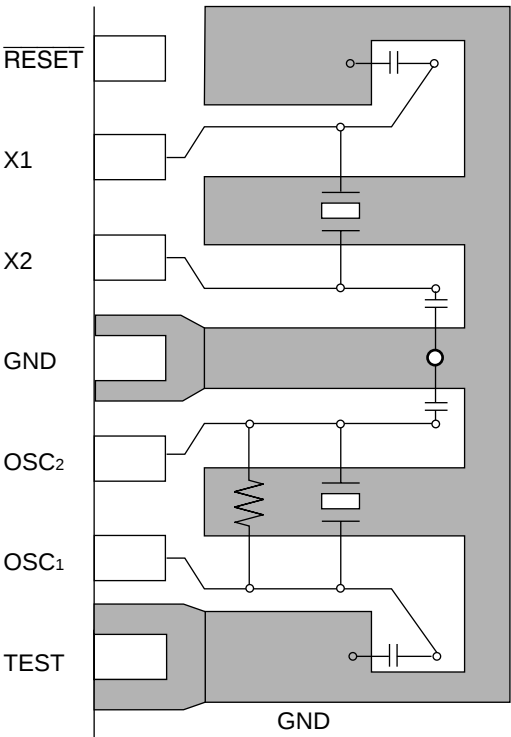


Figure 25 Typical Layouts of Crystal and Ceramic Oscillator

Input/Output

The MCU has 46 input/output pins ( $D_0$  to  $D_{11}$ ,  $R_0$  to  $R_7$ ,  $R_{8_0}$ , and  $R_{8_1}$ ) in the HD404889, HD404899, and HD404878 Series, or 41 input/output pins ( $D_0$  to  $D_9$ ,  $R_{0_0}$ ,  $R_{0_1}$ ,  $R_{0_2}$ , and  $R_1$  to  $R_7$ ) in the HD404868 Series. The features of these pins are described below.

- The four pins  $D_0$  to  $D_3$  are source large-current (10 mA max.) I/O pins.
- The eight pins  $D_4$  to  $D_{11}$  are sink large-current (15 mA max.) I/O pins.
- I/O pins comprise pins ( $D_0$ ,  $D_1$ ,  $R_0$ ,  $R_1$ ,  $R_{2_0}$  to  $R_{2_2}$ ,  $R_3$  to  $R_7$ ,  $R_{8_0}$ , and  $R_{8_1}$ ) that also have a peripheral function (timer, serial interface, etc.). With these pins, the peripheral function setting has priority over the D port or R port pin setting. When a peripheral function setting has been made for a pin, the pin function and input/output mode will be switched automatically in accordance with that setting.
- Selection of input or output for I/O pins, or selection of the port or peripheral function for pins multiplexed as peripheral function pins, is performed by the program.
- All output of the peripheral function pins are CMOS outputs. The SO pin and  $R_{2_2}$  port pin can be designated as NMOS open-drain output by the program.
- A reset clears peripheral function selection. And since the data control registers (DCD, DCR) are also reset, input/output pins go to the high-impedance state.
- Each I/O pin has a built-in pull-up MOS that can be turned on and off individually by the program.

Figure 26 shows the I/O buffer configuration, and table 22 shows I/O pin circuit configuration control by the program.

Table 23 shows the circuit configuration of each I/O pin.

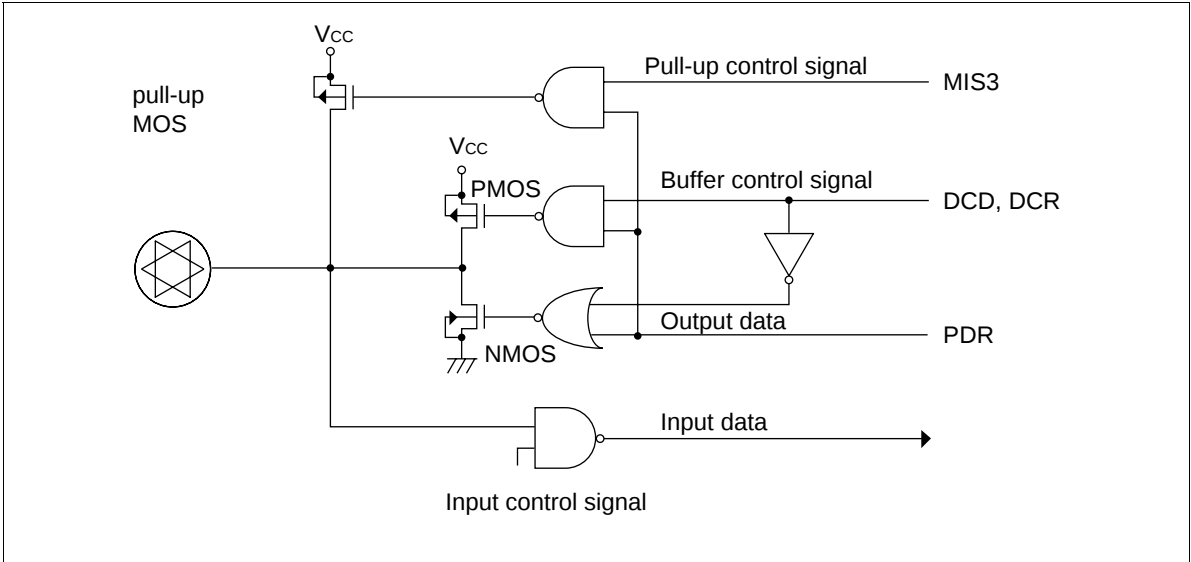


Figure 26 I/O Pin Circuit Configuration

### HD404889/HD404899/HD404878/HD404868 Series

### Table 22 Programmable I/O Circuits

| MIS3 (bit 3 of MIS) |      | 0 |   |    |    | 1 |    |    |    |
|---------------------|------|---|---|----|----|---|----|----|----|
| DCD,DCR             |      | 0 |   | 1  |    | 0 |    | 1  |    |
| PDR                 |      | 0 | 1 | 0  | 1  | 0 | 1  | 0  | 1  |
| CMOS buffer         | PMOS | — | — | —  | ON | — | —  | —  | ON |
|                     | NMOS | — | — | ON | —  | — | —  | ON | —  |
| pull-up MOS         |      | — | — | —  | —  | — | ON | —  | ON |

---

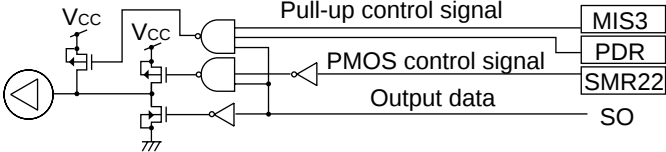
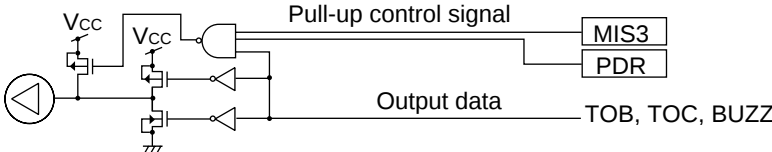
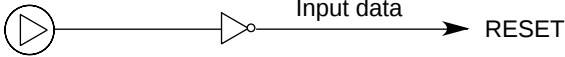
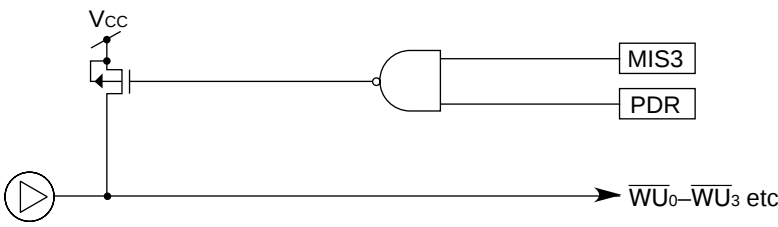
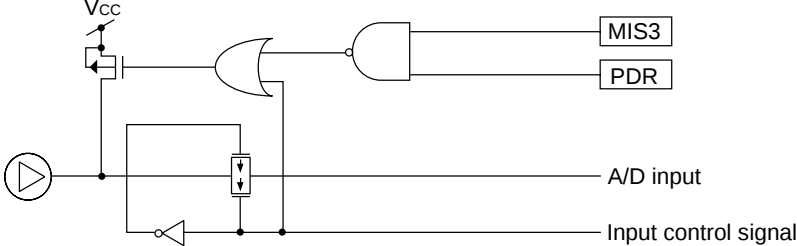
Note: — : OFF

### Table 23 Circuit Configurations of I/O Pins

| Type                     | Circuit Configuration | Pins                                                                                                                                                                                                 |
|--------------------------|-----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I/O pins                 |                       | $D_0$ - $D_{11}$<br>$R0_0$ - $R0_3$<br>$R1_0$ - $R1_3$<br>$R2_0$ , $R2_1$ , $R2_3$<br>$R3_0$ - $R3_3$<br>$R4_0$ - $R4_3$<br>$R5_0$ - $R5_3$<br>$R6_0$ - $R6_3$<br>$R7_0$ - $R7_3$<br>$R8_0$ - $R8_1$ |
| I/O pins                 |                       | $R2_2$                                                                                                                                                                                               |
| Peripheral function pins |                       | $\overline{SCK}$                                                                                                                                                                                     |

Note: In a reset, since the I/O control registers are reset, input/output pins go to the high-impedance state and peripheral function selections are cleared.

Table 23     Circuit Configurations of I/O Pins (cont)

| Type                     | Circuit Configuration                                                               | Pins                                                                                                  |
|--------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------|
| Peripheral function pins |    | SO                                                                                                    |
|                          |   | TOB, TOC, BUZZ                                                                                        |
| Input pins               |    | RESET                                                                                                 |
|                          |   | $\overline{WU_0}-\overline{WU_3}$ ,<br>$\overline{INT_0}$ , $\overline{INT_1}$ ,<br>EVNB,<br>EVND, SI |
|                          |  | $AN_0-AN_5^*$                                                                                         |

Notes: In a reset, since the I/O control registers are reset, input/output pins go to the high-impedance state and peripheral function selections are cleared.

\* Applies to HD404889, HD404899, and HD404868 Series.

## **D Port**

The D port consists of 12 I/O pins (10 I/O pins in the HD404868 Series) that are addressed bit-by-bit.

Ports D<sub>0</sub> to D<sub>3</sub> are source large-current I/O pins, and ports D<sub>4</sub> to D<sub>11</sub> (ports D<sub>4</sub> to D<sub>9</sub> in the HD404868 Series) are sink large-current I/O pins.

The D port can be set and reset by the SED and RED instructions or the SEDD and REDD instructions. Output data is stored in the port data register (PDR) for each pin. The entire D port can be tested by the TD or TDD instruction.

The D port output buffer is turned on and off by the D port data control registers (DCD0 to DCD2: \$030 to \$032). The DCD registers are mapped onto memory addresses (figure 27).

Ports D<sub>0</sub> and D<sub>1</sub> are multiplexed as interrupt input pins  $\overline{\text{INT}}_0$  and INT<sub>1</sub>, respectively. Setting as interrupt pins is performed by bits 0 and 1 (PMR00, PMR01) of port mode register 0 (PMR0: \$008) (figure 28).

Data control registers (DCD0–2 : \$030–\$032)  
(DCR0–8 : \$034–\$03C)

| Register Name | Bit        | 3           | 2           | 1           | 0           |
|---------------|------------|-------------|-------------|-------------|-------------|
| DCD0–DCD2     | Read/Write | W           | W           | W           | W           |
|               | Reset      | 0           | 0           | 0           | 0           |
|               | Bit name   | DCD03–DCD23 | DCD02–DCD22 | DCD01–DCD21 | DCD00–DCD20 |
| DCR0–DCR8     | Read/Write | W           | W           | W           | W           |
|               | Reset      | 0           | 0           | 0           | 0           |
|               | Bit name   | DCR03–DCR73 | DCR02–DCR72 | DCR01–DCR81 | DCR00–DCR80 |

| All bits | CMOS buffer control              |
|----------|----------------------------------|
| 0        | CMOS buffer off (high impedance) |
| 1        | CMOS buffer active               |

Correspondence between each bit of DCD and DCR and ports

| Register Name | Bit 3             | Bit 2             | Bit 1             | Bit 0             |
|---------------|-------------------|-------------------|-------------------|-------------------|
| DCD0          | D <sub>3</sub>    | D <sub>2</sub>    | D <sub>1</sub>    | D <sub>0</sub>    |
| DCD1          | D <sub>7</sub>    | D <sub>6</sub>    | D <sub>5</sub>    | D <sub>4</sub>    |
| DCD2          | D <sub>11</sub> * | D <sub>10</sub> * | D <sub>9</sub>    | D <sub>8</sub>    |
| DCR0          | R <sub>03</sub> * | R <sub>02</sub>   | R <sub>01</sub>   | R <sub>00</sub>   |
| DCR1          | R <sub>13</sub>   | R <sub>12</sub>   | R <sub>11</sub>   | R <sub>10</sub>   |
| DCR2          | R <sub>23</sub>   | R <sub>22</sub>   | R <sub>21</sub>   | R <sub>20</sub>   |
| DCR3          | R <sub>33</sub>   | R <sub>32</sub>   | R <sub>31</sub>   | R <sub>30</sub>   |
| DCR4          | R <sub>43</sub>   | R <sub>42</sub>   | R <sub>41</sub>   | R <sub>40</sub>   |
| DCR5          | R <sub>53</sub>   | R <sub>52</sub>   | R <sub>51</sub>   | R <sub>50</sub>   |
| DCR6          | R <sub>63</sub>   | R <sub>62</sub>   | R <sub>61</sub>   | R <sub>60</sub>   |
| DCR7          | R <sub>73</sub>   | R <sub>72</sub>   | R <sub>71</sub>   | R <sub>70</sub>   |
| DCR8          | —                 | —                 | R <sub>81</sub> * | R <sub>80</sub> * |

Note: \* Applies to HD404889, HD404899, and HD404878 Series

**Figure 27 Data Control Registers (DCD, DCR)**

## **R Port**

The R port consists of 34 I/O pins (31 I/O pins in the HD404868 Series) that are addressed in 4-bit units.

Input can be performed by means of the LAR and LBR instructions, and output by means of the LRA and LRB instructions. Output data is stored in the port data register (PDR) for each pin.

The R port output buffer is turned on and off by the R port data control registers (DCR0 to DCR8: \$034 to \$03C). The DCR registers are mapped onto memory addresses (figure 27).

Ports R0<sub>0</sub> to R0<sub>3</sub> are multiplexed as wakeup input pins  $\overline{WU}_0$  to  $\overline{WU}_3$ , respectively. Setting of these pins as peripheral function pins is performed by port mode register 1 (PMR1: \$009) (figure 29).

Ports R1<sub>0</sub> and R1<sub>1</sub> are multiplexed as peripheral function pins EVNB and EVND, respectively. Setting of these pins as peripheral function pins is performed by bits 0 and 1 (PMR20, PMR21) of port mode register 2 (PMR2: \$00A) (figure 30).

Ports R1<sub>2</sub> to R1<sub>3</sub> and R2<sub>0</sub> are multiplexed as peripheral function pins BUZZ, TOB, and TOC, respectively. Setting of these pins as peripheral function pins is performed by bits 2 and 3 (PMR22, PMR23) of port mode register 2 (PMR2: \$00A) and bit 0 (PMR30) of port mode register 3 (PMR3: \$00B)(figures 30 and 31).

Ports R2<sub>1</sub> and R2<sub>2</sub> are multiplexed as peripheral function pins  $\overline{SCK}$  and SI/SO, respectively. Setting of these pins as peripheral function pins is performed by bits 1 to 3 (PMR31 to PMR33) of port mode register 3 (PMR3: \$00B) (figure 31).

Ports R3 to R6 are multiplexed as peripheral function pins SEG1 to SEG16, respectively. Setting of these pins as segment pins is performed every 4 pins in 4-bit units by port mode register 4 (PMR4: \$00C) (figure 32).

Ports R7<sub>0</sub> to R7<sub>3</sub> and R8<sub>0</sub> to R8<sub>1</sub> also function as peripheral function pins AN<sub>0</sub> to AN<sub>5</sub> (HD404889, HD404899, and HD404868 series only). Peripheral function pin setting of these pins is performed using bits 1 to 3 (AMR<sub>1</sub> to AMR<sub>3</sub>) of the A/D mode register (AMR :\$028). (See Figure 74 in A/D Converter.)

Port mode register 0 (PMR0: \$008)

| Bit                    | 3        | 2        | 1     | 0     |
|------------------------|----------|----------|-------|-------|
| Read/Write             | —        | —        | W     | W     |
| Initial value on reset | —        | —        | 0     | 0     |
| Bit name               | Not used | Not used | PMR01 | PMR00 |

↑

PMR01

D<sub>1</sub>/INT<sub>1</sub> pin mode selection

|   |                  |
|---|------------------|
| 0 | D <sub>1</sub>   |
| 1 | INT <sub>1</sub> |

↑

PMR00

D<sub>0</sub>/INT<sub>0</sub> pin mode selection

|   |                  |
|---|------------------|
| 0 | D <sub>0</sub>   |
| 1 | INT <sub>0</sub> |

Figure 28 Port Mode Register 0 (PMR0: \$008)

Port mode register 1 (PMR1: \$009)

| Bit                    | 3      | 2     | 1     | 0     |
|------------------------|--------|-------|-------|-------|
| Read/Write             | W      | W     | W     | W     |
| Initial value on reset | 0      | 0     | 0     | 0     |
| Bit name               | PMR13* | PMR12 | PMR11 | PMR10 |

↑

| PMR10 | R00/ $\overline{WU}_0$ pin mode selection |
|-------|-------------------------------------------|
| 0     | R00                                       |
| 1     | $\overline{WU}_0$                         |

↑

| PMR11 | R01/ $\overline{WU}_1$ pin mode selection |
|-------|-------------------------------------------|
| 0     | R01                                       |
| 1     | $\overline{WU}_1$                         |

↑

| PMR12 | R02/ $\overline{WU}_2$ pin mode selection |
|-------|-------------------------------------------|
| 0     | R02                                       |
| 1     | $\overline{WU}_2$                         |

↑

| PMR13 | R03/ $\overline{WU}_3$ pin mode selection |
|-------|-------------------------------------------|
| 0     | R03                                       |
| 1     | $\overline{WU}_3$                         |

Note: \* Applies to HD404889, HD404899, and HD404878 Series

Figure 29 Port Mode Register 1 (PMR1: \$009)

Port mode register 2 (PMR2: \$00A)

| Bit                    | 3     | 2     | 1      | 0     |
|------------------------|-------|-------|--------|-------|
| Read/Write             | W     | W     | W      | W     |
| Initial value on reset | 0     | 0     | 0      | 0     |
| Bit name               | PMR23 | PMR22 | PMR21* | PMR20 |

↑

| PMR23 | R13/TOB pin mode selection |
|-------|----------------------------|
| 0     | R13                        |
| 1     | TOB                        |

↑

| PMR22 | R12/BUZZ pin mode selection |
|-------|-----------------------------|
| 0     | R12                         |
| 1     | BUZZ                        |

↑

| PMR21 | R11/EVND pin mode selection |
|-------|-----------------------------|
| 0     | R11                         |
| 1     | EVND                        |

↑

| PMR20 | R10/EVNB pin mode selection |
|-------|-----------------------------|
| 0     | R10                         |
| 1     | EVNB                        |

Note: \* Applies to HD404889, HD404899, and HD404878 Series

Figure 30 Port Mode Register 2 (PMR2: \$00A)

Port mode register 3 (PMR3: \$00B)

| Bit                    | 3     | 2     | 1     | 0     |
|------------------------|-------|-------|-------|-------|
| Read/Write             | W     | W     | W     | W     |
| Initial value on reset | 0     | 0     | 0     | 0     |
| Bit name               | PMR33 | PMR32 | PMR31 | PMR30 |

↑

PMR33

↑

PMR32

↑

PMR31

↑

PMR30

| PMR30 | R20/TOC pin mode selection |
|-------|----------------------------|
| 0     | R20                        |
| 1     | TOC                        |

| PMR31 | R21/ $\overline{\text{SCK}}$ pin mode selection |
|-------|-------------------------------------------------|
| 0     | R21                                             |
| 1     | $\overline{\text{SCK}}$                         |

| PMR33 | PMR32 | R22/SI/SO pin mode selection |
|-------|-------|------------------------------|
| 0     | *     | R22                          |
| 1     | 0     | SI                           |
|       | 1     | SO                           |

\* : Don't care

Figure 31 Port Mode Register 3 (PMR3: \$00B)

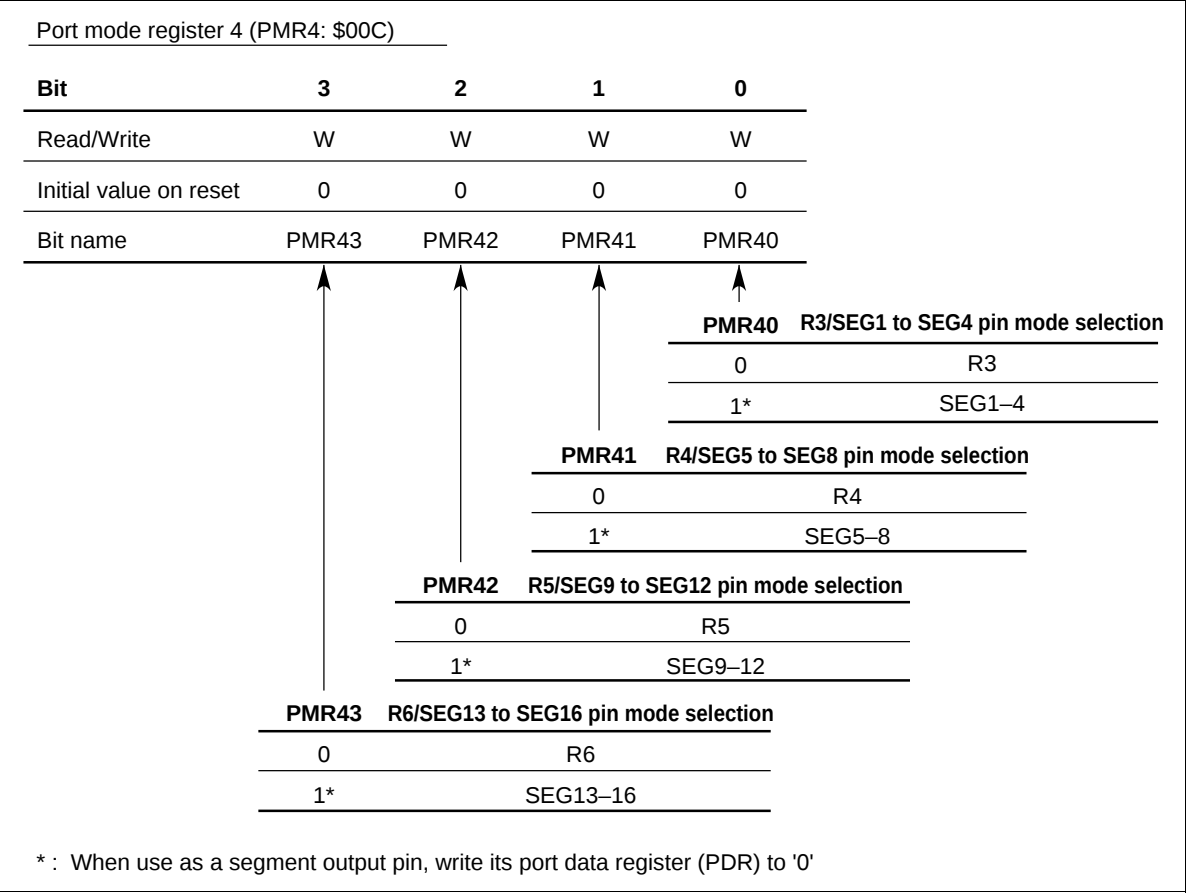


Figure 32 Port Mode Register 4 (PMR4: \$00C)

Pull-Up MOS Control

Program-controllable pull-ups MOS are incorporated in all I/O pins.

On/off control of all pull-ups MOS is performed by bit 3 (MIS3) of the miscellaneous register (MIS: \$005) and the port data register (PDR) for each pin, enabling the pull-up MOS to be turned on or off independently for each pin (table 22, figure 33).

Except for analog input multiplexed pins, the pull-up MOS on/off setting can be made independent of the setting as an on-chip supporting module pin.

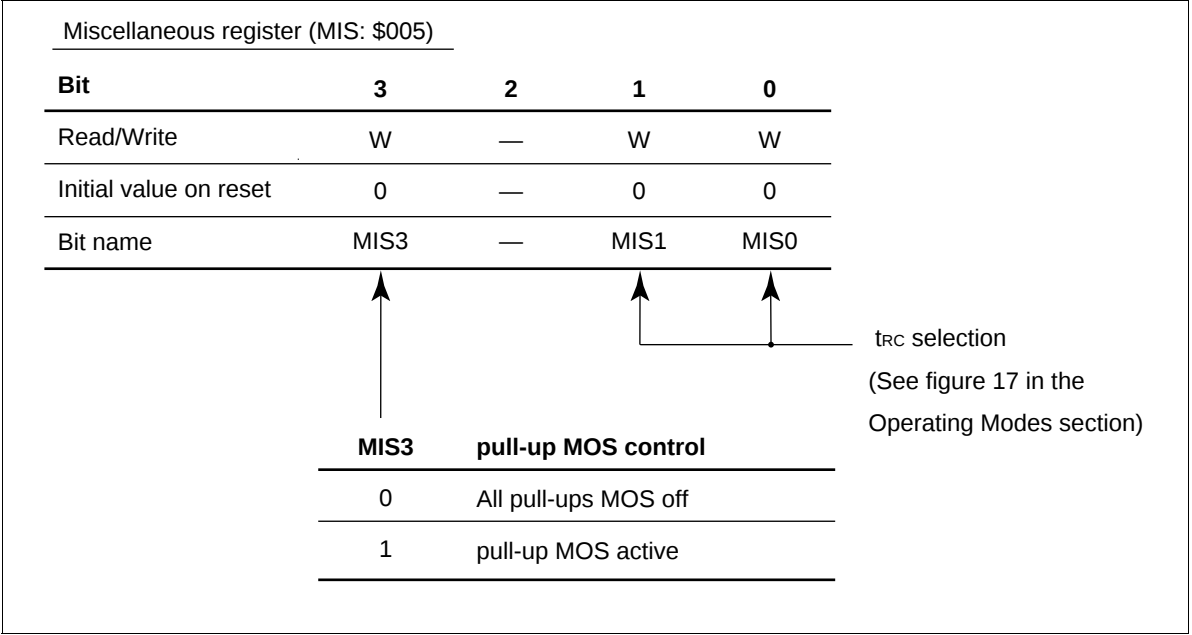


Figure 33 Miscellaneous Register (MIS:\$005)

Handling of I/O Pins Not Used by User System

If I/O pins that are not used by the user system are left floating, they may generate noise that can result in chip malfunctions. Therefore, the pin potential must be fixed.

In this case, pull the pins up to  $V_{CC}$  with the built-in pull-up MOS or with an external resistor of approximately 100 kΩ.

Prescalers

The MCU has the following two prescalers, S and W.

The operating conditions for each prescaler are shown in table 24, and the output supply destinations in figure 34.

Timer A to D input clocks other than external events, serial transfer clocks other than external clocks, and the LCD circuit operating clock are selected from the prescaler outputs in accordance with the respective mode register.

Prescaler Operation

Prescaler S (PSS):

Prescaler S is an 11-bit counter that has the system clock as input. When the MCU is reset, prescaler S is reset to \$000, then divides the system clock. Prescaler S operation is stopped by a reset by the MCU, and in stop mode and watch mode. It does not stop in any other modes.

Prescaler W (PSW):

Prescaler W is a counter that has a clock divided from the X1 input (32 kHz crystal oscillation) as input.

When the MCU is reset, prescaler W is reset to \$00, then divides the input clock. Prescaler W can also be reset by software.

Table 24 Prescaler Operating Conditions

| Prescaler   | Input Clock                                                                             | Reset Conditions               | Stop Conditions                  |
|-------------|-----------------------------------------------------------------------------------------|--------------------------------|----------------------------------|
| Prescaler S | System clock in active and standby modes, Subsystem clock in subactive mode             | MCU reset, Stop mode clearance | MCU reset, Stop mode, Watch mode |
| Prescaler W | Clock obtained by division-by-8 of 32.768 kHz oscillation by subsystem clock oscillator | MCU reset, Software*           | MCU reset, Stop mode             |

Note: If bits TMA3 to TMA1 in timer mode register A (TMA) are all set to 1, PSW is cleared to \$00.

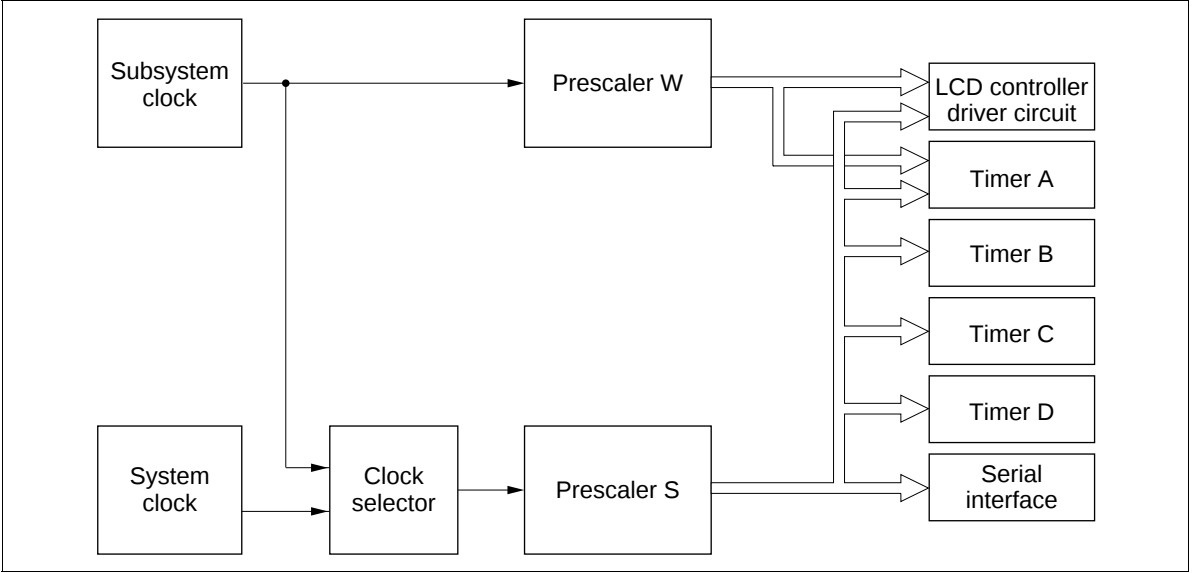


Figure 34 Prescaler Output Destinations

Timers

The MCU incorporates four timers, A to D, in the HD404889, HD404899, and HD404878 Series, or three timers, A to C, in the HD404868 Series.

- Timer A: Free-running timer
- Timer B: Multifunctional timer
- Timer C: Multifunctional timer
- Timer D: Multifunctional timer

Timer A is an 8-bit free-running timer. Timers B, C, and D are 8-bit multifunctional timers; Each one of their have the functions shown in table 25 and their operating mode can be set by the program.

Table 25     Timer Functions

| Functios        |                | Timer A   | Timer B   | Timer C   | Timer D   |
|-----------------|----------------|-----------|-----------|-----------|-----------|
| Clock source    | Prescaler S    | Available | Available | Available | Available |
|                 | Prescaler W    | Available | —         | —         | —         |
|                 | External event | —         | Available | —         | Available |
| Timer functions | Free-running   | Available | Available | Available | Available |
|                 | Time-base      | Available | —         | —         | —         |
|                 | Event counter  | —         | Available | —         | Available |
|                 | Reload         | —         | Available | Available | Available |
|                 | Watchdog       | —         | —         | Available | —         |
|                 | Input Capture  | —         | —         | —         | Available |
| Timer outputs   | Toggle         | —         | Available | Available | —         |
|                 | PWM            | —         | Available | Available | —         |

Note: — implies not available

Timer A

Timer A Functions

Timer A has the following functions.

- Free-running timer
- Realtime clock time base

The block diagram of timer A is shown in figure 35.

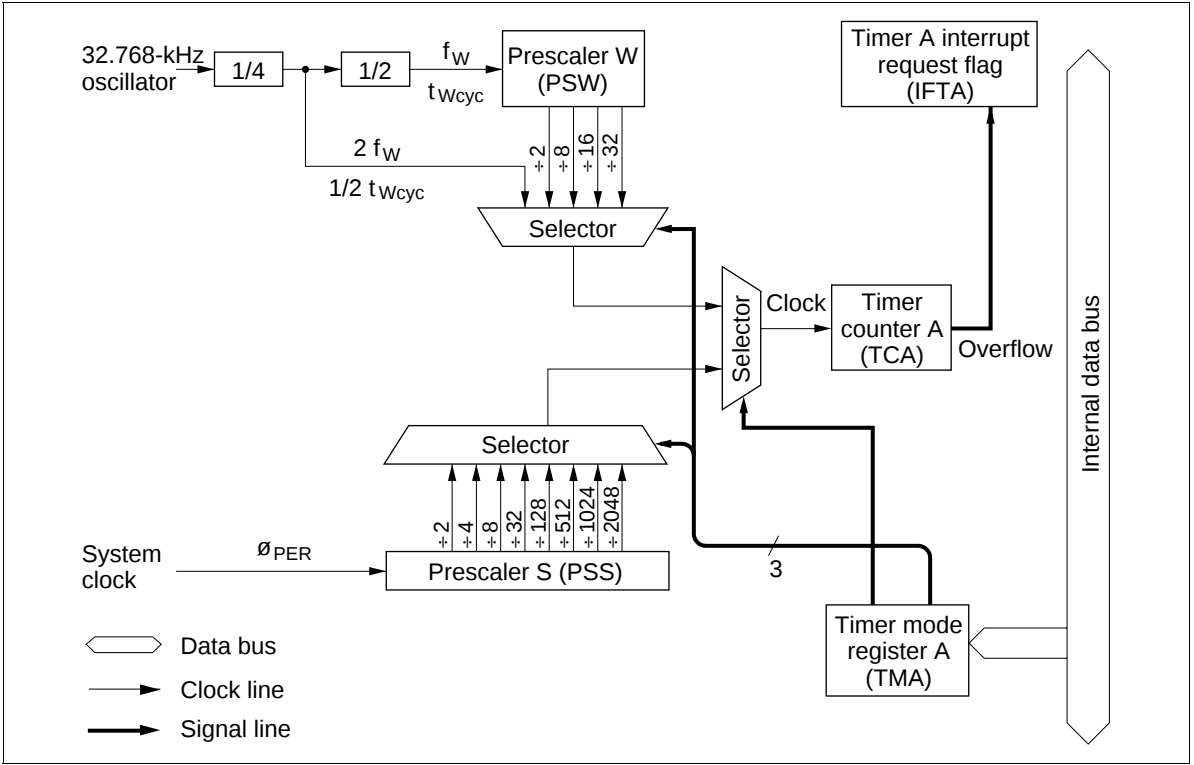


Figure 35 Timer A Block Diagram

## Timer A Operation

### Free-running timer operation:

The timer A input clock is selected by timer mode register A (TMA: \$00F).

Timer A is reset to \$00 by an MCU reset, and counts up each time the input clock is input. When the input clock is input after the timer A value reaches \$FF, overflow output is generated, and the timer A value becomes \$00. The generated overflow output sets the timer A interrupt request flag (IFTA: \$002,0). Timer A continues counting up after the count value returns to \$00, so that an interrupt is generated regularly every 256 input clock cycles.

### Realtime clock time base operation:

Timer A can be used as the realtime clock time base by setting bit 3 (TMA3) of timer mode register A to 1. As the prescaler W output is input to timer/counter A, interrupts are generated with accurate timing using the 32.768 kHz crystal oscillator as the basic clock.

When timer A is used as the realtime clock time base, prescaler W and timer/counter A can be reset to \$00 by the program.

### **Timer A Register**

Timer A operation is set by means of the following register.

#### **Timer mode register A (TMA: \$00F):**

Timer mode register A (TMA: \$00F) is a 4-bit write-only register. Timer A operation and input clock selection are set as shown in figure 36.

Timer mode register A (TMA: \$00F)

| Bit                    | 3    | 2    | 1    | 0    |
|------------------------|------|------|------|------|
| Read/Write             | W    | W    | W    | W    |
| Initial value on reset | 0    | 0    | 0    | 0    |
| Bit name               | TMA3 | TMA2 | TMA1 | TMA0 |

| TMA3 | TMA2 | TMA1 | TMA0 | Source prescaler | Input clock period     | Operating mode |
|------|------|------|------|------------------|------------------------|----------------|
| 0    | 0    | 0    | 0    | PSS              | 2,048 t <sub>cyc</sub> | Timer A mode   |
|      |      |      | 1    | PSS              | 1,024 t <sub>cyc</sub> |                |
|      |      | 1    | 0    | PSS              | 512 t <sub>cyc</sub>   |                |
|      |      |      | 1    | PSS              | 128 t <sub>cyc</sub>   |                |
|      | 1    | 0    | 0    | PSS              | 32 t <sub>cyc</sub>    |                |
|      |      |      | 1    | PSS              | 8 t <sub>cyc</sub>     |                |
|      |      | 1    | 0    | PSS              | 4 t <sub>cyc</sub>     |                |
|      |      |      | 1    | PSS              | 2 t <sub>cyc</sub>     |                |
| 1    | 0    | 0    | 0    | PSW              | 32 t <sub>wcyc</sub>   | Time base mode |
|      |      |      | 1    | PSW              | 16 t <sub>wcyc</sub>   |                |
|      |      | 1    | 0    | PSW              | 8 t <sub>wcyc</sub>    |                |
|      |      |      | 1    | PSW              | 2 t <sub>wcyc</sub>    |                |
|      | 1    | 0    | 0    | PSW              | 1/2 t <sub>wcyc</sub>  |                |
|      |      |      | 1    | Not Used         |                        |                |
|      |      | 1    | *    | PSW, TCA reset   |                        |                |

\* : Don't care

- Notes:
- 1. t<sub>wcyc</sub> = 244.14 μs (using 32.768 kHz crystal oscillator)
  - 2. Timer/counter overflow output period (s) = input clock period (s) × 256.
  - 3. If PSW and TCA reset is selected during LCD, the LCD enters the halt state (power switch off). Therefore, to provide continuous LCD the PSW and TCA reset interval must be minimized by the program.
  - 4. The division ratio must not be changed while time base mode is being used, as this will result in an error in the overflow period.

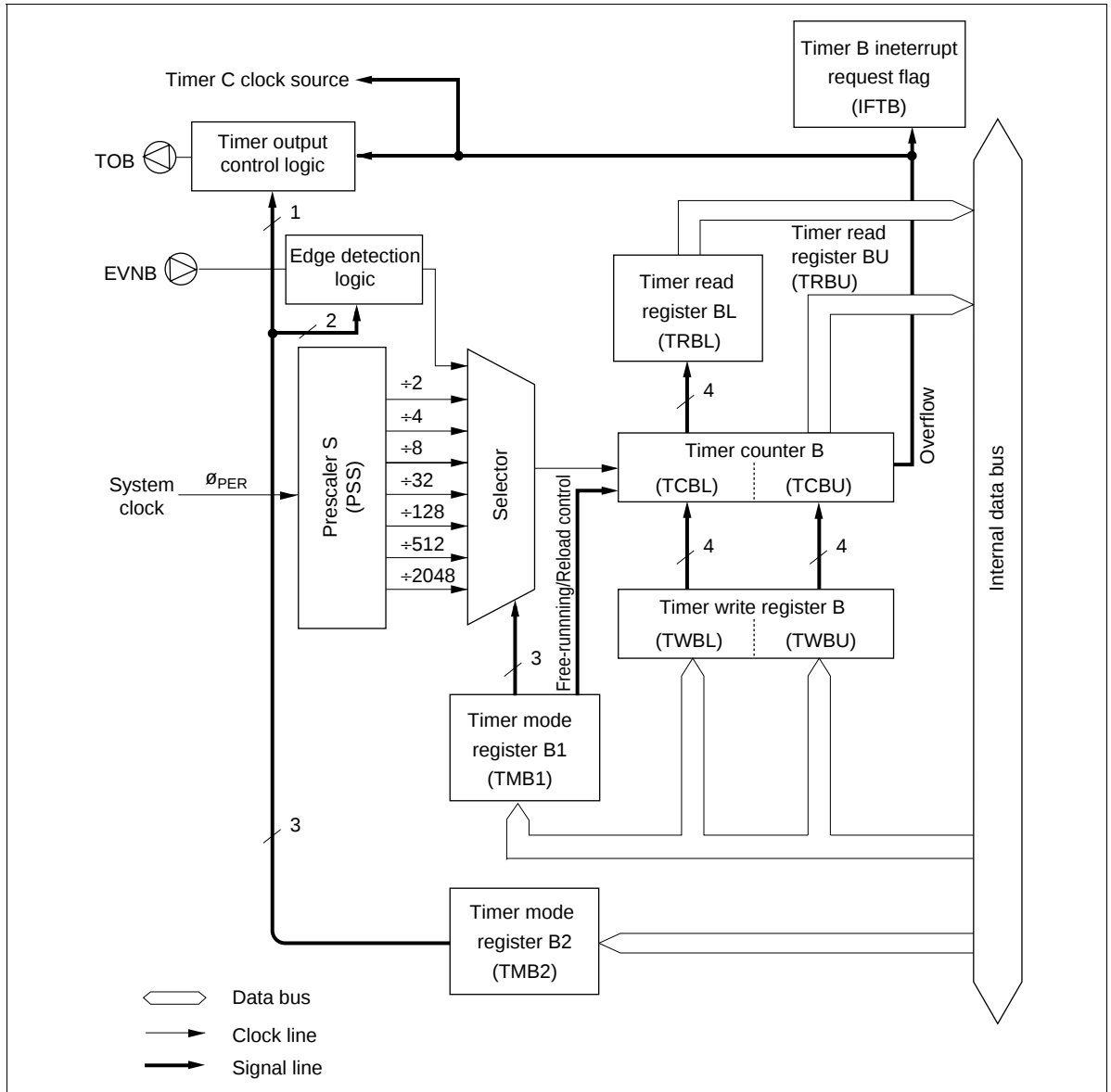
Figure 36 Timer Mode Register A (TMA)

### Timer B

**Timer B Functions:** Timer B has the following functions.

- Free-running/reload timer
- External event counter
- Timer output operation (toggle output, PWM output)

The block diagram of timer B is shown in figure 37.



### Figure 37 Timer B Block Diagram

## **Timer B Operation**

- Free-running/reload timer:

Free-running/reload timer operation, the input clock source, and the prescaler division ratio are selected by means of timer mode register B1 (TMB1).

Timer B is initialized to the value written to timer write register B (TWBL, TWBU) by software, and counts up by 1 each time the input clock is input. When the input clock is input after the timer B value reaches \$FF, overflow output is generated. Timer B is then set to the value in timer write register B if the reload timer function is selected, or to \$00 if the free-running timer function is selected, and starts counting up again.

Overflow output sets the timer B interrupt request flag (IFTB). This flag is reset by the program or by an MCU reset.

For details, see figure 3, Interrupt Control Bit and Register Flag Area Configuration, and table 1, Initial Values after MCU Reset.

- External event counter operation:

When external event input is designated for the input clock, timer B operates as an external event counter. When external event input is used, the R1<sub>0</sub>/EVNB pin is designated as the EVNB pin by port mode register 2 (PMR2).

The external event detected edge for timer B can be designated as a falling edge, rising edge, or both falling and rising edges in the input signal by means of timer mode register B2 (TMB2). If both falling and rising edges are selected, the input signal falling and rising edge interval should be at least 2tcyc.

Timer B counts up by 1 each time a falling edge is detected in the signal input at the EVNB pin. Other operations are the same as for the free-running/reload timer function.

- Timer output operation:

With timer B, the R13/TOB pin is designated as the TOB pin by the setting of bit 3 of port mode register 2 (PMR2), and toggle waveform output or PWM waveform output can be selected by timer mode register B2 (TMB2).

- Toggle output:

With toggle output, the output level is changed upon input of the next clock pulse after the timer B value reaches \$FF. Use of this function in combination with the reload timer allows a clock signal with any period to be output, enabling it to be used as buzzer output. The output waveform is shown in figure 38 (1).

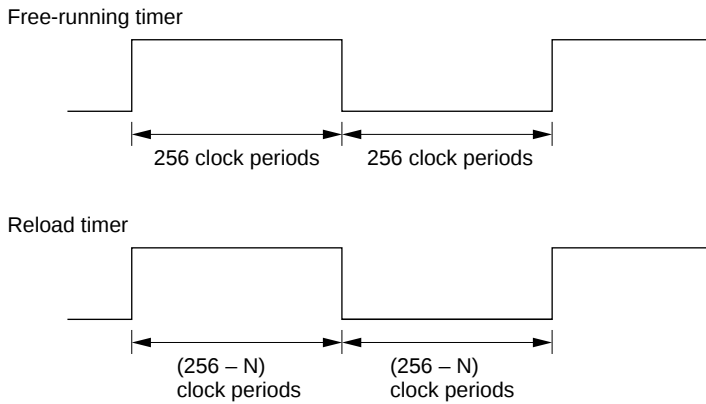
- PWM output:

With PWM output, variable-duty pulses are output. The output waveform is as shown in figure 38 (2), according to the contents of timer mode register B1 (TMB1) and timer write register B (TWBL, TWBU). When the waveform is output with bit 3 (TMB13) of timer mode register B1 cleared to 0, the write to timer write register B to change the duty is effective from the next frame, whereas if the waveform is output with the TMB13 bit set to 1 (reload setting), the next frame is output immediately after the timer write register write.

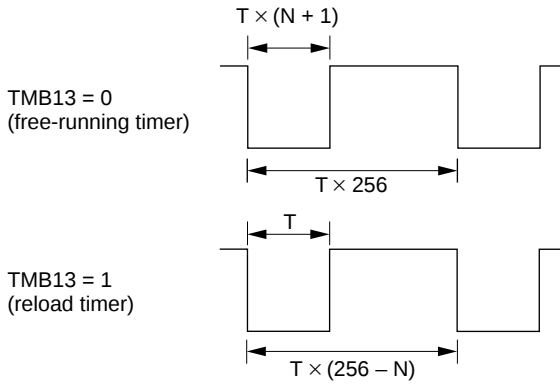
- Module standby:

With timer B, the supply of the system clock to the timer/counter can be halted by setting bit 0 of module standby register 1 (MSR1: \$00D) to 1. In the module standby state, the mode register value is retained but the counter value is not guaranteed.

(1) Toggle output waveform (timer B, timer C)



(2) PWM output waveform (timer B, timer C)



Notes: T: Counter input clock period

(The clock input source and division ratio are controlled by timer mode register B1 and timer mode register C1.)

N: Value in timer write register B or timer write register C

When  $N = 255 (= \$FF)$ , PWM output is always fixed at the timer low level.)

Figure 38 Timer Output Waveforms

### **Timer B Registers**

Timer B operation setting and timer B value reading/writing is controlled by the following registers.

Timer mode register B1 (TMB1: \$010)

Timer mode register B2 (TMB2: \$011)

Timer write register B (TWBL: \$012, TWBU: \$013)

Timer read register B (TRBL: \$012, TRBU: \$013)

Port mode register 2 (PMR2: \$00A)

Module standby register 1 (MSR1: \$00D)

- Timer mode register B1 (TMB1: \$010):

Timer mode register B1 (TMB1) is a 4-bit write-only register, used to select free-running/reload timer operation and the input clock as shown in figure 39.

Timer mode register B1 (TMB1) is reset to \$0 by an MCU reset:

A modification of timer mode register B1 (TMB1) becomes effective after execution of two instructions following the timer mode register B1 (TMB1) write instruction. The program must provide for timer B initialization by writing to timer write register B (TWBL, TWBU) to be executed after the post-modification mode has become effective.

Timer mode register B1 (TMB1: \$010)

| Bit                    | 3     | 2     | 1     | 0     |
|------------------------|-------|-------|-------|-------|
| Read/Write             | W     | W     | W     | W     |
| Initial value on reset | 0     | 0     | 0     | 0     |
| Bit name               | TMB13 | TMB12 | TMB11 | TMB10 |

TMB12

TMB11

TMB10

Input clock period and input clock source

|   |   |   |                                 |
|---|---|---|---------------------------------|
| 0 | 0 | 0 | 2,048 $t_{\text{cyc}}$          |
|   |   | 1 | 512 $t_{\text{cyc}}$            |
|   | 1 | 0 | 128 $t_{\text{cyc}}$            |
|   |   | 1 | 32 $t_{\text{cyc}}$             |
| 1 | 0 | 0 | 8 $t_{\text{cyc}}$              |
|   |   | 1 | 4 $t_{\text{cyc}}$              |
|   | 1 | 0 | 2 $t_{\text{cyc}}$              |
|   |   | 1 | R10/EVNB (external event input) |

|       |                           |
|-------|---------------------------|
| TMB13 | Free-running/reload timer |
| 0     | Free-running timer        |
| 1     | Reload timer              |

Figure 39 Timer Mode Register B1 (TMB1)

- Timer mode register B2 (TMB2: \$011):  
Timer mode register B2 (TMB2) is a 3-bit write-only register, used to select the timer B output mode and EVNB pin detected edge as shown in figure 40.  
Timer mode register B2 (TMB2) is reset to \$0 by an MCU reset.

Timer mode register B2 (TMB2: \$011)

| Bit                    | 3 | 2     | 1     | 0     |
|------------------------|---|-------|-------|-------|
| Read/Write             | — | W     | W     | W     |
| Initial value on reset | — | 0     | 0     | 0     |
| Bit name               | — | TMB22 | TMB21 | TMB20 |

TMB21

TMB20

EVNB pin detected edge

|   |   |                                        |
|---|---|----------------------------------------|
| 0 | 0 | Not detected                           |
|   | 1 | Falling edge detection                 |
| 1 | 0 | Rising edge detection                  |
|   | 1 | Both rising and falling edge detection |

TMB22

Timer B output waveform

|   |               |
|---|---------------|
| 0 | Toggle output |
| 1 | PWM output    |

Figure 40 Timer Mode Register B2 (TMB2)

- Timer write register B (TWBL: \$012, TWBU:\$013):  
Timer write register B (TWBL, TWBU) is a write-only register composed of a lower digit (TWBL) and an upper digit (TWBU) (figures 41 and 42).  
The lower digit (TWBL) of timer write register B is reset to \$0 by an MCU reset, while the upper digit (TWBU) is undetermined.  
Timer B can be initialized by writing to timer write register B (TWBL, TWBU). To write the data, first write the lower digit (TWBL). The lower digit write does not change the timer B value. Next, write the upper digit (TWBU). Timer B is then initialized to the timer write register B (TWBL, TWBU) value. When writing to timer write register B (TWBL, TWBU) from the second time onward, if it is not necessary to change the lower digit (TWBL) reload value, timer B initialization is completed by the upper digit write alone.

Timer write register B (lower) (TWBL: \$012)

| Bit                    | 3     | 2     | 1     | 0     |
|------------------------|-------|-------|-------|-------|
| Read/Write             | W     | W     | W     | W     |
| Initial value on reset | 0     | 0     | 0     | 0     |
| Bit name               | TWBL3 | TWBL2 | TWBL1 | TWBL0 |

Figure 41 Timer Write Register B (Lower) (TWBL)

Timer write register B (upper) (TWBU: \$013)

| Bit                    | 3            | 2            | 1            | 0            |
|------------------------|--------------|--------------|--------------|--------------|
| Read/Write             | W            | W            | W            | W            |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name               | TWBU3        | TWBU2        | TWBU1        | TWBU0        |

**Figure 42 Timer Write Register B (Upper) (TWBU)**

- Timer read register B (TRBL: \$012, TRBU: \$013):

Timer read register B (TRBL, TRBU) is a read-only register composed of a lower digit (TRBL) and an upper digit (TRBU) from which the value of the upper digit of timer B is read directly (figures 43 and 44).

First, read the upper digit (TRBU) of timer read register B. The current value of the timer B upper digit is read and, at the same time, the value of the timer B lower digit is latched in the lower digit (TRBL) of timer read register B. The timer B value is obtained when the upper digit (TRBU) of timer read register B is read by reading the lower digit (TRBL) of timer read register B.

Timer read register B (lower) (TRBL: \$012)

| Bit                    | 3            | 2            | 1            | 0            |
|------------------------|--------------|--------------|--------------|--------------|
| Read/Write             | R            | R            | R            | R            |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name               | TRBL3        | TRBL2        | TRBL1        | TRBL0        |

**Figure 43 Timer Read Register B (Lower) (TRBL)**

Timer read register B (upper) (TRBU: \$013)

| Bit                    | 3            | 2            | 1            | 0            |
|------------------------|--------------|--------------|--------------|--------------|
| Read/Write             | R            | R            | R            | R            |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name               | TRBU3        | TRBU2        | TRBU1        | TRBU0        |

**Figure 44 Timer Read Register B (Upper) (TRBU)**

- Port mode register 2 (PMR2: \$00A):  
Port mode register 2 (PMR2) is a write-only register used to set the function of the R1<sub>0</sub>/EVNB and R1<sub>3</sub>/TOB pins as shown in figure 45.  
Port mode register 2 (PMR2) is reset to \$0 by an MCU reset.

Port mode register 2 (PMR2: \$00A)

| Bit                    | 3     | 2     | 1      | 0     |
|------------------------|-------|-------|--------|-------|
| Read/Write             | W     | W     | W      | W     |
| Initial value on reset | 0     | 0     | 0      | 0     |
| Bit name               | PMR23 | PMR22 | PMR21* | PMR20 |

↑

| PMR20 | R1 <sub>0</sub> /EVNB pin mode selection |
|-------|------------------------------------------|
| 0     | R1 <sub>0</sub>                          |
| 1     | EVNB                                     |

↑

| PMR21 | R1 <sub>1</sub> /EVND pin mode selection |
|-------|------------------------------------------|
| 0     | R1 <sub>1</sub>                          |
| 1     | EVND                                     |

↑

| PMR22 | R1 <sub>2</sub> /BUZZ pin mode selection |
|-------|------------------------------------------|
| 0     | R1 <sub>2</sub>                          |
| 1     | BUZZ                                     |

↑

| PMR23 | R1 <sub>3</sub> /TOB pin mode selection |
|-------|-----------------------------------------|
| 0     | R1 <sub>3</sub>                         |
| 1     | TOB                                     |

Note: \* Applies to HD404889, HD404899, and HD404878 Series

Figure 45 Port Mode Register 2 (PMR2: \$00A)

- Module standby register 1 (MSR1: \$00D):  
Module standby register 1 (MSR1) is a write-only register used to designate supply or stopping of the clock to timer B as shown in figure 46.  
Module standby register 1 (MSR1) is reset to \$0 by an MCU reset.

Module standby register 1 (MSR1: \$00D)

| Bit                    | 3 | 2     | 1     | 0     |
|------------------------|---|-------|-------|-------|
| Read/Write             | — | W     | W     | W     |
| Initial value on reset | — | 0     | 0     | 0     |
| Bit name               | — | MSR12 | MSR11 | MSR10 |

↑

MSR12

Timer D clock supply control

|   |          |
|---|----------|
| 0 | Supplied |
| 1 | Stopped  |

↑

MSR11

Timer C clock supply control

|   |          |
|---|----------|
| 0 | Supplied |
| 1 | Stopped  |

↑

MSR10

Timer B clock supply control

|   |          |
|---|----------|
| 0 | Supplied |
| 1 | Stopped  |

Figure 46 Module Standby Register 1 (MSR1)

### Timer C

**Timer C Functions:** Timer C has the following functions.

- Free-running/reload timer
- Watchdog timer
- Timer output operation (toggle output, PWM output)

The block diagram of timer C is shown in figure 47.

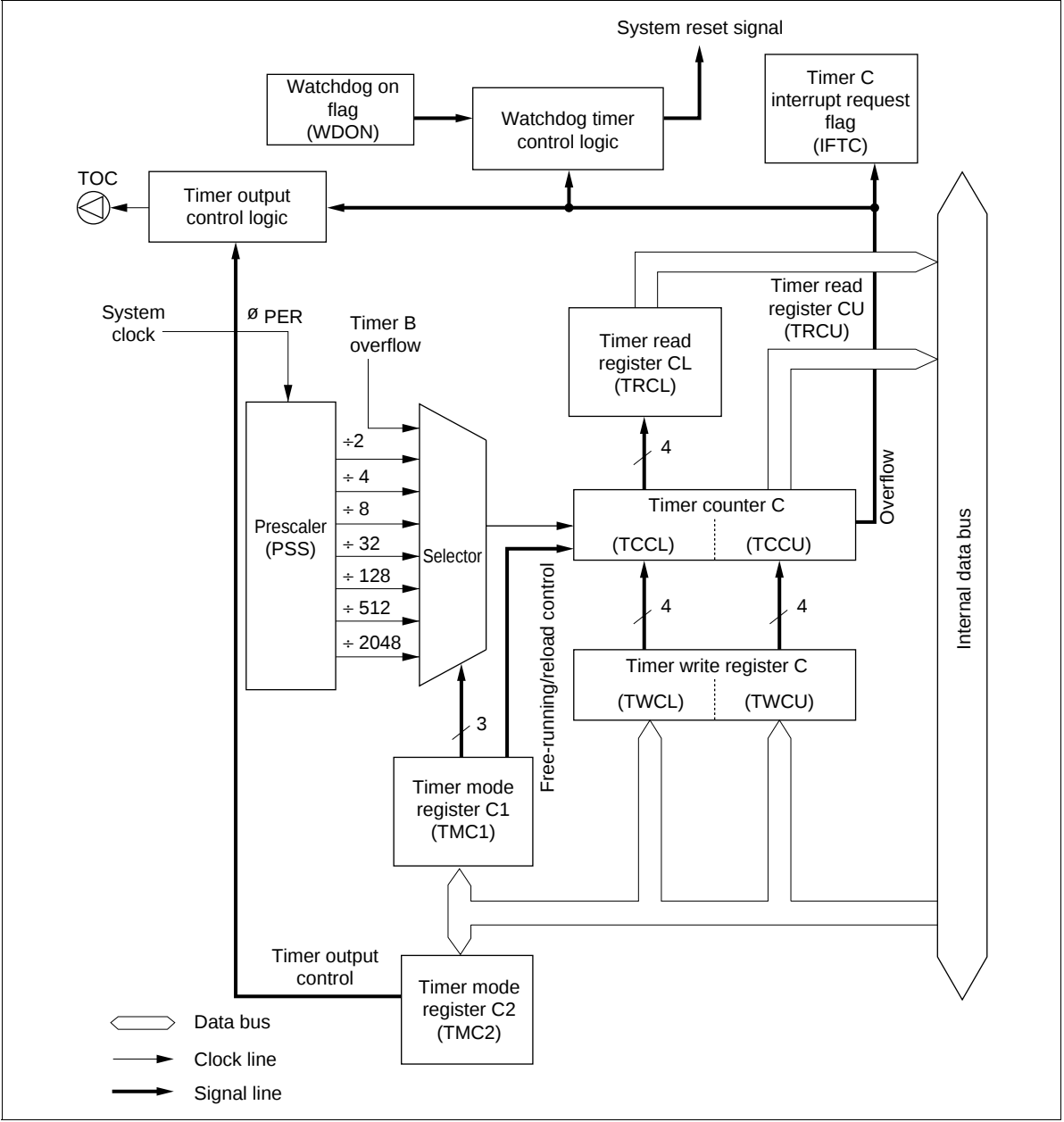


Figure 47 Timer C Block Diagram

## Timer C Operation

- Free-running/reload timer:

Free-running/reload timer operation, the input clock source, and the prescaler division ratio are selected by means of timer mode register C1 (TMC1).

Timer C is initialized to the value written to timer write register C (TWCL, TWCU) by software, and counts up by 1 each time the input clock is input. When the input clock is input after the timer C value reaches \$FF, overflow output is generated. Timer C is then set to the value in timer write register C (TWCL, TWCU) if the reload timer function is selected, or to \$00 if the free-running timer function is selected, and starts counting up again.

Overflow output sets the timer C interrupt request flag (IFTC). This flag is reset by the program or by an MCU reset.

For details, see figure 3, Interrupt Control Bit and Register Flag Area Configuration, and table 1, Initial Values after MCU Reset.

- 16-bit timer operation:

When timer B overflow flag is selected as the clock source, timer C can be used as a 16-bit timer that counts the timer B clock source pulses. In this case, since the timer B and timer C free-running/reload settings are independent, the settings should be made to suit the purpose.

- Watchdog timer operation:

By using the timer C overflow output, timer C can be used as a watchdog timer for detecting program runaway. The watchdog timer is enabled when the watchdog on flag (WDON) is set to 1, and generates an MCU reset when timer C overflows. Usually, timer C initialization is performed by the program before the timer C value reaches \$FF, so controlling program runaway.

- Timer output operation:

With timer C, the R2<sub>0</sub>/TOC pin is designated as the TOC pin by setting bit 0 of port mode register 3 (PMR3) to 1, and toggle waveform output or PWM waveform output can be selected by timer mode register C2 (TMC2).

- Toggle output

The operation is similar to that for timer B toggle output.

- PWM output

The operation is similar to that for timer B PWM output.

- Module standby:

The operation is similar to that for timer B module standby.

## **Timer C Registers**

Timer C operation setting and timer C value reading/writing is controlled by the following registers.

Timer mode register C1 (TMC1: \$014)

Timer mode register C2 (TMC2: \$015)

Timer write register C (TWCL: \$016, TWCU: \$017)

Timer read register C (TRCL: \$016, TRCU: \$017)

Port mode register 3 (PMR3: \$00B)

Module standby register 1 (MSR1: \$00D)

- **Timer mode register C1 (TMC1: \$014):**

Timer mode register C1 (TMC1) is a 4-bit write-only register, used to select free-running/reload timer operation, the input clock, and the prescaler division ratio as shown in figure 48.

Timer mode register C1 (TMC1) is reset to \$0 by an MCU reset.

A modification of timer mode register C1 (TMC1) becomes effective after execution of two instructions following the timer mode register C1 (TMC1) write instruction. The program must provide for timer C initialization by writing to timer write register C (TWCL, TWCU) to be executed after the post-modification mode has become effective.

Timer mode register C1 (TMC1: \$014)

| Bit                    | 3     | 2     | 1     | 0     |
|------------------------|-------|-------|-------|-------|
| Read/Write             | W     | W     | W     | W     |
| Initial value on reset | 0     | 0     | 0     | 0     |
| Bit name               | TMC13 | TMC12 | TMC11 | TMC10 |

|   | TMC12 | TMC11 | TMC10 | Input clock period     |
|---|-------|-------|-------|------------------------|
| 0 | 0     | 0     | 0     | 2,048 t <sub>cyc</sub> |
|   |       |       | 1     | 512 t <sub>cyc</sub>   |
|   | 1     | 0     | 0     | 128 t <sub>cyc</sub>   |
|   |       |       | 1     | 32 t <sub>cyc</sub>    |
| 1 | 0     | 0     | 0     | 8 t <sub>cyc</sub>     |
|   |       |       | 1     | 4 t <sub>cyc</sub>     |
|   | 1     | 0     | 0     | 2 t <sub>cyc</sub>     |
|   |       |       | 1     | Timer B overflow       |

| TMC13 | Free-running/reload timer |
|-------|---------------------------|
| 0     | Free-running timer        |
| 1     | Reload timer              |

Figure 48 Timer Mode Register C1 (TMC1)

• Timer mode register C2 (TMC2: \$015):

Timer mode register C2 (TMC2) is a 1-bit write-only register, used to select the timer C output mode as shown in figure 49.

Timer mode register C2 (TMC2) is reset to \$0 by an MCU reset.

| Timer mode register C2 (TMC2: \$015) |   |       |   |   |
|--------------------------------------|---|-------|---|---|
| Bit                                  | 3 | 2     | 1 | 0 |
| Read/Write                           | — | W     | — | — |
| Initial value on reset               | — | 0     | — | — |
| Bit name                             | — | TMC22 | — | — |

↑

| TMC22 | Timer C output waveform |
|-------|-------------------------|
| 0     | Toggle output           |
| 1     | PWM output              |

Figure 49 Timer Mode Register C2 (TMC2)

• Timer write register C (TWCL: \$016, TWCU: \$017):

Timer write register C (TWCL, TWCU) is a write-only register composed of a lower digit (TWCL) and an upper digit (TWCU) (figures 50 and 51).

Timer write register C (TWCL, TWCU) operation is similar to that for timer write register B (TWBL, TWBU).

| Timer write register C (lower) (TWCL: \$016) |       |       |       |       |
|----------------------------------------------|-------|-------|-------|-------|
| Bit                                          | 3     | 2     | 1     | 0     |
| Read/Write                                   | W     | W     | W     | W     |
| Initial value on reset                       | 0     | 0     | 0     | 0     |
| Bit name                                     | TWCL3 | TWCL2 | TWCL1 | TWCL0 |

Figure 50 Timer Write Register C (Lower) (TWCL)

Timer write register C (upper) (TWCU: \$017)

| Bit                    | 3            | 2            | 1            | 0            |
|------------------------|--------------|--------------|--------------|--------------|
| Read/Write             | W            | W            | W            | W            |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name               | TWCU3        | TWCU2        | TWCU1        | TWCU0        |

Figure 51 Timer Write Register C (Upper) (TWCU)

- Timer read register C (TRCL: \$016, TRCU: \$017):  
Timer read register C (TRCL, TRCU) is a read-only register composed of a lower digit (TRCL) and an upper digit (TRCU) from which the value of the upper digit of timer C is read directly (figures 52 and 53).  
Timer read register C (TRCL, TRCU) operation is similar to that for timer read register B (TRBL, TRBU).

Timer read register C (lower) (TRCL: \$016)

| Bit                    | 3            | 2            | 1            | 0            |
|------------------------|--------------|--------------|--------------|--------------|
| Read/Write             | R            | R            | R            | R            |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name               | TRCL3        | TRCL2        | TRCL1        | TRCL0        |

Figure 52 Timer Read Register C (Lower) (TRCL)

Timer read register C (upper) (TRCU: \$017)

| Bit                    | 3            | 2            | 1            | 0            |
|------------------------|--------------|--------------|--------------|--------------|
| Read/Write             | R            | R            | R            | R            |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name               | TRCU3        | TRCU2        | TRCU1        | TRCU0        |

Figure 53 Timer Read Register C (Upper) (TRCU)

• Port mode register 3 (PMR3: \$00B):

Port mode register 3 (PMR3) is a write-only register used to set the function of the R2<sub>0</sub>/TOC pin as shown in figure 54.

Port mode register 3 (PMR3) is reset to \$0 by an MCU reset.

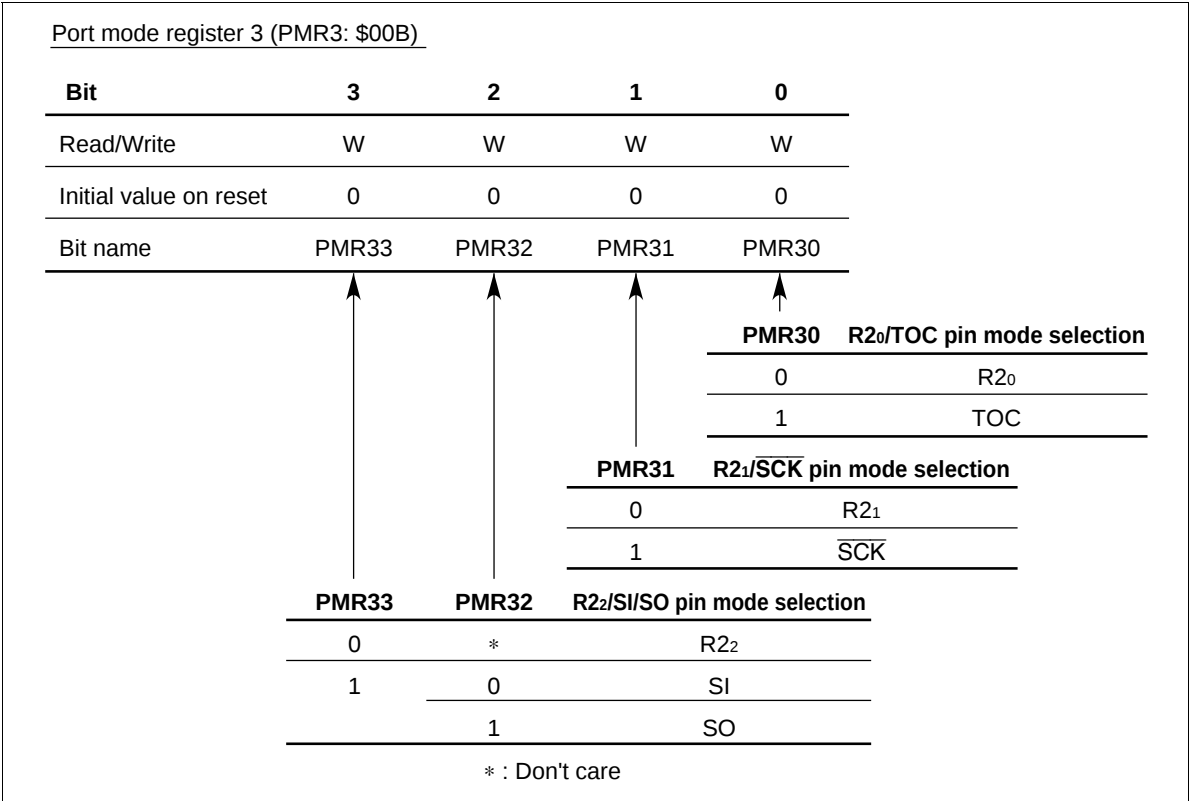


Figure 54 Port Mode Register 3 (PMR3)

• Module standby register 1 (MSR1: \$00D):

Module standby register 1 (MSR1) is a write-only register used to designate supply or stopping of the clock to timer C as shown in figure 46.

Module standby register 1 (MSR1) is reset to \$0 by an MCU reset.

### Timer D (HD404889/HD404899/HD404878 Series)

**Timer D functions :** Timer D has the following functions.

- Free-running/reload timer
- External event counter
- Input capture timer

Block diagrams of timer D in different operating modes are shown in figures 55-1 and 55-2.

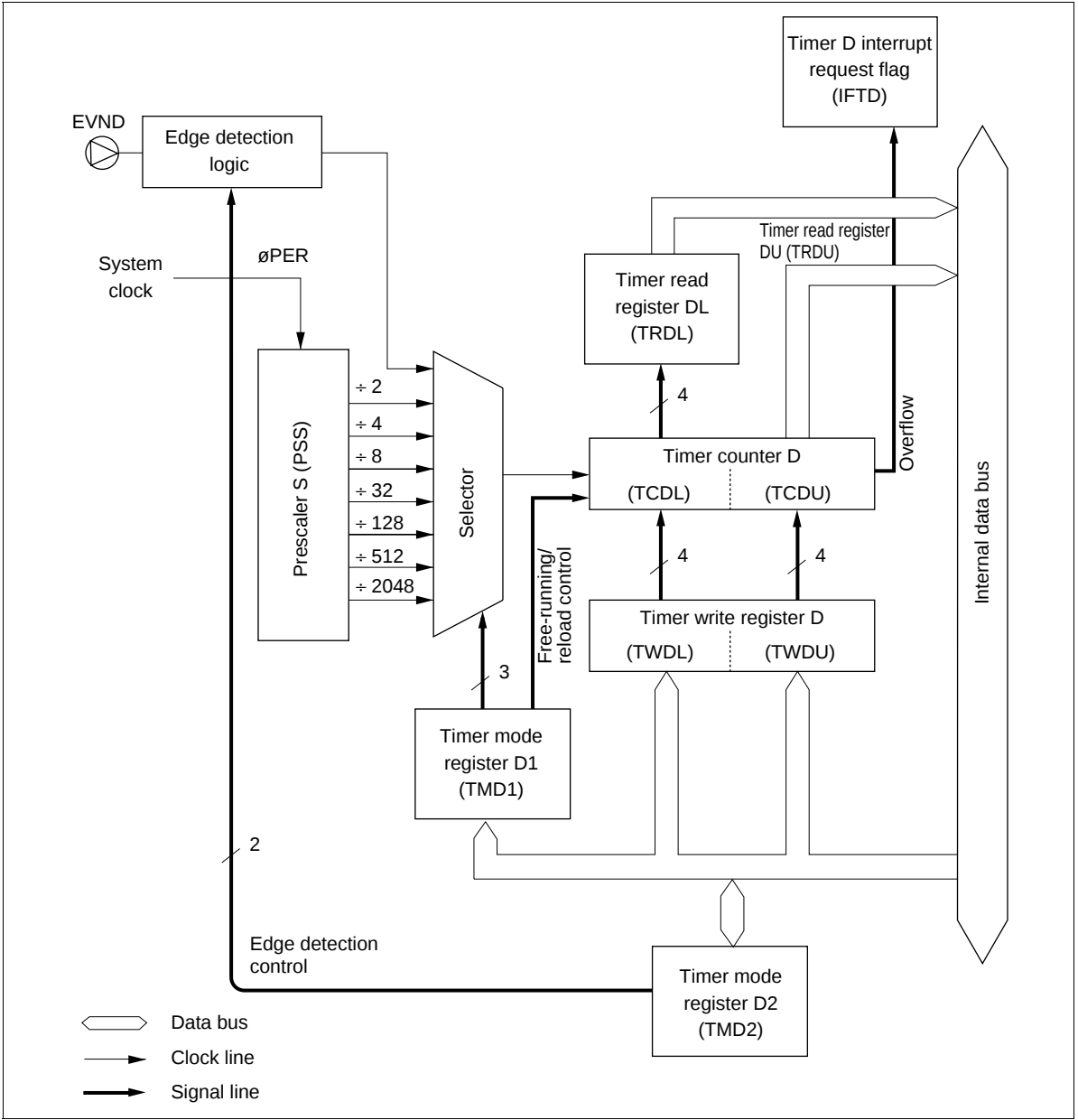


Figure 55-1 Timer D Block Diagram (Reload Timer and Event Counter Modes)

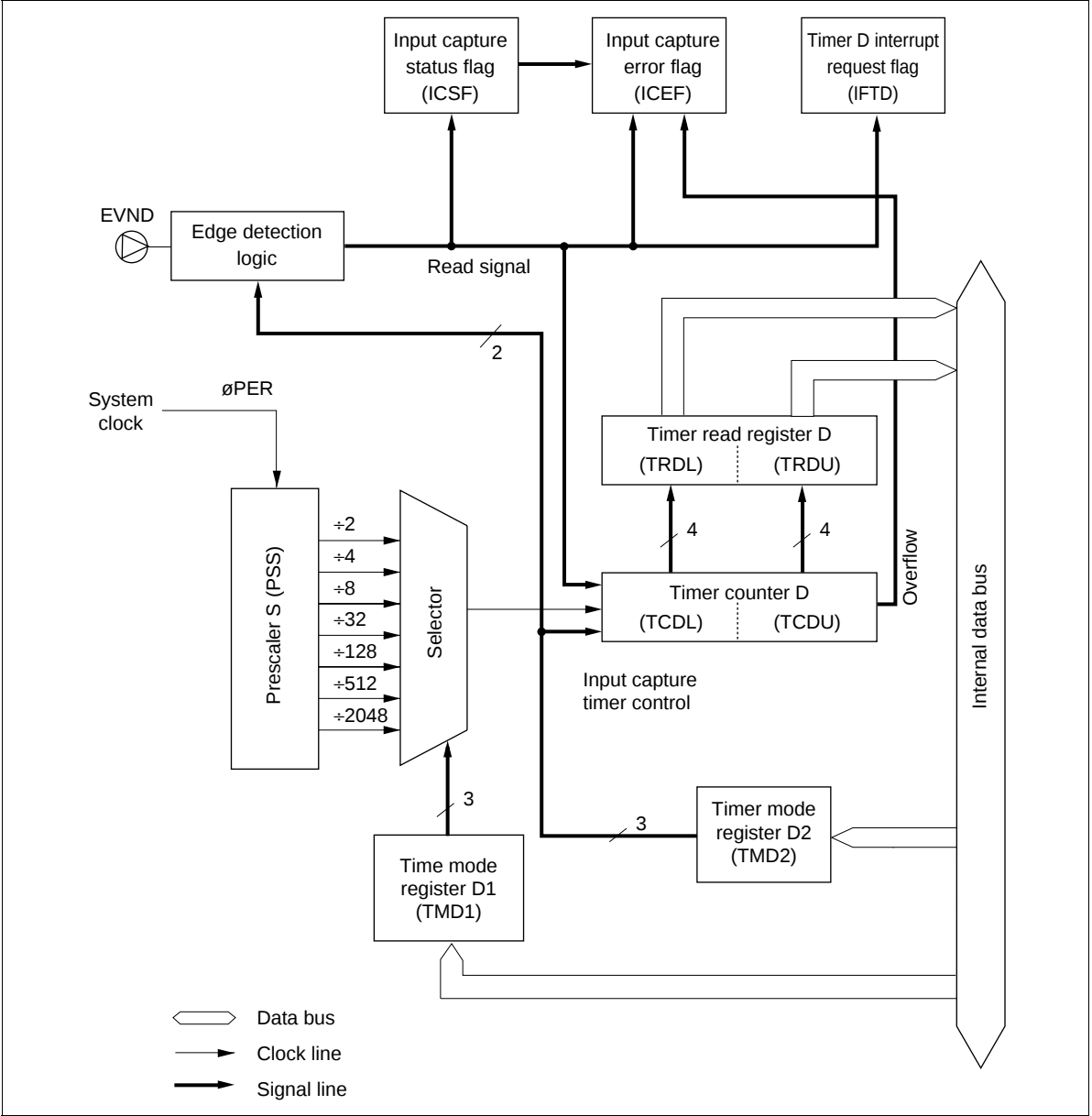


Figure 55-2 Timer D Block Diagram (Input Capture Timer Mode)

## Timer D Operation

- Free-running/reload timer:

Free-running/reload timer operation, the input clock source, and the prescaler division ratio are selected by means of timer mode register D1 (TMD1).

Timer D is initialized to the value written to timer write register D (TWDL, TWDU) by software, and counts up by 1 each time the input clock is input. When the input clock is input after the timer D value reaches \$FF, overflow output is generated. Timer D is then set to the value in timer write register D (TWDL, TWDU) if the reload timer function is selected, or to \$00 if the free-running timer function is selected, and starts counting up again.

Overflow output sets the timer D interrupt request flag (IFTD). This flag is reset by the program or by an MCU reset. For details, see figure 3, Interrupt Control Bit and Register Flag Area Configuration, and table 1, Initial Values after MCU Reset.

- External event counter operation:

When external event input is designated for the input clock, timer D operates as an external event counter. When external event input is used, the R1<sub>1</sub>/EVND pin is designated as the EVND pin by port mode register 2 (PMR2).

The external event detected edge for timer D can be designated as a falling edge, rising edge, or both falling and rising edges in the input signal by means of timer mode register D2 (TMD2). If both falling and rising edges are selected, the input signal falling and rising edge interval should be at least 2tcyc.

Timer D counts up by 1 each time the edge selected by timer mode register D2 (TMD2) is detected. Other operations are the same as for the free-running/reload timer function.

- Input capture timer operation:

The input capture timer function is used to measure the time between trigger input edges input at the EVND pin.

The trigger input edge can be designated as a falling edge, rising edge, or both falling and rising edges by means of timer mode register D2 (TMD2).

When a trigger input edge is detected at the EVND pin, the current timer D value is stored in timer read register D (TRDL, TRDU), and the timer D interrupt request flag (IFTD) and input capture status flag (ICSF) are set. At the same time, timer D is reset to \$00 and continues counting up.

If the next trigger input edge is input while the input capture status flag (ICSF) is set, or if timer D overflows, the input capture error flag (ICEF) is set.

The input capture status flag (ICSF) and input capture error flag (ICEF) are reset to 0 by an MCU reset or by writing 0 to them.

When timer D is set to operate as an input capture timer, it is reset to \$00.

**Timer D Registers:** Timer D operation setting and timer D value reading/writing is controlled by the following registers.

Timer mode register D1 (TMD1: \$018)

Timer mode register D2 (TMD2: \$019)

Timer write register D (TWDL: \$01A, TWDU: \$01B)

Timer read register D (TRDL: \$01A, TRDU: \$01B)

Port mode register 2 (PMR2: \$00A)

Module standby register 1 (MSR1: \$00D)

- Timer mode register D1 (TMD1: \$018):

Timer mode register D1 (TMD1) is a 4-bit write-only register, used to select free-running/reload timer operation, the input clock, and the prescaler division ratio as shown in figure 56.

Timer mode register D1 (TMD1) is reset to \$0 by an MCU reset.

A modification of timer mode register D1 (TMD1) becomes effective after execution of two instructions following the timer mode register D1 (TMD1) write instruction. The program must provide for timer D initialization by writing to timer write register D (TWDL, TWDU) to be executed after the post-modification mode has become effective.

When timer D is set to operate as an input capture timer, an internal clock should be set as the input clock.

Timer mode register D1 (TMD1: \$018)

| Bit                    | 3     | 2     | 1     | 0     |
|------------------------|-------|-------|-------|-------|
| Read/Write             | W     | W     | W     | W     |
| Initial value on reset | 0     | 0     | 0     | 0     |
| Bit name               | TMD13 | TMD12 | TMD11 | TMD10 |

TMD12

TMD11

TMD10

Input clock period and input clock source

|   |   |   |                                 |
|---|---|---|---------------------------------|
| 0 | 0 | 0 | 2,048 t <sub>cyc</sub>          |
|   |   | 1 | 512 t <sub>cyc</sub>            |
|   | 1 | 0 | 128 t <sub>cyc</sub>            |
|   |   | 1 | 32 t <sub>cyc</sub>             |
| 1 | 0 | 0 | 8 t <sub>cyc</sub>              |
|   |   | 1 | 4 t <sub>cyc</sub>              |
|   | 1 | 0 | 2 t <sub>cyc</sub>              |
|   |   | 1 | R11/EVND (external event input) |

|       |                           |
|-------|---------------------------|
| TMD13 | Free-running/reload timer |
| 0     | Free-running timer        |
| 1     | Reload timer              |

Figure 56 Timer Mode Register D1 (TMD1)

- Timer mode register D2 (TMD2: \$019):  
Timer mode register D2 (TMD2) is a 3-bit write-only register, used to select the EVND pin detected edge and input capture operation as shown in figure 57.  
Timer mode register D2 (TMD2) is reset to \$0 by an MCU reset.

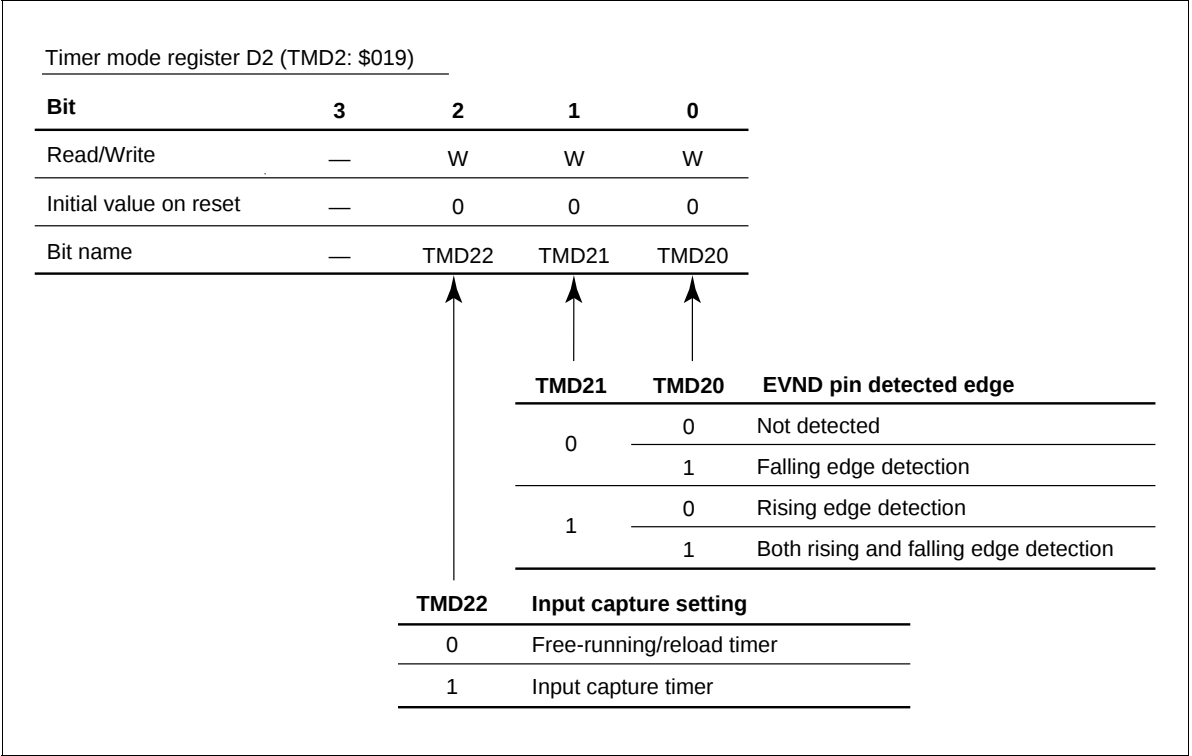


Figure 57 Timer Mode Register D2 (TMD2)

- Timer write register D (TWDL: \$01A, TWDU: \$01B):  
Timer write register D (TWDL, TWDU) is a write-only register composed of a lower digit (TWDL) and an upper digit (TWDU) (figures 58 and 59).  
Timer write register D (TWDL, TWDU) operation is similar to that for timer write register B (TWBL, TWBU).

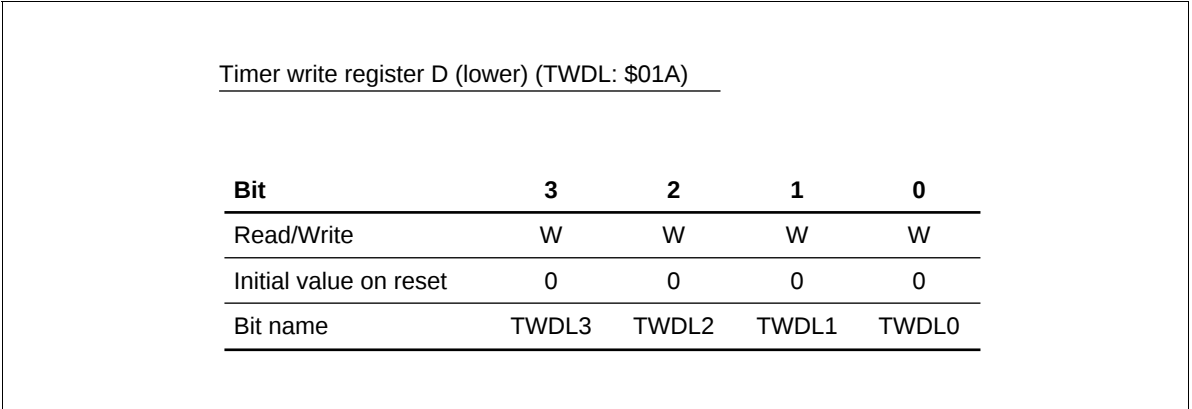


Figure 58 Timer Write Register D (Lower) (TWDL)

Timer write register D (upper) (TWDU: \$01B)

| Bit                    | 3            | 2            | 1            | 0            |
|------------------------|--------------|--------------|--------------|--------------|
| Read/Write             | W            | W            | W            | W            |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name               | TWDU3        | TWDU2        | TWDU1        | TWDU0        |

**Figure 59 Timer Write Register D (Upper) (TWDU)**

- Timer read register D (TRDL: \$01A, TRDU: \$01B):

Timer read register D (TRDL, TRDU) is a read-only register composed of a lower digit (TRDL) and an upper digit (TRDU) (figures 60 and 61).

Timer read register D (TRDL, TRDU) operation is similar to that for timer read register B (TRBL, TRBU).

In the input capture timer operating mode, when the timer D value is read after trigger input, it does not matter whether the lower or upper digit is read first.

Timer read register D (lower) (TRDL: \$01A)

| Bit                    | 3            | 2            | 1            | 0            |
|------------------------|--------------|--------------|--------------|--------------|
| Read/Write             | R            | R            | R            | R            |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name               | TRDL3        | TRDL2        | TRDL1        | TRDL0        |

**Figure 60 Timer Read Register D (Lower) (TRDL)**

Timer read register D (upper) (TRDU: \$01B)

| Bit                    | 3            | 2            | 1            | 0            |
|------------------------|--------------|--------------|--------------|--------------|
| Read/Write             | R            | R            | R            | R            |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name               | TRDU3        | TRDU2        | TRDU1        | TRDU0        |

**Figure 61 Timer Read Register D (Upper) (TRDU)**

- Port mode register 2 (PMR2: \$00A):

Port mode register 2 (PMR2) is a write-only register used to set the R1<sub>1</sub>/EVND pin function as shown in figure 45.

Port mode register 2 (PMR2) is reset to \$0 by an MCU reset.

- Module standby register 1 (MSR1: \$00D):

Module standby register 1 (MSR1) is a write-only register used to designate supply or stopping of the clock to timer D as shown in figure 46.

Module standby register 1 (MSR1) is reset to \$0 by an MCU reset.

## **Serial Interface**

The serial interface serially transfers and receives 8-bit data, and includes the following features.

- Multiple transmit clock sources
  - External clock
  - Internal prescaler output clock
  - System clock
- Output level control in idle states

Five registers, an octal counter, and a multiplexer are also configured for the serial interface as follows.

- Serial data register (SRL: \$026, SRU: \$027)
- Serial mode register 1 (SMR1: \$024)
- Serial mode register 2 (SMR2: \$025)
- Port mode register 3 (PMR3: \$00B)
- Octal counter (OC)
- Selector

The block diagram of the serial interface is shown in figure 62.

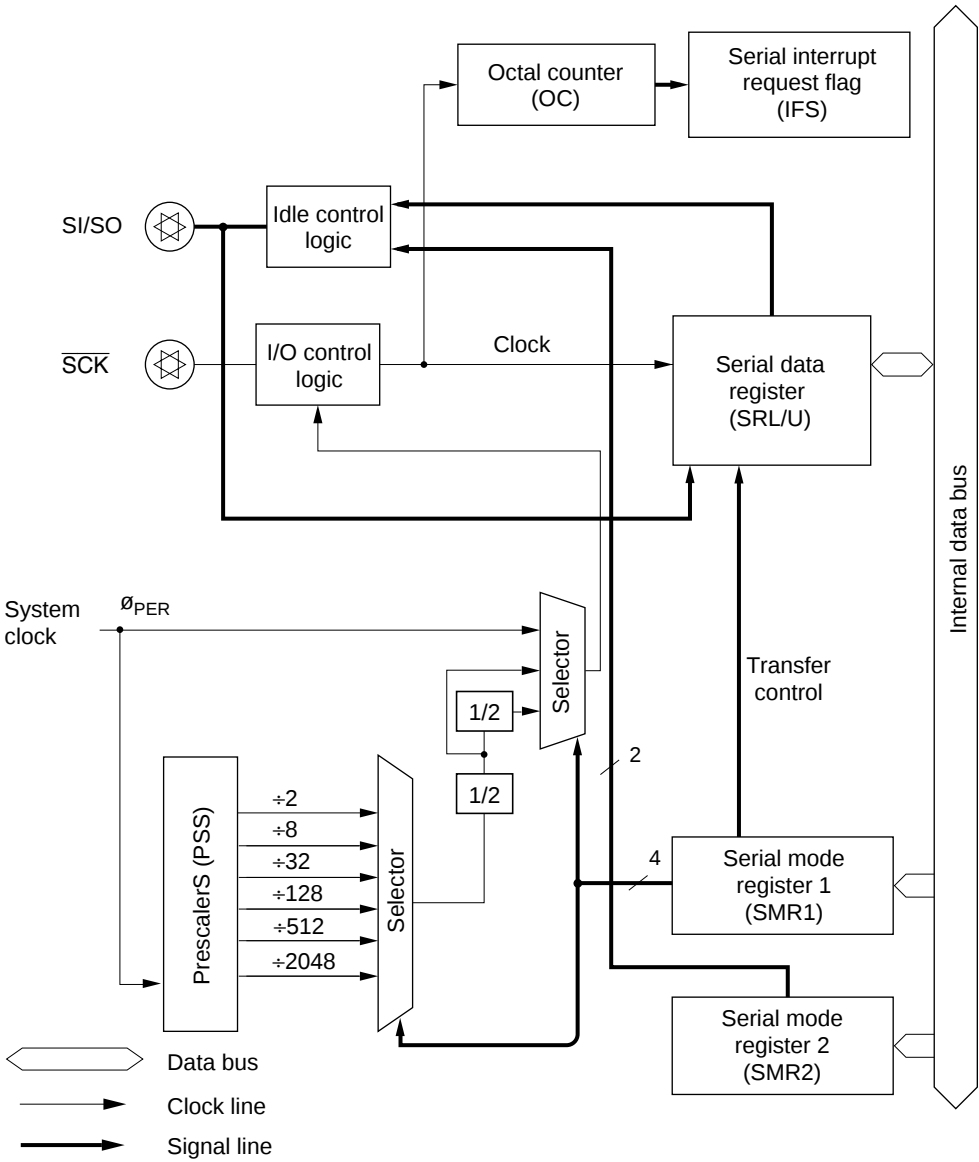


Figure 62 Serial Interface Block Diagram

## Serial Interface Operation

### Selecting and changing serial interface operating mode:

The operating modes that can be selected for the serial interface are shown in table 26. The combination of port mode register 3 (PMR3) values should be selected from this table. When the serial interface operating mode is changed, the serial interface internal state must be initialized by writing to serial mode register 1 (SMR1).

Note : The serial interface is initialized by writing to serial mode register 1 (SMR1: \$024). See serial mode register 1 for details.

**Table 26 Serial Interface Operating Modes**

| PMR3 |      |      | Serial interface operating mode |
|------|------|------|---------------------------------|
| Bit3 | Bit2 | Bit1 |                                 |
| 0    | *    | 1    | Clock continuous output mode    |
| 1    | 0    | 1    | Receive mode                    |
| 1    | 1    | 1    | Transmit mode                   |

\*: Don't care

### Serial interface pin setting:

The R2<sub>1</sub>/SCK pin and R2<sub>2</sub>/SI/SO pin are set by writing data to port mode register 3 (PMR3). See serial interface registers for details.

### Serial clock source setting:

The serial clock is set by writing data to serial mode register 1 (SMR1). See serial interface registers for details.

### Serial data setting:

Transmit serial data is set by writing data to the serial data register (SRL, SRU).

Receive serial data is obtained by reading the serial data register (SRL, SRU). Serial data is shifted by means of the serial clock to perform input/output from/to an external device.

The output level of the SO pin is undetermined until the first data is output after a reset by the MCU, or until high/low control is performed in the idle state.

### Transfer control:

Serial interface operation is started by an STS instruction. The octal counter is reset to 000 by the STS instruction, and is incremented by 1 on each rise of the serial clock. When 8 serial clock pulses have been input, or if data transmission/reception is suspended midway, the octal counter is reset to 000, the serial interrupt request flag (IFS) is set, and transfer is terminated.

The serial clock is selected by means of serial mode register 1 (SMR1). See figure 66.

**Serial interface operating states:**

The serial interface has the operating states shown in figure 63 in external clock mode and internal clock mode.

STS instruction wait state  
Serial clock wait state  
Transfer state  
Clock continuous output state (internal clock mode only)

- STS instruction wait state

Upon MCU reset ((00), (10) in figure 63), the serial interface enters the STS instruction wait state. In the STS instruction wait state, the internal state of the serial interface is initialized. Even if the serial clock is input at this time, the serial interface will not operate. When the STS instruction is executed ((01), (11)), the serial interface enters the serial clock wait state.

- Serial clock wait state

The serial clock wait state is the interval from STS instruction execution until the first serial clock falling edge. When the serial clock is input in the serial clock wait state ((02), (12)), the octal counter begins counting, the contents of the serial data register (SRL) begin shifting, and the serial interface enters the transfer state. However, if clock continuous output mode is selected in internal clock mode, the serial interface enters the clock continuous output state ((17)) instead of the transfer state.

If a write to serial mode register 1 (SMR1) is performed in the serial clock wait state, the serial interface enters the STS instruction wait state ((04), (14)).

- Transfer state

The transfer state is the interval from the first serial clock falling edge until the eighth serial clock rising edge. In the transfer state, if an STS instruction is executed or if eight serial clocks have been input, the octal counter is cleared to 000, and the serial interface makes a state transition. If an STS instruction is executed ((05), (15)), the serial interface enters the serial clock wait state. After eight serial clocks have been input, the serial interface enters the serial clock wait state ((03)) when in external clock mode, and enters the STS instruction wait state ((13)) when in internal clock mode.

In internal clock mode, the serial clock stops after output of eight clocks.

If a write to serial mode register 1 (SMR1) is performed in the transfer state ((06), (16)), the serial interface is initialized and enters the STS instruction wait state.

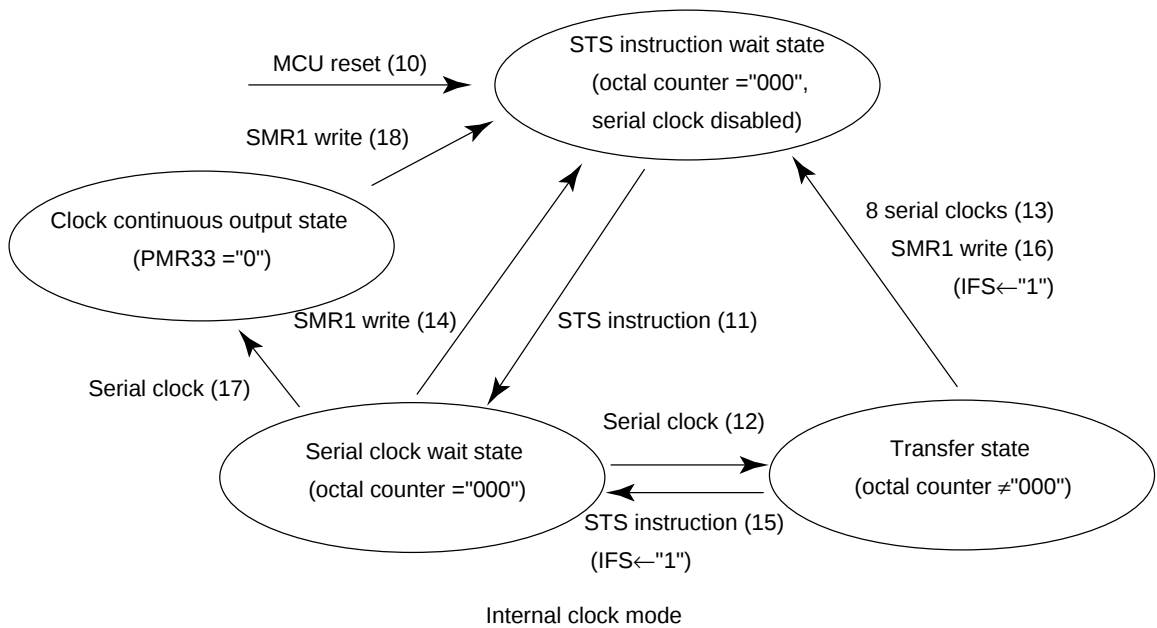
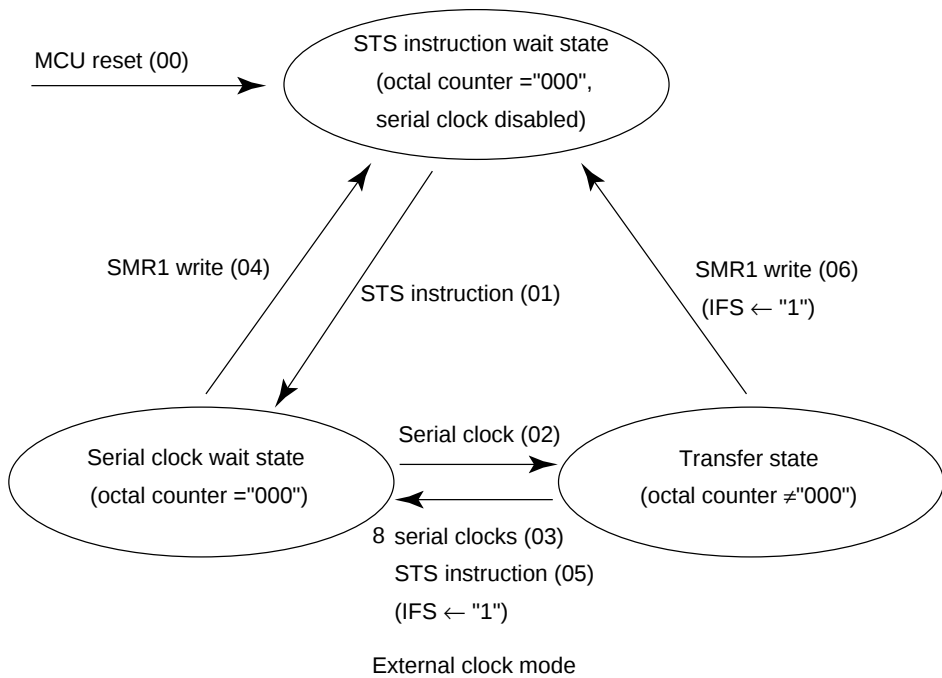
When the serial interface switches from the transfer state to another state, the octal counter is reset to 000 and the serial interrupt request flag (IFS) is set.

- Clock continuous output state (internal clock mode only)

In the clock continuous output state, no receive or transmit operation is performed, and the serial clock is only output from the  $\overline{\text{SCK}}$  pin. It is therefore effective in internal clock mode.

If the serial clock is input ((17)) when bit 3 (PMR33) of port mode register 3 (PMR3) is cleared to 0 and the serial interface is in the serial clock wait state, a transition is made to the clock continuous output state.

If a write to serial mode register 1 (SMR1) is performed in the clock continuous output state ((18)), the serial interface enters the STS instruction wait state.



( ) Refer to the text for details on the circled numbers in the figure.

Figure 63 Serial Interface Operating States

### **Idle high/low control:**

When the serial interface is in the STS instruction wait state or the serial clock wait state (i.e. when idle), the output level of the SO pin can be set arbitrarily by software. Idle high/low control is performed by writing the output level to bit 1 (SMR21) of serial mode register 2 (SMR2).

An example of idle high/low control is shown in figure 64. Idle high/low control cannot be performed in the transfer state.

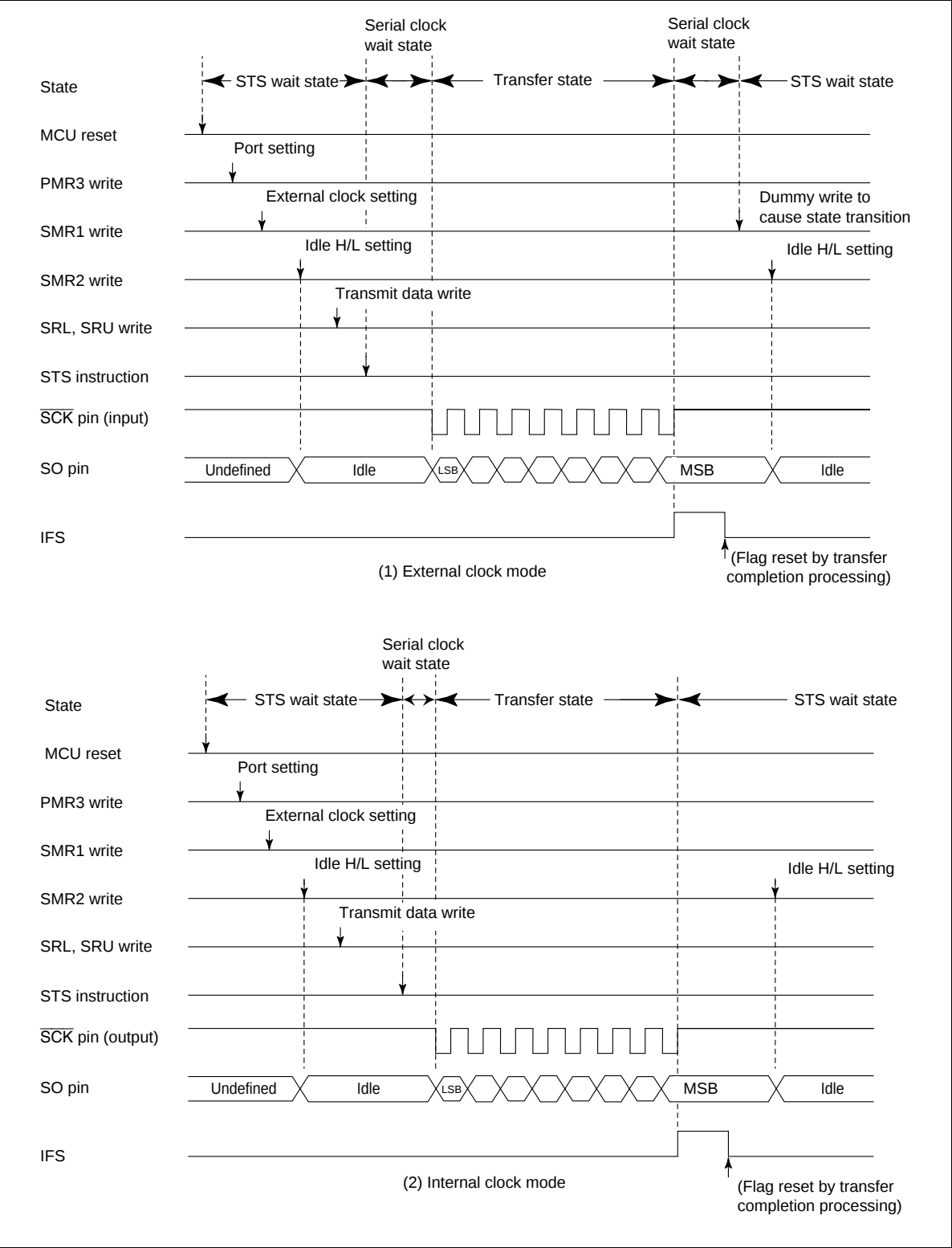


Figure 64 Examples of Serial Interface Operation Sequence

**Serial clock error detection (external clock mode):**

The serial interface will operate incorrectly in the transfer state if external noise results in unnecessary pulses being added to the serial clock. Serial clock error detection in such cases is carried out as shown in figure 65.

If more than eight serial clock pulses are input due to external noise while in the transfer state, at the eighth clock pulse (including any external noise pulses), the octal counter is cleared to 000 and the serial interrupt request flag (IFS) is set. At the same time, the serial interface exits the transfer state and enters the serial clock wait state, but returns to the transfer state at the next regular clock pulse falling edge.

Meanwhile, in the interrupt handling routine, transfer end processing is performed, the serial interrupt request flag is reset, and a dummy write is performed into serial mode register 1 (SMR1). The serial interface then returns to the STS wait state, and the serial interrupt request flag (IFS) is set again. It is therefore possible to detect a serial clock error by testing the serial interrupt request flag after the dummy write to serial mode register 1.

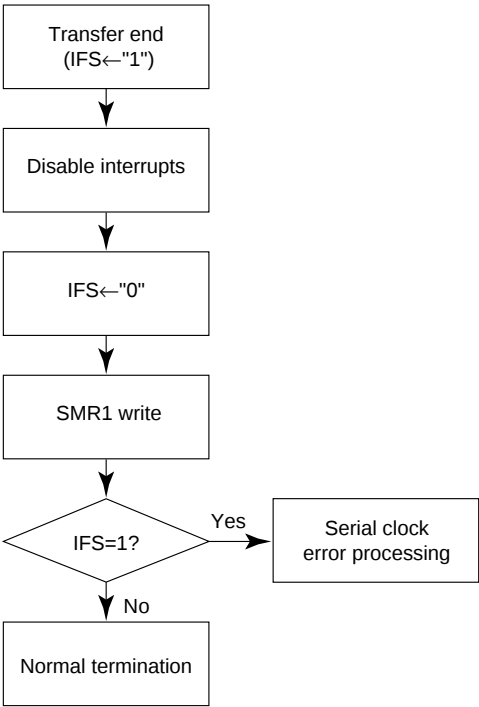
**Usage notes:**

- Initialization after register modification

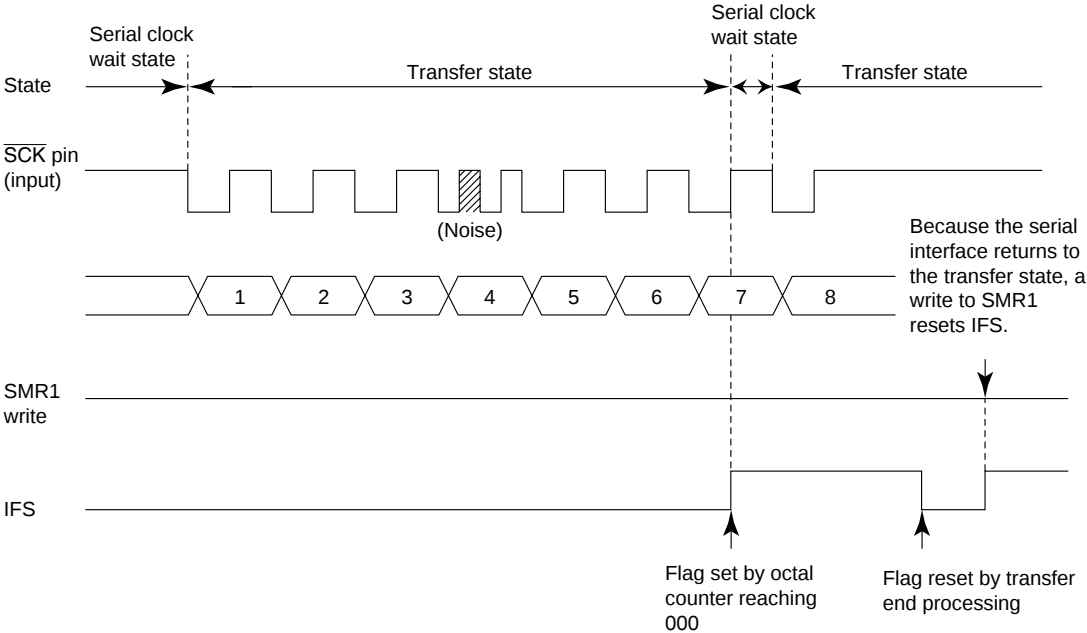
If a port mode register 3 (PMR3) write is performed in the serial clock wait state or transfer state, a serial mode register 1 (SMR1) write should be performed again to initialize the serial interface.

- Serial interrupt request flag (IFS:\$023, 2) setting

If a serial mode register 1 (SMR1) write or STS instruction is executed during the first low-level interval of the serial clock in the transfer state, the serial interrupt request flag (IFS) will not be set. To ensure that the serial interrupt request flag (IFS) is properly set in this case, programming is required to make sure that the  $\overline{\text{SCK}}$  pin is in the 1 state (by executing an input instruction for the R2 port) before executing a serial mode register 1 (SMR1) write or an STS instruction.



(1) Serial clock error detection flowchart



(2) Serial clock error detection sequence

Figure 65 Example of Serial Clock Error Detection

### **Serial Interface Registers**

Serial interface operation setting and serial data reading/writing is controlled by the following registers.

Serial mode register 1 (SMR1: \$024)

Serial mode register 2 (SMR2: \$025)

Serial data register (SRL: \$026, SRU: \$027)

Port mode register 3 (PMR3: \$00B)

Module standby register 2 (MSR2: \$00E)

#### **Serial mode register 1 (SMR1: \$024):**

Serial mode register 1 (SMR1) has the following functions. See figure 66.

- Serial clock selection
- Prescaler division ratio selection
- Serial interface initialization

The serial mode register 1 (SMR1) is a 4-bit write-only register, and is reset to \$0 by an MCU reset.

A write to serial mode register 1 (SMR1) halts the supply of the serial clock to the serial data register (SRL, SRU) and the octal counter, and resets the octal counter to 000. Therefore, if serial mode register 1 (SMR1) is written to during serial interface operation, data transmission/reception will be suspended and the serial interrupt request flag (IFS) will be set.

A modification of serial mode register 1 (SMR1) becomes effective after execution of two instructions following the serial mode register 1 (SMR1) write instruction. The program must therefore provide for the STS instruction to be executed two cycles after the instruction that writes to serial mode register 1 (SMR1).

Serial mode register 1 (SMR1: \$024)

| Bit                    | 3     | 2     | 1     | 0     |
|------------------------|-------|-------|-------|-------|
| Read/Write             | W     | W     | W     | W     |
| Initial value on reset | 0     | 0     | 0     | 0     |
| Bit name               | SMR13 | SMR12 | SMR11 | SMR10 |

| SMR13 | SMR12 | SMR11 | SMR10 | $\overline{\text{SCK}}$ pin | Serial clock source | Serial clock (PSS division ratio $\div 2$ or $4$ ) | Serial clock cycle |
|-------|-------|-------|-------|-----------------------------|---------------------|----------------------------------------------------|--------------------|
| 0     | 0     | 0     | 0     | Output                      | PSS                 | $(\theta_{\text{PER}}/2048)\div 2$                 | 4096 tcyc          |
|       |       | 1     | 0     | Output                      | PSS                 | $(\theta_{\text{PER}}/512)\div 2$                  | 1024 tcyc          |
|       |       | 0     | 1     | Output                      | PSS                 | $(\theta_{\text{PER}}/128)\div 2$                  | 256 tcyc           |
|       |       | 1     | 1     | Output                      | PSS                 | $(\theta_{\text{PER}}/32)\div 2$                   | 64 tcyc            |
|       | 1     | 0     | 0     | Output                      | PSS                 | $(\theta_{\text{PER}}/8)\div 2$                    | 16 tcyc            |
|       |       | 1     | 0     | Output                      | PSS                 | $(\theta_{\text{PER}}/2)\div 2$                    | 4 tcyc             |
|       |       | 0     | 1     | Output                      | System clock        | $\theta_{\text{PER}}$                              | tcyc               |
|       |       | 1     | 1     | Input                       | External clock      | —                                                  | —                  |
| 1     | 0     | 0     | 0     | Output                      | PSS                 | $(\theta_{\text{PER}}/2048)\div 4$                 | 8192 tcyc          |
|       |       | 1     | 0     | Output                      | PSS                 | $(\theta_{\text{PER}}/512)\div 4$                  | 2048 tcyc          |
|       |       | 0     | 1     | Output                      | PSS                 | $(\theta_{\text{PER}}/128)\div 4$                  | 512 tcyc           |
|       |       | 1     | 1     | Output                      | PSS                 | $(\theta_{\text{PER}}/32)\div 4$                   | 128 tcyc           |
|       | 1     | 0     | 0     | Output                      | PSS                 | $(\theta_{\text{PER}}/8)\div 4$                    | 32 tcyc            |
|       |       | 1     | 0     | Output                      | PSS                 | $(\theta_{\text{PER}}/2)\div 4$                    | 8 tcyc             |
|       |       | 0     | 1     | Output                      | System clock        | $\theta_{\text{PER}}$                              | tcyc               |
|       |       | 1     | 1     | Input                       | External clock      | —                                                  | —                  |

Figure 66 Serial Mode Register 1 (SMR1)

Serial mode register 2 (SMR2: \$025):

Serial mode register 2 (SMR2) has the following functions. See figure 67.

- R2<sub>2</sub>/SI/SO pin PMOS control
- Idle high/low control

Serial mode register 2 (SMR2) is a 2-bit write-only register. The register value cannot be modified in the transfer state.

Bit 2 (SMR22) of serial mode register 2 (SMR2) controls the on/off status of the R2<sub>2</sub>/SI/SO pin PMOS. The bit 2 (SMR22) only is reset to 0 by an MCU reset.

Bit 1 (SMR21) of serial mode register 2 (SMR2) performs SO pin high/low control in the idle state. The SO pin changes at the same time as the high/low write.

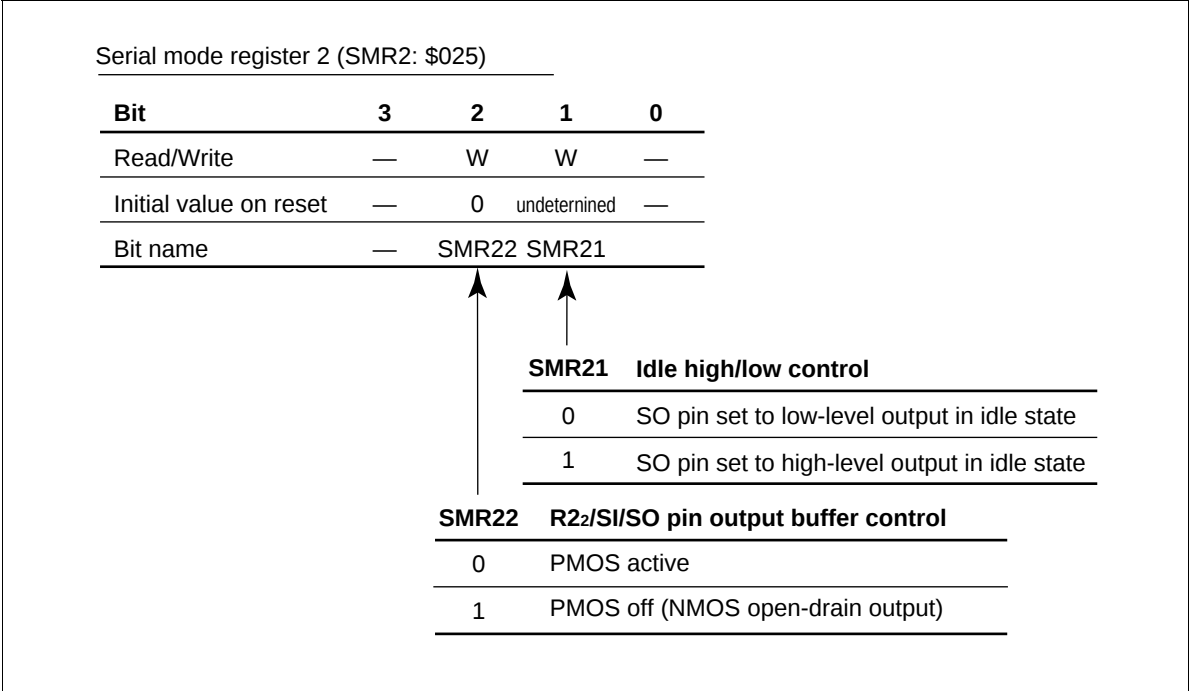


Figure 67 Serial Mode Register 2 (SMR2)

**Serial data register (SRL: \$026, SRU: \$027):**

The serial data register (SRL, SRU) has the following functions. See figures 68 and 69.

- Transmit data write and shift operations
- Receive data shift and read operations

The data written to the serial data register (SRL, SRU) is output LSB-first from the SO pin in synchronization with the falling edge of the serial clock.

External data input LSB-first from the SI pin is latched in synchronization with the rising edge of the serial clock. Figure 70 shows the serial clock and data input/output timing chart.

Writing and reading of the serial data register (SRL, SRU) must be performed only after data transmission/reception is completed. The data contents are not guaranteed if a read or write is performed during data transmission or reception.

Serial data register (lower) (SRL: \$026)

| Bit                    | 3            | 2            | 1            | 0            |
|------------------------|--------------|--------------|--------------|--------------|
| Read/Write             | R/W          | R/W          | R/W          | R/W          |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name               | SR3          | SR2          | SR1          | SR0          |

Figure 68 Serial Data Register (SRL)

Serial data register (upper) (SRU: \$027)

| Bit                    | 3            | 2            | 1            | 0            |
|------------------------|--------------|--------------|--------------|--------------|
| Read/Write             | R/W          | R/W          | R/W          | R/W          |
| Initial value on reset | Undetermined | Undetermined | Undetermined | Undetermined |
| Bit name               | SR7          | SR6          | SR5          | SR4          |

Figure 69 Serial Data Register (SRU)

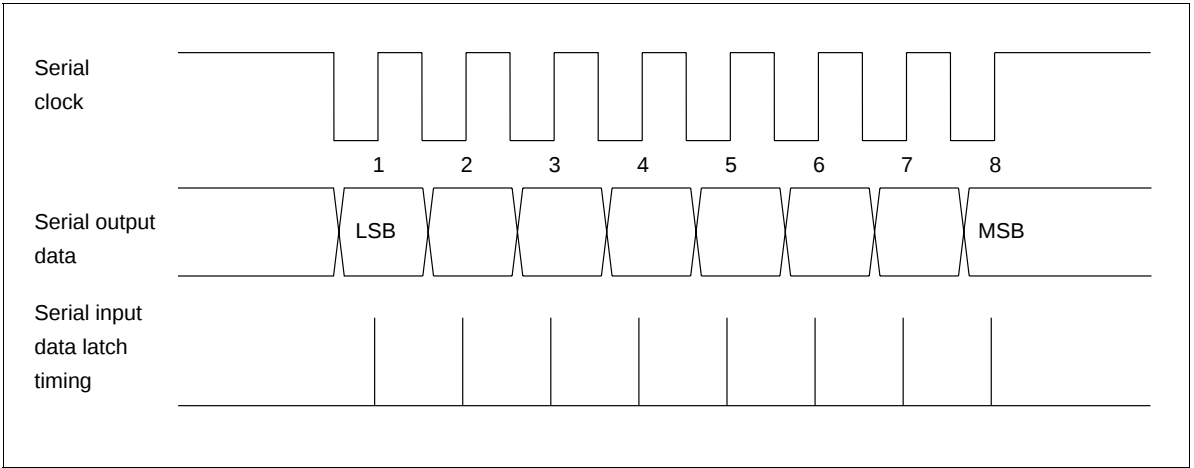


Figure 70 Serial Interface Input/Output Timing Chart

Port mode register 3 (PMR3: \$00B):

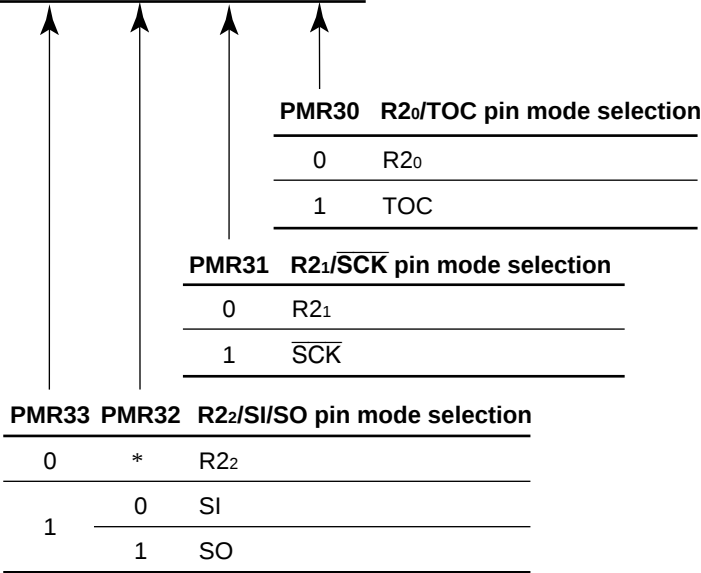
Port mode register 3 (PMR3) has the following functions. See figure 71.

- R2<sub>1</sub>/ $\overline{\text{SCK}}$  pin selection
- R2<sub>2</sub>/SI/SO pin selection

Port mode register 3 (PMR3) is a 4-bit write-only register used to select serial interface pin settings as shown in figure 71. It is reset to \$0 by an MCU reset.

Port mode register 3 (PMR3: \$00B)

| Bit                    | 3     | 2     | 1     | 0     |
|------------------------|-------|-------|-------|-------|
| Read/Write             | W     | W     | W     | W     |
| Initial value on reset | 0     | 0     | 0     | 0     |
| Bit name               | PMR33 | PMR32 | PMR31 | PMR30 |



\* : Don't care

Figure 71 Port Mode Register 3 (PMR3)

Module standby register 2 (MSR2: \$00E):

Module standby register 2 (MSR2) is a write-only register used to designate supply or stopping of the clock to the serial interface as shown in figure 72.

Module standby register 2 (MSR2) is reset to \$0 by an MCU reset.

Module standby register 2 (MSR2: \$00E)

| Bit                    | 3 | 2 | 1     | 0     |
|------------------------|---|---|-------|-------|
| Read/Write             | — | — | W     | W     |
| Initial value on reset | — | — | 0     | 0     |
| Bit name               | — | — | MSR21 | MSR20 |

↑

MSR21 A/D clock supply control

|   |          |
|---|----------|
| 0 | Supplied |
| 1 | Stopped  |

↑

MSR20 Serial clock supply control

|   |          |
|---|----------|
| 0 | Supplied |
| 1 | Stopped  |

Figure 72 Module Standby Register 2 (MSR2)

A/D Converter

HD404889 Series

The MCU has a built-in successive approximation type A/D converter using a resistance ladder method, capable of digital conversion of six analog inputs with an 8-bit resolution. The A/D converter block diagram is shown in figure 73.

The A/D converter comprises the following four registers.

- A/D mode register (AMR: \$028)
- A/D start flag (ADSF: \$020,2)
- A/D data register (ADRL: \$02A, ADRU: \$02B)
- Module standby register 2 (MSR2: \$00E)

Note : Address \$029 is a reserved register, and should not be read or written to.

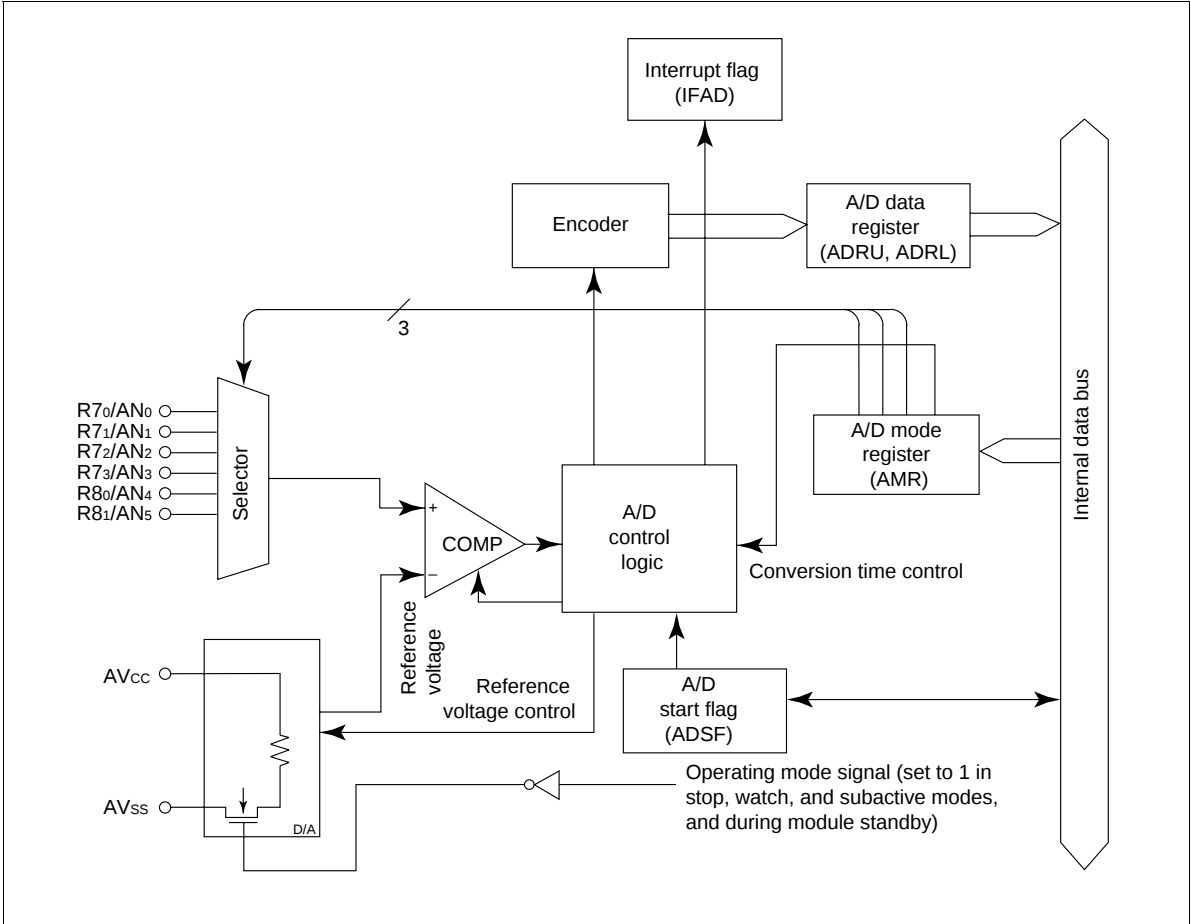


Figure 73 A/D Converter Block Diagram

A/D mode register (AMR: \$028):

The A/D mode register is a 4-bit write-only register that shows the A/D converter speed setting and information on the analog input pin specification. The A/D conversion time is selected by bit 0, and the channel by bits 1, 2, and 3 (figure 74).

A/D start flag (ADSF: \$020,2):

A/D conversion is started by writing 1 to the A/D start flag. When conversion ends, the converted data is placed in the A/D data register and the A/D start flag is cleared at the same time. (figure 75).

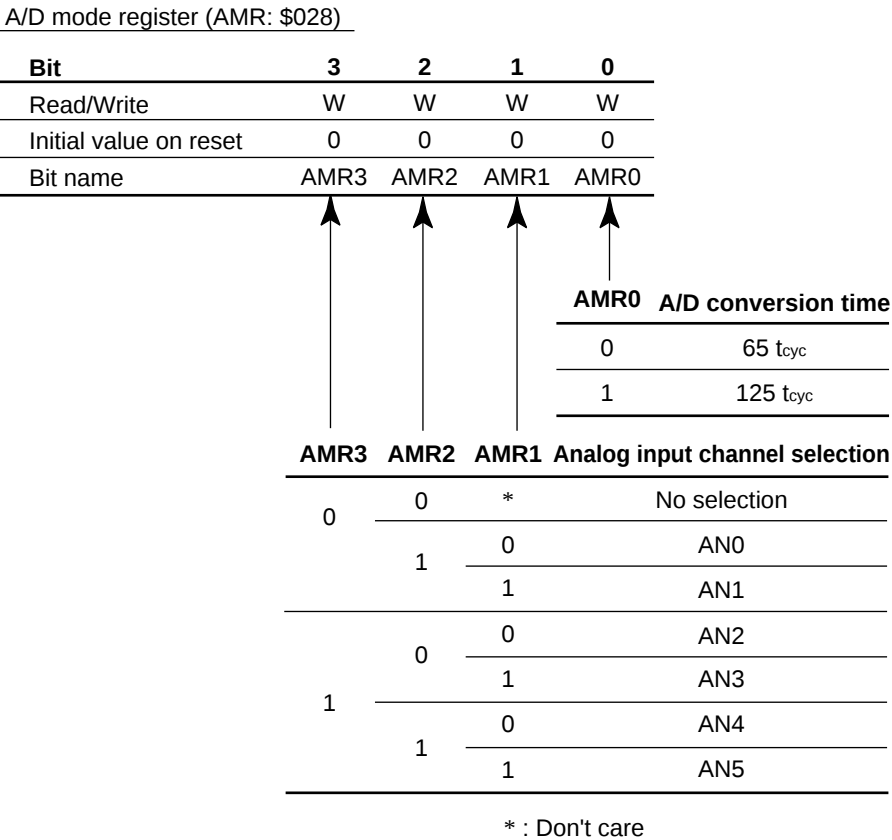


Figure 74 A/D Mode Register (AMR)

A/D start flag (ADSF: \$020,2)

| Bit                    | 3    | 2    | 1    | 0    |
|------------------------|------|------|------|------|
| Read/Write             | R/W  | R/W  | R/W  | R/W  |
| Initial value on reset | 0    | 0    | 0    | 0    |
| Bit name               | DTON | ADSF | WDON | LSON |

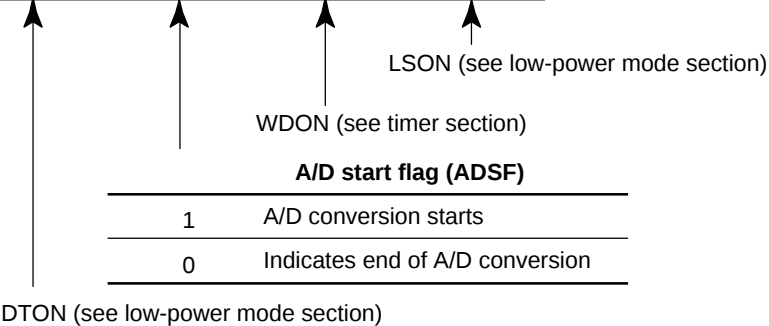


Figure 75 A/D Start Flag (ADSF)

A/D data register (ADRL: \$02A, ADRU: \$02B):

The A/D data register is a read-only register consisting of a lower and upper 4 bits. This register is not cleared by a reset. Also, data read during A/D conversion is not guaranteed. At the end of A/D conversion, the resulting 8-bit data is stored in this register, and is held until the next conversion operation starts (figures 76, 77, and 78).

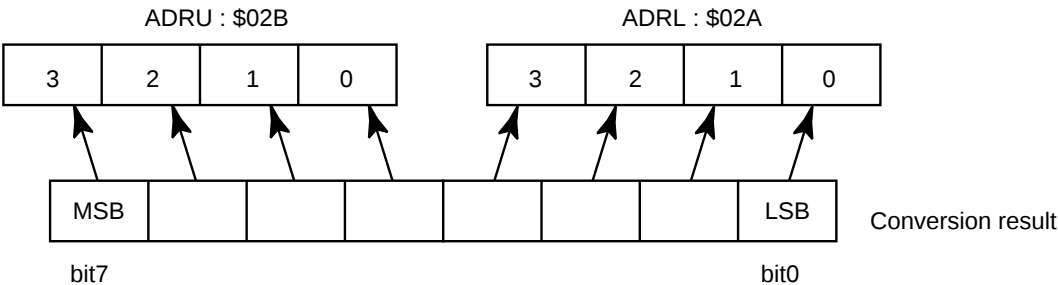


Figure 76 A/D Data Register

A/D data register-lower (ADRL: \$02A)

| Bit                    | 3     | 2     | 1     | 0     |
|------------------------|-------|-------|-------|-------|
| Read/Write             | R     | R     | R     | R     |
| Initial value on reset | 1     | 1     | 1     | 1     |
| Bit name               | ADRL3 | ADRL2 | ADRL1 | ADRL0 |

Figure 77 A/D Data Register-Lower (ADRL)

A/D data register-upper (ADRU: \$02B)

| Bit                    | 3     | 2     | 1     | 0     |
|------------------------|-------|-------|-------|-------|
| Read/Write             | R     | R     | R     | R     |
| Initial value on reset | 0     | 1     | 1     | 1     |
| Bit name               | ADRU3 | ADRU2 | ADRU1 | ADRU0 |

Figure 78 A/D Data Register-Upper (ADRU)

**Module standby register 2 (MSR2: \$00E):**

Writing 1 to bit 1 of module standby register 2 stops the supply of the system clock to the A/D module and cuts the current ( $I_{AD}$ ) flowing in the ladder resistor.

**Usage notes:**

- Use the SEM or SEMD instruction to write to the A/D start flag (ADSF).
- Do not write to the ADSF during A/D conversion.
- Data in the A/D data register is undetermined during A/D conversion.
- As the A/D converter operates on a clock from OSC, it stops in stop mode, watch mode, and subactive mode. The current flowing in the A/D converter ladder resistor is also cut in these low-power modes to reduce power consumption.
- When an analog input pin is selected by the A/D mode register, the pull-up MOS for that pin is disabled.

A/D Converter

HD404899/HD404868 Series

The MCU has a built-in successive approximation type A/D converter using a resistance ladder method, capable of digital conversion of six analog inputs (four analog inputs in the HD404868 Series) with a 10-bit resolution. The A/D converter block diagram is shown in figures 79-1 and 79-2.

The A/D converter comprises the following four registers.

- A/D mode register (AMR: \$028)
- A/D start flag (ADSF: \$020,2)
- A/D data register (ADRL: \$029, ADRM: \$02A, ADRU: \$02B)
- Module standby register 2 (MSR2: \$00E)

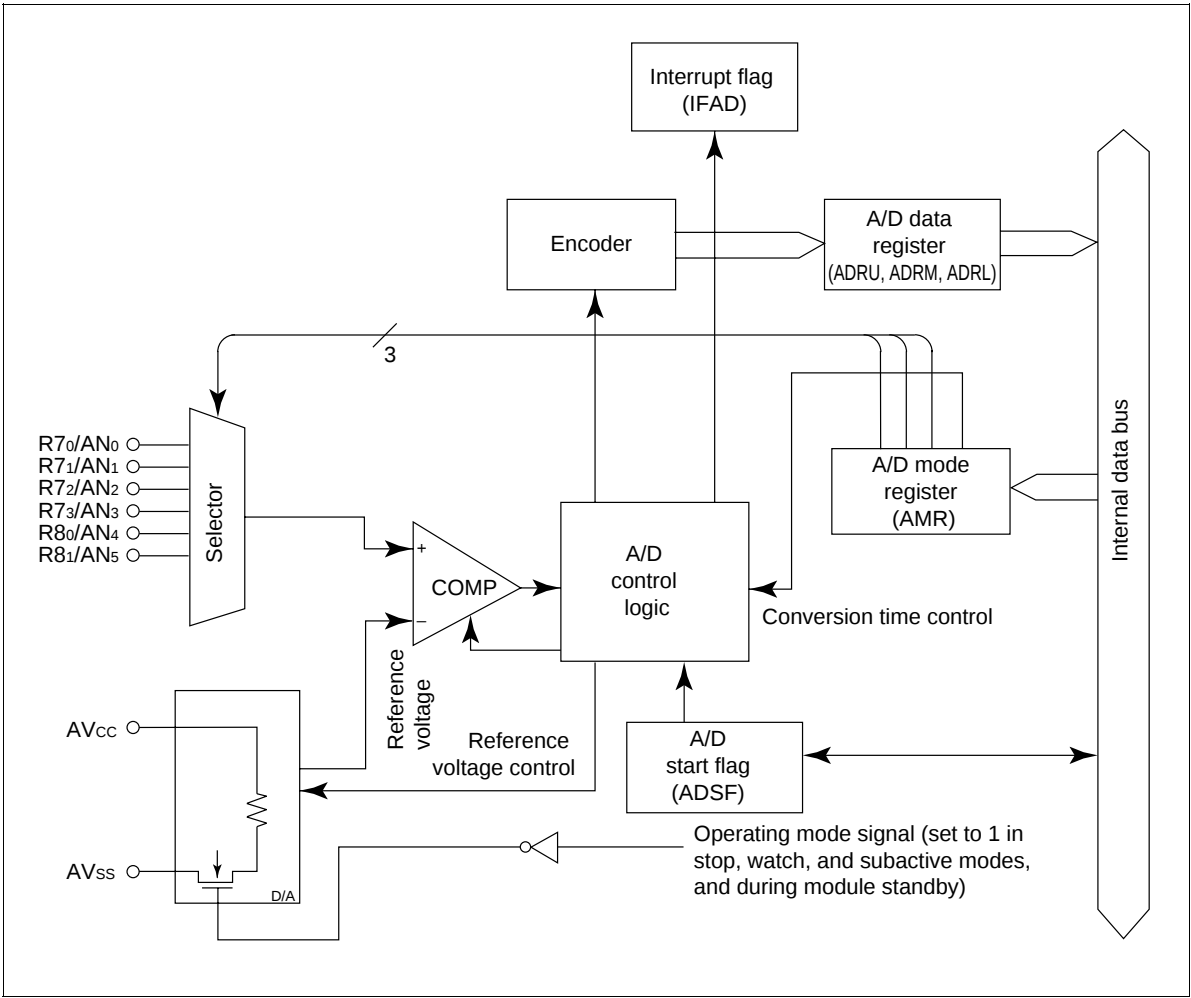


Figure 79-1 A/D Converter Block Diagram (HD404899 Series)

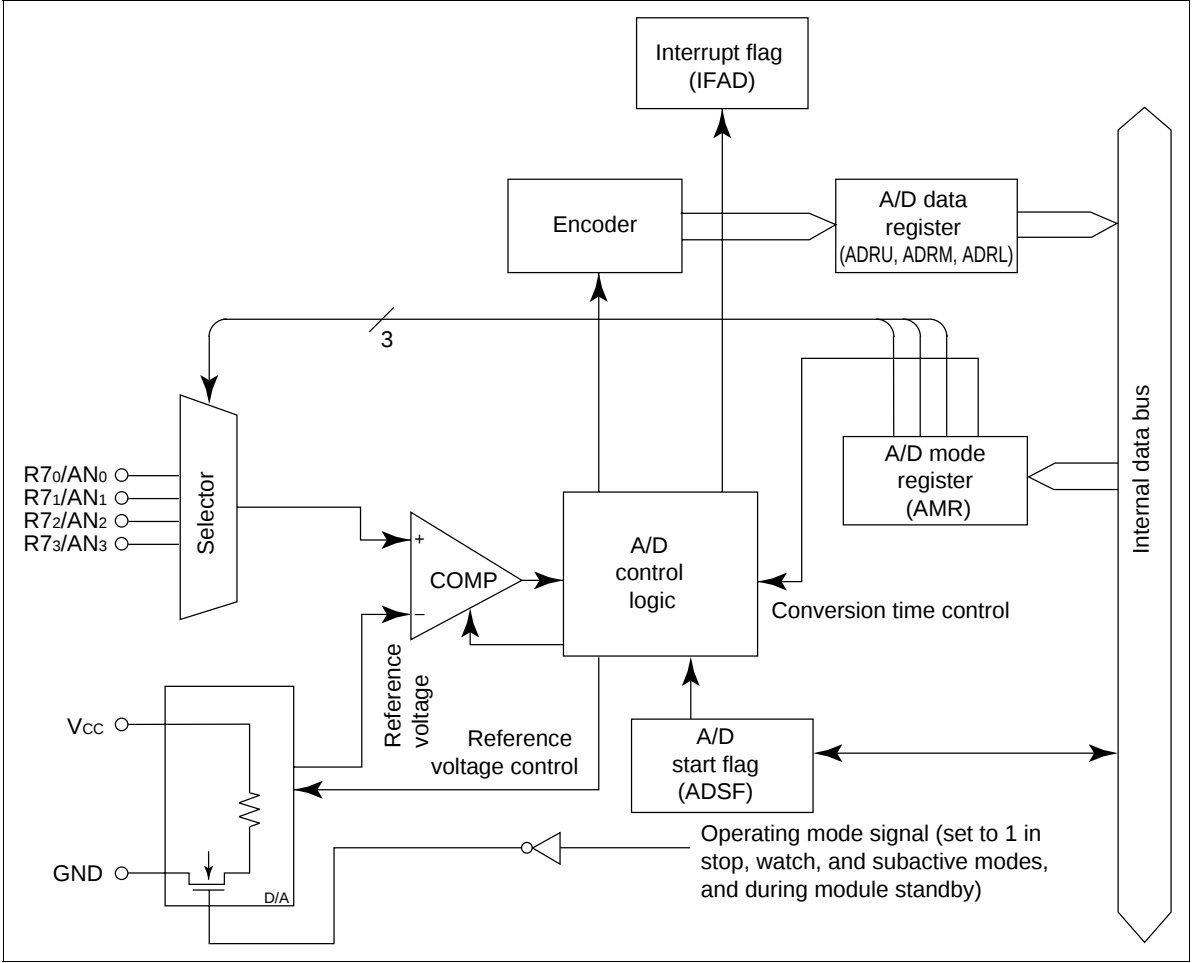


Figure 79-2 A/D Converter Block Diagram (HD404868 Series)

A/D mode register (AMR: \$028):

The A/D mode register is a 4-bit write-only register that shows the A/D converter speed setting and information on the analog input pin specification. The A/D conversion time is selected by bit 0, and the channel by bits 1, 2, and 3 (figure 80).

A/D start flag (ADSF: \$020,2):

A/D conversion is started by writing 1 to the A/D start flag. When conversion ends, the converted data is placed in the A/D data register and the A/D start flag is cleared at the same time. (figure 81).

A/D mode register (AMR: \$028)

| Bit                    | 3    | 2    | 1    | 0    |
|------------------------|------|------|------|------|
| Read/Write             | W    | W    | W    | W    |
| Initial value on reset | 0    | 0    | 0    | 0    |
| Bit name               | AMR3 | AMR2 | AMR1 | AMR0 |

↑

↑

↑

↑

| AMR0 | A/D conversion time  |
|------|----------------------|
| 0    | 65 t <sub>cyc</sub>  |
| 1    | 125 t <sub>cyc</sub> |

| AMR3 | AMR2 | AMR1 | Analog input channel selection |
|------|------|------|--------------------------------|
| 0    | 0    | *    | No selection                   |
|      | 1    | 0    | AN0                            |
|      |      | 1    | AN1                            |
| 1    | 0    | 0    | AN2                            |
|      |      | 1    | AN3                            |
|      | 1    | 0    | AN4*                           |
|      |      | 1    | AN5*                           |
|      |      |      |                                |

Note: \* Applies to HD404899 Series.

Figure 80 A/D Mode Register (AMR)

A/D start flag (ADSF: \$020,2)

| Bit                    | 3    | 2    | 1    | 0    |
|------------------------|------|------|------|------|
| Read/Write             | R/W  | R/W  | R/W  | R/W  |
| Initial value on reset | 0    | 0    | 0    | 0    |
| Bit name               | DTON | ADSF | WDON | LSON |

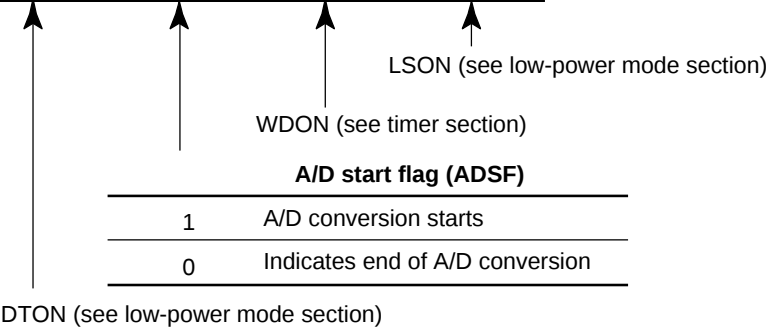


Figure 81 A/D Start Flag (ADSF)

**A/D data register (ADRL: \$029, ADRM: \$02A, ADRU: \$02B):**

The A/D data register is a read-only register consisting of a middle and upper 4 bits. This register is not cleared by a reset. Also, data read during A/D conversion is not guaranteed. At the end of A/D conversion, the resulting 10-bit data is stored in this register, and is held until the next conversion operation starts (figures 82, 83, 84 and 85).

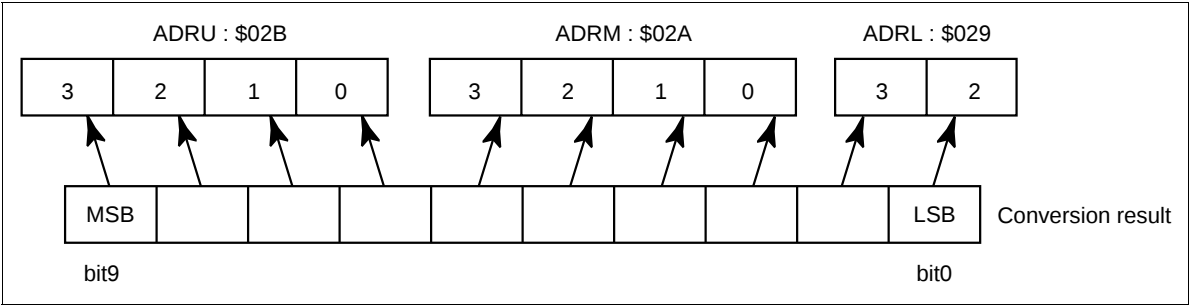


Figure 82 A/D Data Register

A/D data register-lower (ADRL: \$029)

| Bit                    | 3     | 2     | 1        | 0        |
|------------------------|-------|-------|----------|----------|
| Read/Write             | R     | R     | —        | —        |
| Initial value on reset | 1     | 1     | —        | —        |
| Bit name               | ADRL3 | ADRL2 | Not used | Not used |

Figure 83 A/D Data Register-Lower (ADRL)

A/D data register-middle (ADRM: \$02A)

| Bit                    | 3     | 2     | 1     | 0     |
|------------------------|-------|-------|-------|-------|
| Read/Write             | R     | R     | R     | R     |
| Initial value on reset | 1     | 1     | 1     | 1     |
| Bit name               | ADRM3 | ADRM2 | ADRM1 | ADRM0 |

Figure 84 A/D Data Register-Middle (ADRM)

A/D data register-upper (ADRU: \$02B)

| Bit                    | 3     | 2     | 1     | 0     |
|------------------------|-------|-------|-------|-------|
| Read/Write             | R     | R     | R     | R     |
| Initial value on reset | 0     | 1     | 1     | 1     |
| Bit name               | ADRU3 | ADRU2 | ADRU1 | ADRU0 |

Figure 85 A/D Data Register-Upper (ADRU)

**Module standby register 2 (MSR2: \$00E):**

Writing 1 to bit 1 of module standby register 2 stops the supply of the system clock to the A/D module and cuts the current ( $I_{AD}$ ) flowing in the ladder resistor.

**Usage notes:**

- Use the SEM or SEMD instruction to write to the A/D start flag (ADSF).
- Do not write to the ADSF during A/D conversion.
- Data in the A/D data register is undetermined during A/D conversion.

- As the A/D converter operates on a clock from OSC, it stops in stop mode, watch mode, and subactive mode. The current flowing in the A/D converter ladder resistor is also cut in these low-power modes to reduce power consumption.
- When an analog input pin is selected by the A/D mode register, the pull-up MOS for that pin is disabled.

## **LCD Circuit**

The MCU incorporates a controller and driver that drive four common signal pins and 32 segment pins (24 segment pins in the HD404868 Series). The controller unit consists of a RAM unit that stores the display data, a display control register (LCR), and a duty/clock control register (LMR) (figures 86-1 and 86-2).

The LCD circuit allows four different duties and LCD clocks to be controlled by the program, and also incorporates dual-port RAM, enabling display data to be transferred to the segment signal pins automatically without program processing. If the 32 kHz oscillator clock is designated as the LCD clock source, LCD display is also possible in watch mode in which the system clock stops.

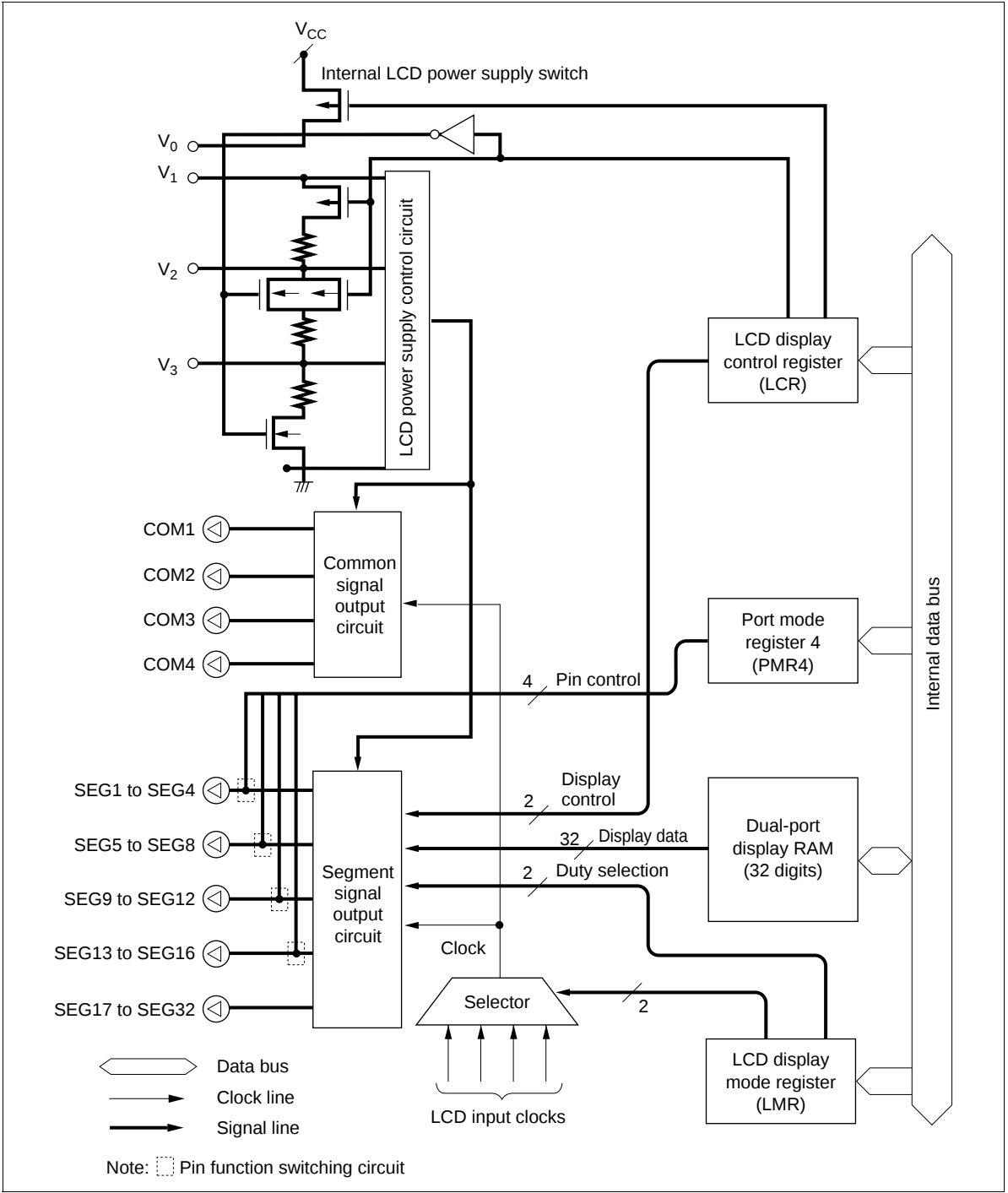
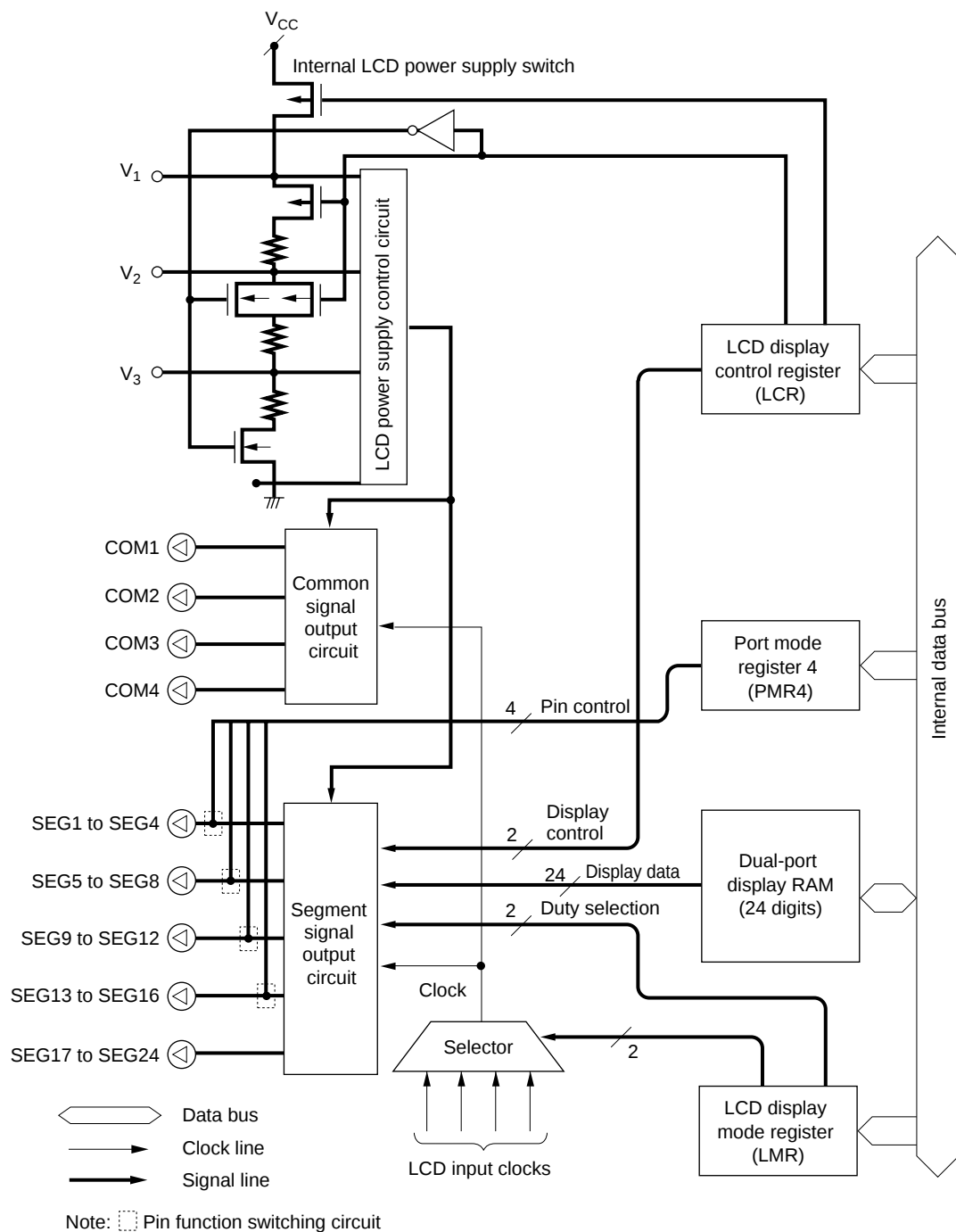


Figure 86-1 LCD Circuit Block Diagram (HD404889/HD404899/HD404878 Series)



### Figure 86-2 LCD Circuit Block Diagram (HD404868 Series)

## LCD data area and segment data: \$050 to \$06F (HD404889/HD404899/HD404878 Series) \$050 to \$067 (HD404868 Series)

Figures 87-1 and 87-2 show the LCD RAM area configuration. Each bit of the storage area corresponds to one of four duties. When data is written to the area corresponding to a particular duty, it is automatically output to the segment as display data.

|       | bit3  | bit2  | bit1  | bit0  |       | bit3  | bit2  | bit1  | bit0  |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$050 | SEG1  | SEG1  | SEG1  | SEG1  | \$060 | SEG17 | SEG17 | SEG17 | SEG17 |
| \$051 | SEG2  | SEG2  | SEG2  | SEG2  | \$061 | SEG18 | SEG18 | SEG18 | SEG18 |
| \$052 | SEG3  | SEG3  | SEG3  | SEG3  | \$062 | SEG19 | SEG19 | SEG19 | SEG19 |
| \$053 | SEG4  | SEG4  | SEG4  | SEG4  | \$063 | SEG20 | SEG20 | SEG20 | SEG20 |
| \$054 | SEG5  | SEG5  | SEG5  | SEG5  | \$064 | SEG21 | SEG21 | SEG21 | SEG21 |
| \$055 | SEG6  | SEG6  | SEG6  | SEG6  | \$065 | SEG22 | SEG22 | SEG22 | SEG22 |
| \$056 | SEG7  | SEG7  | SEG7  | SEG7  | \$066 | SEG23 | SEG23 | SEG23 | SEG23 |
| \$057 | SEG8  | SEG8  | SEG8  | SEG8  | \$067 | SEG24 | SEG24 | SEG24 | SEG24 |
| \$058 | SEG9  | SEG9  | SEG9  | SEG9  | \$068 | SEG25 | SEG25 | SEG25 | SEG25 |
| \$059 | SEG10 | SEG10 | SEG10 | SEG10 | \$069 | SEG26 | SEG26 | SEG26 | SEG26 |
| \$05A | SEG11 | SEG11 | SEG11 | SEG11 | \$06A | SEG27 | SEG27 | SEG27 | SEG27 |
| \$05B | SEG12 | SEG12 | SEG12 | SEG12 | \$06B | SEG28 | SEG28 | SEG28 | SEG28 |
| \$05C | SEG13 | SEG13 | SEG13 | SEG13 | \$06C | SEG29 | SEG29 | SEG29 | SEG29 |
| \$05D | SEG14 | SEG14 | SEG14 | SEG14 | \$06D | SEG30 | SEG30 | SEG30 | SEG30 |
| \$05E | SEG15 | SEG15 | SEG15 | SEG15 | \$06E | SEG31 | SEG31 | SEG31 | SEG31 |
| \$05F | SEG16 | SEG16 | SEG16 | SEG16 | \$06F | SEG32 | SEG32 | SEG32 | SEG32 |
|       | COM4  | COM3  | COM2  | COM1  |       | COM4  | COM3  | COM2  | COM1  |

**Figure 87-1 LCD RAM Area Configuration (Using Dual-Port RAM)  
(HD404889/HD404899/HD404878 Series)**

|       | bit3  | bit2  | bit1  | bit0  |       | bit3  | bit2  | bit1  | bit0  |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$050 | SEG1  | SEG1  | SEG1  | SEG1  | \$060 | SEG17 | SEG17 | SEG17 | SEG17 |
| \$051 | SEG2  | SEG2  | SEG2  | SEG2  | \$061 | SEG18 | SEG18 | SEG18 | SEG18 |
| \$052 | SEG3  | SEG3  | SEG3  | SEG3  | \$062 | SEG19 | SEG19 | SEG19 | SEG19 |
| \$053 | SEG4  | SEG4  | SEG4  | SEG4  | \$063 | SEG20 | SEG20 | SEG20 | SEG20 |
| \$054 | SEG5  | SEG5  | SEG5  | SEG5  | \$064 | SEG21 | SEG21 | SEG21 | SEG21 |
| \$055 | SEG6  | SEG6  | SEG6  | SEG6  | \$065 | SEG22 | SEG22 | SEG22 | SEG22 |
| \$056 | SEG7  | SEG7  | SEG7  | SEG7  | \$066 | SEG23 | SEG23 | SEG23 | SEG23 |
| \$057 | SEG8  | SEG8  | SEG8  | SEG8  | \$067 | SEG24 | SEG24 | SEG24 | SEG24 |
| \$058 | SEG9  | SEG9  | SEG9  | SEG9  |       |       |       |       |       |
| \$059 | SEG10 | SEG10 | SEG10 | SEG10 |       |       |       |       |       |
| \$05A | SEG11 | SEG11 | SEG11 | SEG11 |       |       |       |       |       |
| \$05B | SEG12 | SEG12 | SEG12 | SEG12 |       |       |       |       |       |
| \$05C | SEG13 | SEG13 | SEG13 | SEG13 |       |       |       |       |       |
| \$05D | SEG14 | SEG14 | SEG14 | SEG14 |       |       |       |       |       |
| \$05E | SEG15 | SEG15 | SEG15 | SEG15 |       |       |       |       |       |
| \$05F | SEG16 | SEG16 | SEG16 | SEG16 |       |       |       |       |       |
|       | COM4  | COM3  | COM2  | COM1  |       |       |       |       |       |

**Figure 87-2 LCD RAM Area Configuration (Using Dual-Port RAM) (HD404868 Series)**

**LCD control register (LCR: \$02C):**

The LCD control register is a 4-bit write-only register that controls LCD blanking, the on/off state of the LCD power switch, display in watch mode and subactive mode, and disconnection of the LCD power supply dividing resistor, as shown in figure 88.

Individual bit in this register can be set and reset by bit manipulation instructions.

- Display on/off control
  - Off: Segment signals are in the off state, regardless of LCD RAM data.
  - On: LCD RAM data is output as segment signals.
- Built-in power switch on/off control
  - Off: The built-in LCD power switch is off.
  - On: The built-in LCD power switch is on. If V0 and V1 are shorted externally, V1 goes to the  $V_{CC}$  level.
- LCD display in watch mode and subactive mode
  - Off: In watch mode and subactive mode, all common and segment pins are fixed at GND potential. The built-in LCD power switch is off.
  - On: In watch mode and subactive mode, LCD RAM data is output as segment signals.
- LCD power supply dividing resistor switch on/off control
  - Off: The built-in LCD power supply dividing resistor is disconnected.
  - On: The built-in LCD power supply dividing resistor is connected.

LCD control register (LCR: \$02C)

| Bit                    | 3    | 2    | 1    | 0    |
|------------------------|------|------|------|------|
| Read/Write             | W    | W    | W    | W    |
| Initial value on reset | 0    | 0    | 0    | 0    |
| Bit name               | LCR3 | LCR2 | LCR1 | LCR0 |

↑

LCR0

LCD on/off control

|   |     |
|---|-----|
| 0 | Off |
| 1 | On  |

↑

LCR1

Built-in LCD power switch on/off control

|   |     |
|---|-----|
| 0 | Off |
| 1 | On  |

↑

LCR2

Watch mode/subactive mode LCD display

|   |     |
|---|-----|
| 0 | Off |
| 1 | On  |

↑

LCR3

LCD power supply dividing resistor

|   |     |
|---|-----|
| 0 | On  |
| 1 | Off |

Figure 88 LCD Control Register (LCR)

LCD duty/clock control register (LMR: \$02D):

The LCD duty/clock control register is a 4-bit write-only register used to set four kinds of display duty ratio and LCD reference clock (figure 89). Table 27 shows the LCD frame frequencies for each duty setting.

LCD duty/clock control register (LMR: \$02D)

| Bit                    | 3    | 2    | 1    | 0    |
|------------------------|------|------|------|------|
| Read/Write             | W    | W    | W    | W    |
| Initial value on reset | 0    | 0    | 0    | 0    |
| Bit name               | LMR3 | LMR2 | LMR1 | LMR0 |

↑

↑

↑

↑

| LMR1 | LMR0 | Duty factor      |
|------|------|------------------|
| 0    | 0    | 1/4              |
|      | 1    | 1/3              |
| 1    | 0    | 1/2              |
|      | 1    | 1 (static drive) |

| LMR3 | LMR2 | LCD circuit clock                                                                                                                           |
|------|------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 0    | 0    | $CL0=32.768\text{kHz} \times \text{Duty}/128$                                                                                               |
|      | 1    | $CL1=32.768\text{kHz} \times \text{Duty}/256$                                                                                               |
| 1    | 0    | $CL2=\varnothing_{\text{PER}} \times \text{Duty}/256$                                                                                       |
|      | 1    | When TMA3 = 0, $CL3 = \varnothing_{\text{PER}} \times \text{Duty}/2048$<br>When TMA3 = 1, $CL3 = 32.768 \text{ kHz} \times \text{Duty}/512$ |

Figure 89 LCD Duty/Clock Control Register (LMR)

**Table 27 LCD Frame Frequencies for Each Duty Setting**

| Duty   | LMR3 | LMR2 |      | Frame Period     |                   |                  |                   |                  |                   |                  |                   |
|--------|------|------|------|------------------|-------------------|------------------|-------------------|------------------|-------------------|------------------|-------------------|
|        |      |      |      | fosc=400kHz      |                   | fosc=800kHz      |                   | fosc=2.0MHz      |                   | fosc=4.0MHz      |                   |
|        |      |      |      | Division<br>by 4 | Division<br>by 32 | Division<br>by 4 | Division<br>by 32 | Division<br>by 4 | Division<br>by 32 | Division<br>by 4 | Division<br>by 32 |
| Static | 0    | 0    | CL0  | 256Hz            |                   |                  |                   |                  |                   |                  |                   |
|        |      | 1    | CL1  | 128Hz            |                   |                  |                   |                  |                   |                  |                   |
|        | 1    | 0    | CL2  | 390.6Hz          | 48.8Hz            | 781.3Hz          | 97.7Hz            | 1953Hz           | 244.1Hz           | 3906Hz           | 488.3Hz           |
|        |      | 1    | CL3* | 48.8Hz           | 6.1Hz             | 97.7Hz           | 12.2Hz            | 244.1Hz          | 30.5Hz            | 488.3Hz          | 61.0Hz            |
| 1/2    | 0    | 0    | CL0  | 128Hz            |                   |                  |                   |                  |                   |                  |                   |
|        |      | 1    | CL1  | 64Hz             |                   |                  |                   |                  |                   |                  |                   |
|        | 1    | 0    | CL2  | 195.3Hz          | 24.4Hz            | 390.6Hz          | 48.8Hz            | 976.6Hz          | 122.1Hz           | 1953Hz           | 244.1Hz           |
|        |      | 1    | CL3* | 24.4Hz           | 3.1Hz             | 48.8Hz           | 6.1Hz             | 122.1Hz          | 15.3Hz            | 244.1Hz          | 30.5Hz            |
| 1/3    | 0    | 0    | CL0  | 85.3Hz           |                   |                  |                   |                  |                   |                  |                   |
|        |      | 1    | CL1  | 42.7Hz           |                   |                  |                   |                  |                   |                  |                   |
|        | 1    | 0    | CL2  | 130.1Hz          | 16.3Hz            | 260.2Hz          | 32.5Hz            | 650Hz            | 81.3Hz            | 1301Hz           | 162.6Hz           |
|        |      | 1    | CL3* | 16.3Hz           | 2.0Hz             | 32.5Hz           | 4.1Hz             | 81.3Hz           | 10.2Hz            | 162.6Hz          | 20.3Hz            |
| 1/4    | 0    | 0    | CL0  | 64Hz             |                   |                  |                   |                  |                   |                  |                   |
|        |      | 1    | CL1  | 32Hz             |                   |                  |                   |                  |                   |                  |                   |
|        | 1    | 0    | CL2  | 97.7Hz           | 12.2Hz            | 195.3Hz          | 24.4Hz            | 488.3Hz          | 61.0Hz            | 976.6Hz          | 122.1Hz           |
|        |      | 1    | CL3* | 12.2Hz           | 1.5Hz             | 24.4Hz           | 3.1Hz             | 61.0Hz           | 7.6Hz             | 122.1Hz          | 15.3Hz            |

Port mode register 4 (PMR4: \$00C):

Port mode register 4 (PMR4) is a 4-bit write-only register that enables the R3 to R6 port pins to be switched to SEG1 to SEG16 pin functions in 4-port units (figure 90).

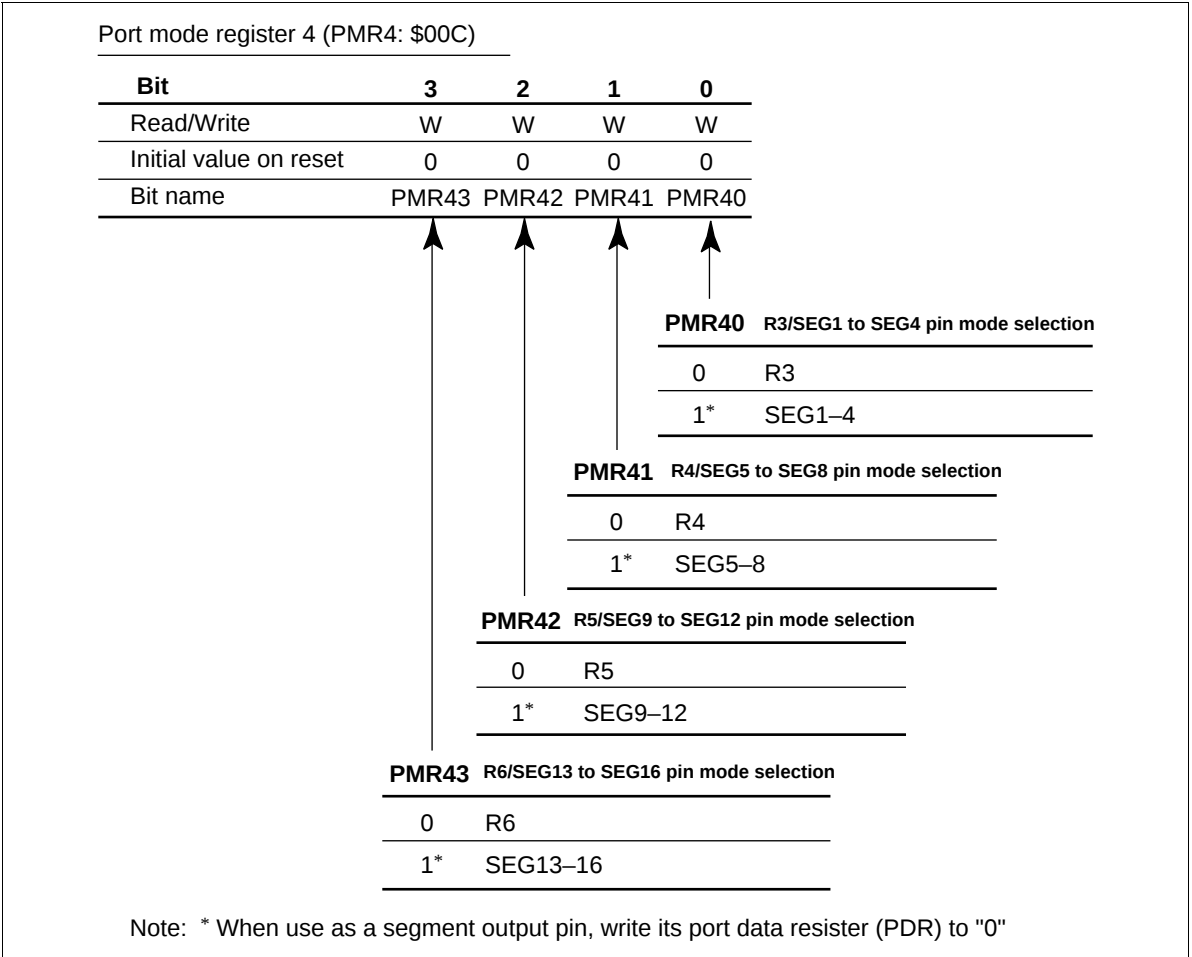


Figure 90 Port Mode Register 4 (PMR4: \$00C)

LCD drive voltage ( $V_{LCD}$ ):

Example of LCD drive power supply wiring are shown in figures 91-1 and 91-2. The LCD drive voltage ( $V_{LCD}$ ) should be within the following range.

$$2.2 \leq V_{LCD} \leq V_{CC} \text{ (V)}$$

If the LCD drive voltage is applied from off-chip, connect the V0 pin to  $V_{CC}$  and turn the LCD power switch (LCD control register) off. (HD404889/HD404899/HD404878 Series)

When the power supply voltage is used as the LCD drive voltage, the V0 and V1 pins should be shorted. (HD404889/HD404899/HD404878 Series)

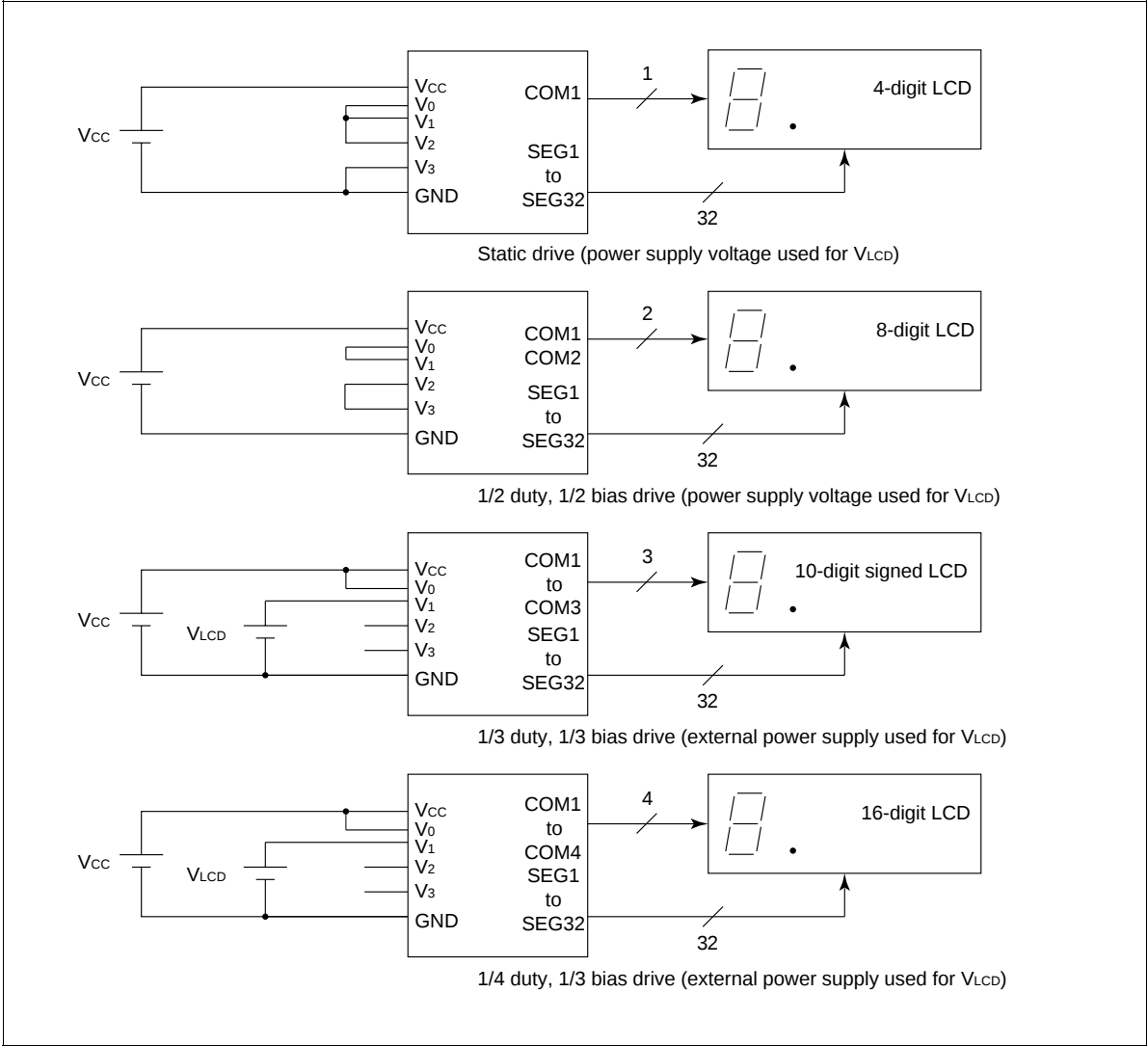


Figure 91-1 Examples of LCD Wiring (HD404889/HD404899/HD404878 Series)

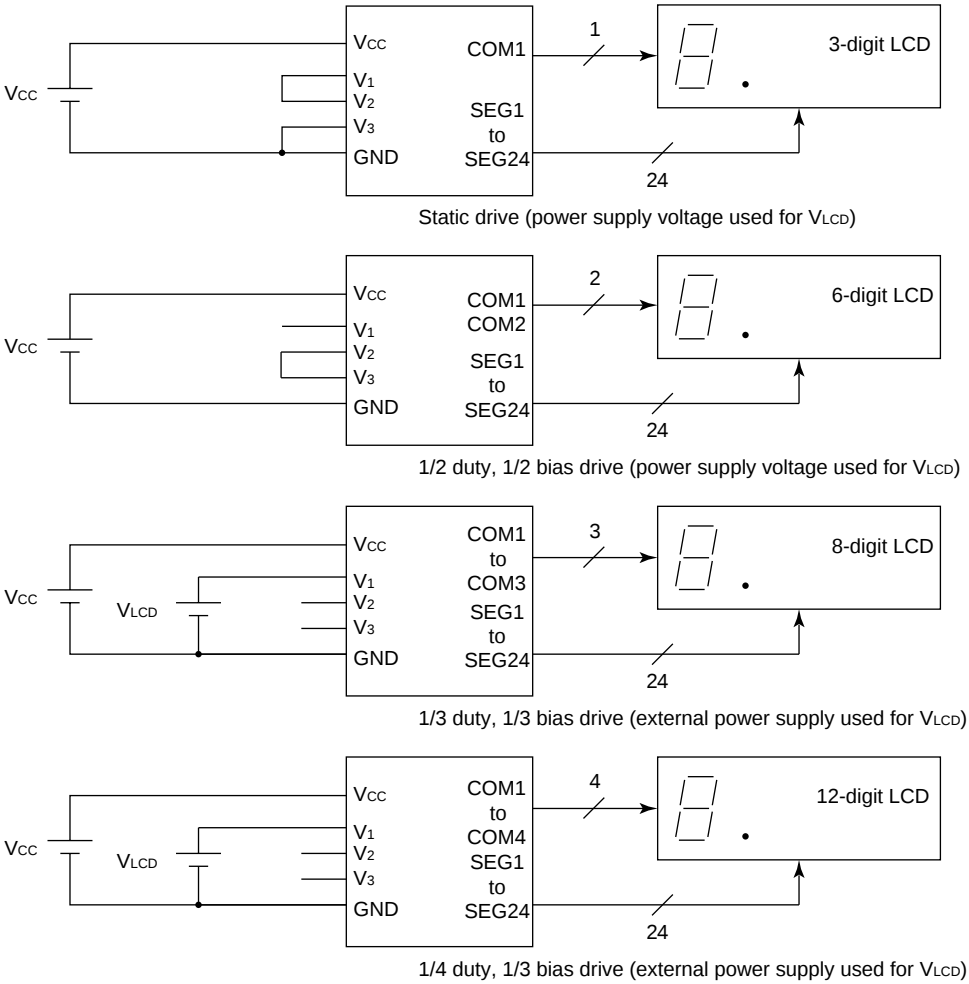


Figure 91-2 Examples of LCD Wiring (HD404868 Series)

**Large LCD panel drive:**

If the capacitance of the driven LCD is large, the value of the divided resistance should be reduced by dividing the resistance in parallel with the built-in divided resistor (see figures 92-1 and 92-2).

As an LCD has a matrix structure, the path of the charge/discharge current flowing to the load capacitance is complicated. Moreover, the current varies depending on the illumination state, so that it is not possible to determine the resistance values simply from the LCD load capacitance. The resistance values must therefore be determined experimentally in accordance with the power consumption requirement of the equipment, including the LCD. (Adding capacitors C with a value of 0.1 to 0.3  $\mu\text{F}$  is also effective).

A value of 1 k $\Omega$  to 10 k $\Omega$  is normally set for R.

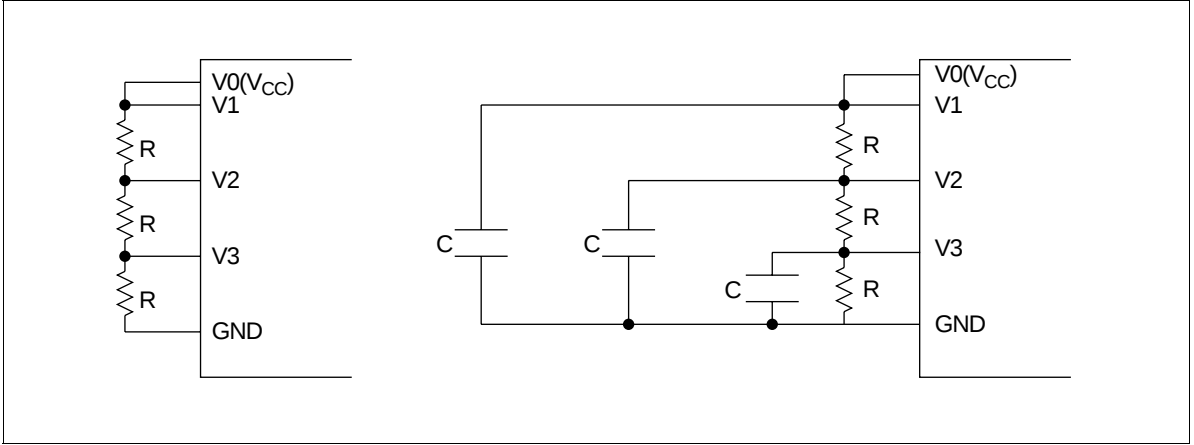


Figure 92-1 Large LCD Panel Drive (Using Power Supply Voltage for V<sub>LCD</sub>)  
(HD404889/HD404899/HD404878 Series)

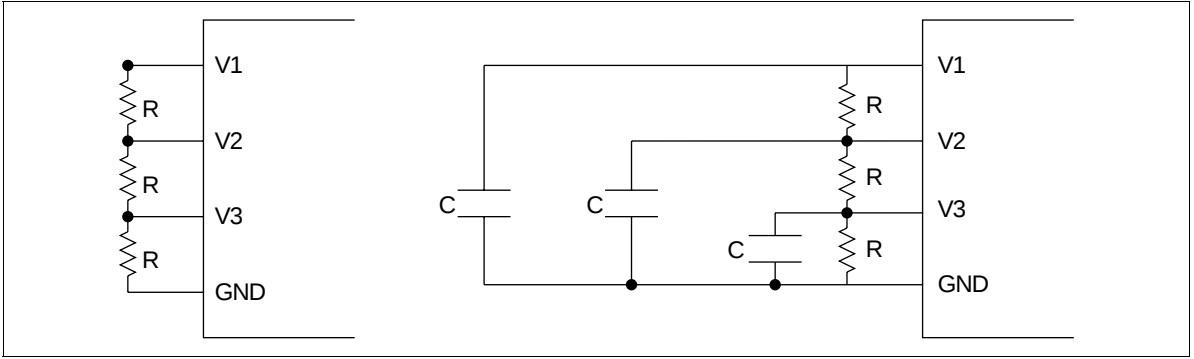


Figure 92-2 Large LCD Panel Drive (Using Power Supply Voltage for V<sub>LCD</sub>) (HD404868 Series)

Usage Notes

When R3<sub>0</sub>/SEG1 to R6<sub>0</sub>/SEG16 pins are used as segment output pins, write their port data register (PDR) to “0”.

## Buzzer Output Circuit

**Buzzer Output Circuit Functions:** The buzzer output circuit has the following functions.

- Timer overflow toggle output
- System clock divided clock pulse output

The block diagram of the buzzer output circuit is shown in figure 93.

### Buzzer Output Circuit Operation

- Timer overflow toggle output operation

The timer overflow toggle output operation setting is made by bits 1 and 2 of the buzzer mode register (BMR) and bit 2 of port mode register 2 (PMR2). By clearing bit 2 of the buzzer mode register (BMR) to 0, selecting timer B or timer C overflow by bit 1, and setting bit 2 of port mode register 2 (PMR2) to 1, a toggle waveform is output from the BUZZ pin with overflow as the trigger.

- System clock divided clock pulse output

The system clock divided clock pulse output operation setting is made by bits 0 to 3 of the buzzer mode register (BMR) and bit 2 of port mode register 2 (PMR2). Bit 2 of the buzzer mode register (BMR) is set to 1, the system clock division ratio is selected by bits 0 and 1, and bit 2 of port mode register 2 (PMR2) is set to 1. Clock pulses are output by setting bit 3 of the buzzer mode register (BMR) to 1. If bit 3 of the buzzer mode register (BMR) is cleared to 0, the BUZZ pin goes low.

The clock pulse width is fixed without regard to the timing set by bit 3 of the buzzer mode register (BMR), and careful coordination with software is necessary with regard to the number of output pulses. After a clock pulse modification is made, clock pulses should not be output until 4tcyc after the modifying instruction.

Only a bit manipulation instruction can be used on bit 3 of the buzzer mode register (BMR).

### Buzzer Output Circuit Registers

Buzzer output circuit operation setting is performed by the following registers.

Buzzer mode register (BMR: \$02E)

Port mode register 2 (PMR2: \$00A)

#### **Buzzer mode register (BMR: \$02E):**

The buzzer mode register (BMR) is a 4-bit write-only register used to set toggle output by timer overflow and system clock divided clock pulse output as shown in figure 94.

Bit 3 of the buzzer mode register (BMR) can only be accessed by a bit manipulation instruction.

The buzzer mode register (BMR) is reset to \$0 by an MCU reset.

Port mode register 2 (PMR2: \$00A):

Port mode register 2 (PMR2) is a 4-bit write-only register used to switch the R1<sub>2</sub>/BUZZ pin function as shown in figure 30.

Port mode register 2 (PMR2) is reset to \$0 by an MCU reset.

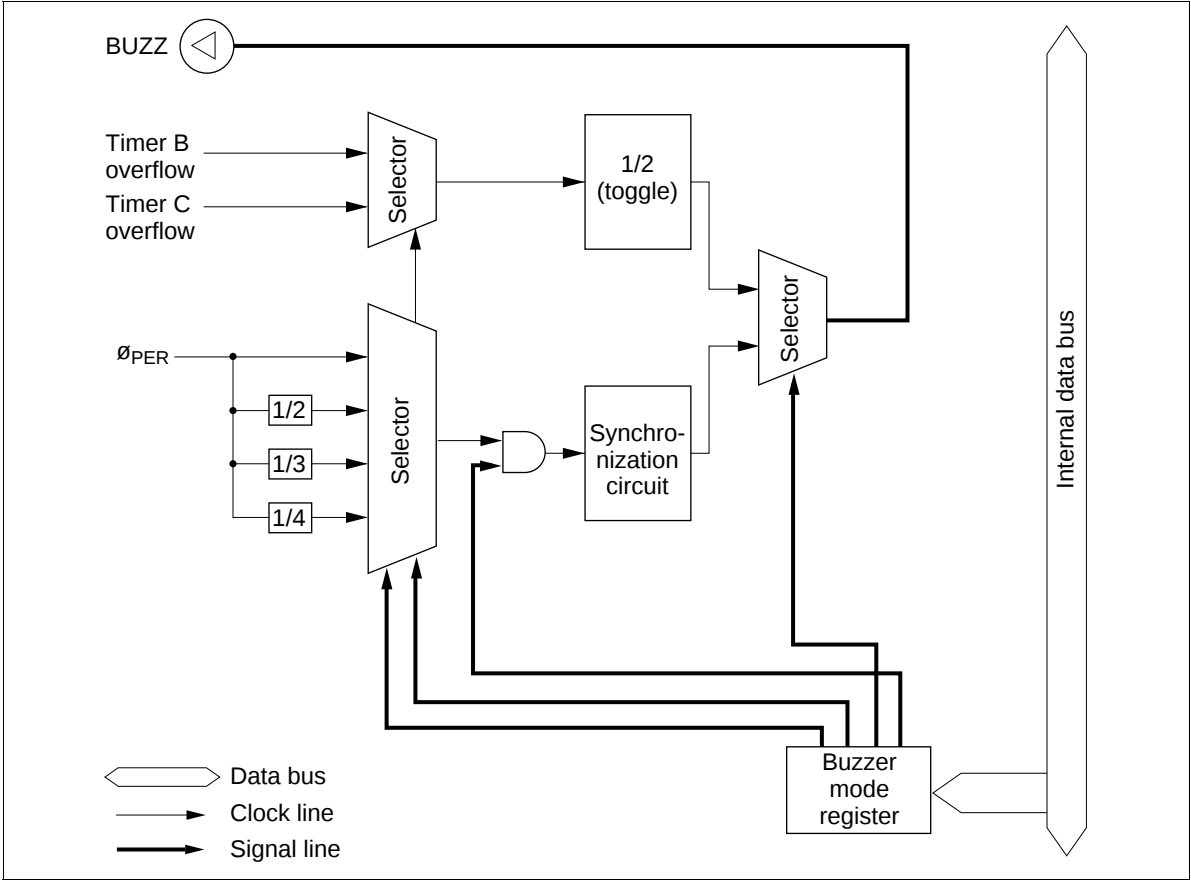


Figure 93 Buzzer Output Circuit

Buzzer mode register (BMR: \$02E)

| Bit                    | 3    | 2    | 1    | 0    |
|------------------------|------|------|------|------|
| Read/Write             | W    | W    | W    | W    |
| Initial value on reset | 0    | 0    | 0    | 0    |
| Bit name               | BMR3 | BMR2 | BMR1 | BMR0 |

|   | BMR2 | BMR1 | BMR0 | BUZZ pin output                   |
|---|------|------|------|-----------------------------------|
| 0 | 0    | 0    | *    | Division by 2 of timer B overflow |
|   |      | 1    | *    | Division by 2 of timer C overflow |
| 1 | 0    | 0    | 0    | øPER clock                        |
|   |      |      | 1    | øPER/2clock                       |
|   | 1    | 0    | 0    | øPER/3clock                       |
|   |      |      | 1    | øPER/4clock                       |

\* : Don't care

Clock output control (enabled when BMR2 = 1, bit manipulation instruction)

|   |                     |
|---|---------------------|
| 0 | Stopped (low level) |
| 1 | Output              |

Figure 94 Buzzer Mode Register (BMR)

## **ZTAT<sup>TM</sup> Microcomputer with Built-in Programmable ROM**

### **1. Precautions for use of ZTAT<sup>TM</sup> microcomputer with built-in programmable ROM**

#### **(1) Precautions for writing to programmable ROM built in ZTAT<sup>TM</sup> microcomputer**

In the ZTAT<sup>TM</sup> microcomputer with built-in plastic mold one-time programmable ROM, incomplete electrical connection between the PROM writer and socket adapter causes writing errors and, makes the computer unoperatable. To enhance the writing efficiency, attention should be paid to the following points:

- (a) Make sure that the socket adapter is firmly fixed to the PROM writer and connected electrically with each other (neither opened nor shorted), before starting the writing process.
- (b) To secure the electrical connection between the contact pin and IC lead, make sure that there is no foreign substance on the contact pin of the socket adapter, which may cause improper electrical connection.
- (c) When inserting the IC, be careful to protect the IC lead from bending in order to secure the electrical connection between the contact pin and IC lead. If the lead is bent, correct the bending and insert it again.
- (d) If any trouble is noticed during a blank check to be performed to prevent erroneous writing due to improper electrical connection, carry out the writing process again according to above steps (a), (b), and (c).
- (e) During the writing process, do not touch the socket adapter and IC to prevent erroneous writing.
- (f) To write continuously in the IC, follow steps (a), (b), (c), (d) and (e).
- (g) If a writing error recurs, or the rate of writing errors occur frequently, stop writing and check the PROM writer, socket adapter, etc. for defects.
- (h) If any problem is noticed in the written program or in the program after being left at a high temperature, consult our technical staff.

#### **(2) Precautions when new PROM writer, socket adapter or IC is used**

When a new PROM writer, socket adapter or IC is employed, breakdown of the IC may occur or its writing may become impossible because the noise, overshoot, timing or other electrical characteristics may be inconsistent with the assured IC writing characteristics. To avoid such troubles, check the following points before starting the writing process.

- (a) To ensure stable writing operation, check that the  $V_{CC}$  of the power supplied to the PROM writer, power source current capacity of  $V_{PP}$ , and current consumption at the time of writing to IC are provided with sufficient margin.
- (b) To prevent breakdown of the IC, check that the power source voltage between GND- $V_{CC}$  and GND- $V_{PP}$ , and overshoot or undershoot of the power source at the connecting terminal of the socket adapter are within the ratings. Particularly, if the overshoot or undershoot exceeds the maximum rating, the p-n connection may be damaged, leading to permanent breakdown. If overshoot or undershoot occurs, recheck the power source damping resistance of capacity.
- (c) To prevent breakdown of the IC and for stable writing and reading operation, insert the IC into the socket adapter and check the power noise between the GND- $V_{CC}$  and GND- $V_{PP}$  near the IC connecting

terminal. If power source noise is noticed, insert an appropriate capacitor between the GND power sources depending on the noise generated. In case of high frequency noise, insert a capacitor of low inductance.

- (d) For stable writing and reading operation, insert the IC into the socket adapter and check the input waveform, timing and noise near the R/W, CS, address and data terminals. Particularly, since recent ICs have increased in speed, caution should be exercised against the noise to the power source or address due to crosstalk from the output data terminal. To avoid these problems, inserting a low inductance capacitor between the GND and power source or inserting a damping resistance to the output data terminal is effective.
- (e) Particularly, when a multiple PROM writer is used, perform above items (a), (b), (c), and (d) assuming all ICs inserted into the socket adapter.
- (f) In the case of a multiple PROM writer, when an unacceptable result is noticed during a blank check performed to prevent erroneous writing due to improper electrical connection of the power source, etc., rewriting is impossible unless every writing process can be stopped. Therefore, the potential increases due to erroneous writing because of improper connection. Be sure to check the electrical connection between the PROM writer and socket adapter and IC.
- (g) If any abnormality is noticed while checking a written program, consult our technical staff.

## **2. Programming of Built-in programmable ROM**

The MCU can stop its function as an MCU in PROM mode for programming the built-in PROM.

PROM mode is set by driving the  $\overline{\text{RESET}}$ ,  $\overline{\text{M}}_0$ , and  $\overline{\text{M}}_1$  pins low (or by driving the  $\overline{\text{RESET}}$  and  $\overline{\text{M}}_0$  pins low in the HD4074869), and driving the TEST pin to the  $V_{pp}$  level.

Writing and reading specifications of the PROM are the same as those for the commercial EPROM27256. Using a socket adapter for specific use of each product, programming is possible with a general-purpose PROM writer.

Since an instruction of the HMCS400 series is 10 bits long, a conversion circuit is incorporated to adapt the general-purpose PROM writer. This circuit splits each instruction into five lower bits and five higher bits to write from or read to two addresses. This enables use of a general-purpose PROM. For instance, to write to a 16kword of built-in PROM writer with a general-purpose PROM, specify 32kbyte address (\$0000-\$7FFF). An example of PROM memory map is shown in figure 95.

### **Notes:**

1. When programming with a PROM writer, set up each ROM size to the address given in table 30. If it is programmed erroneously to an address given in table 30 or later, check of writing of PROM may become impossible. Particularly, caution should be exercised in the case of a plastic package since reprogramming is impossible with it. Set the data in unused addresses to \$FF.
2. If the indexes of the PROM writer socket, socket adapter and product are not aligned precisely, the product may break down due to overcurrent. Be sure to check that they are properly set to the writer before starting the writing process.

- Two levels of program voltages ( $V_{PP}$ ) are available for the PROM: 12.5V and 21V. Our product employs a  $V_{PP}$  of 12.5V. If a voltage of 21V is applied, permanent breakdown of the product will result. The  $V_{PP}$  of 12.5V is obtained for the PROM writer by setting it according to the Intel 27258 specifications.

**Table 28     Socket Adapters**

| Package | Model Name                          | Manufacturer |
|---------|-------------------------------------|--------------|
| FP-80A  | Please ask Hitachi service section. |              |
| TFP-80C | Please ask Hitachi service section. |              |
| FP-64A  | Please ask Hitachi service section. |              |
| DP-64S  | Please ask Hitachi service section. |              |

## Writing/verification

Programming of the built-in program ROM employs a high speed programming method. With this method, high speed writing is effected without voltage stress to the device or without damaging the reliability of the written data.

A basic programming flow chart is shown in figure 96 and a timing chart in figure 97.

For precautions for PROM writing procedure, refer to Section 2, "Characteristics of ZTAT™ Microcomputer's Built-in Programmable ROM and precautions for its Applications."

**Table 29     Selection of Mode**

| Mode                       | CE     | OE     | $V_{PP}$ | $O_0$ to $O_4$ |
|----------------------------|--------|--------|----------|----------------|
| Writing                    | "Low"  | "High" | $V_{PP}$ | Data input     |
| Verification               | "High" | "Low"  | $V_{PP}$ | Data output    |
| Prohibition of programming | "High" | "High" | $V_{PP}$ | High impedance |

**Table 30     PROM Writer Program Address**

| ROM size | Address       |
|----------|---------------|
| 8k       | \$0000~\$3FFF |
| 12k      | \$0000~\$5FFF |
| 16k      | \$0000~\$7FFF |

# HD404889/HD404899/HD404878/HD404868 Series

## Programmable Rom (HD4074889, HD4074899, HD4074869)

The HD4074889, HD4074899, and HD4074869 are a ZTAT™ microcomputers with built-in PROM that can be programmed in PROM mode.

### PROM Mode Pin Description

HD4074889, HD4074899

| Pin No. | MCU Mode                        |     | PROM Mode       |     |
|---------|---------------------------------|-----|-----------------|-----|
| FP-80A  | Pin Name                        | I/O | Pin Name        | I/O |
| TFP-80C |                                 |     |                 |     |
| 1       | AV <sub>CC</sub>                | —   | V <sub>CC</sub> | —   |
| 2       | R7 <sub>/</sub> AN0             | I/O | V <sub>CC</sub> | —   |
| 3       | R7 <sub>/</sub> AN1             | I/O | V <sub>CC</sub> | —   |
| 4       | R7 <sub>/</sub> AN2             | I/O |                 |     |
| 5       | R7 <sub>/</sub> AN3             | I/O |                 |     |
| 6       | R8 <sub>/</sub> AN4             | I/O |                 |     |
| 7       | R8 <sub>/</sub> AN5             | I/O |                 |     |
| 8       | AV <sub>SS</sub>                | —   | GND             | —   |
| 9       | TEST                            | I   | V <sub>PP</sub> | —   |
| 10      | OSC1                            | I   | V <sub>CC</sub> | —   |
| 11      | OSC2                            | O   |                 |     |
| 12      | GND                             | —   | GND             | —   |
| 13      | X2                              | O   |                 |     |
| 14      | X1                              | I   | GND             | —   |
| 15      | RESET                           | I   | RESET           | I   |
| 16      | V <sub>CC</sub>                 | —   | V <sub>CC</sub> | —   |
| 17      | D <sub>/</sub> INT <sub>0</sub> | I/O | A <sub>n</sub>  | I   |
| 18      | D <sub>/</sub> INT <sub>1</sub> | I/O |                 |     |
| 19      | D <sub>2</sub>                  | I/O | A <sub>5</sub>  | I   |
| 20      | D <sub>3</sub>                  | I/O | A <sub>6</sub>  | I   |
| 21      | D <sub>4</sub>                  | I/O | A <sub>7</sub>  | I   |
| 22      | D <sub>5</sub>                  | I/O | A <sub>8</sub>  | I   |
| 23      | D <sub>6</sub>                  | I/O | A <sub>9</sub>  | I   |
| 24      | D <sub>7</sub>                  | I/O | A <sub>10</sub> | I   |
| 25      | D <sub>8</sub>                  | I/O | A <sub>11</sub> | I   |
| 26      | D <sub>9</sub>                  | I/O | A <sub>12</sub> | I   |
| 27      | D <sub>10</sub>                 | I/O | A <sub>13</sub> | I   |
| 28      | D <sub>11</sub>                 | I/O | A <sub>14</sub> | I   |
| 29      | R0 <sub>/</sub> WU <sub>0</sub> | I/O | V <sub>CC</sub> | —   |
| 30      | R0 <sub>/</sub> WU <sub>1</sub> | I/O |                 |     |
| 31      | R0 <sub>/</sub> WU <sub>2</sub> | I/O |                 |     |
| 32      | R0 <sub>/</sub> WU <sub>3</sub> | I/O |                 |     |
| 33      | R1 <sub>/</sub> EVNB            | I/O |                 |     |
| 34      | R1 <sub>/</sub> EVND            | I/O | M0              | I   |
| 35      | R1 <sub>/</sub> BUZZ            | I/O | M1              | I   |
| 36      | R1 <sub>/</sub> TOB             | I/O | CE              | I   |
| 37      | R2 <sub>/</sub> TOC             | I/O |                 |     |
| 38      | R2 <sub>/</sub> SCK             | I/O | OE              | I   |
| 39      | R2 <sub>/</sub> SI/SO           | I/O | XM0             | O   |
| 40      | R2 <sub>3</sub>                 | I/O | XM1             | O   |

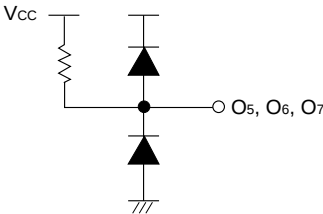
| Pin No. | MCU Mode              |     | PROM Mode       |     |
|---------|-----------------------|-----|-----------------|-----|
| FP-80A  | Pin Name              | I/O | Pin Name        | I/O |
| TFP-80C |                       |     |                 |     |
| 41      | R3 <sub>/</sub> SEG1  | I/O | A <sub>1</sub>  | I   |
| 42      | R3 <sub>/</sub> SEG2  | I/O | A <sub>2</sub>  | I   |
| 43      | R3 <sub>/</sub> SEG3  | I/O | A <sub>3</sub>  | I   |
| 44      | R3 <sub>/</sub> SEG4  | I/O | A <sub>4</sub>  | I   |
| 45      | R4 <sub>/</sub> SEG5  | I/O | O <sub>0</sub>  | I/O |
| 46      | R4 <sub>/</sub> SEG6  | I/O | O <sub>1</sub>  | I/O |
| 47      | R4 <sub>/</sub> SEG7  | I/O | O <sub>2</sub>  | I/O |
| 48      | R4 <sub>/</sub> SEG8  | I/O | O <sub>3</sub>  | I/O |
| 49      | R5 <sub>/</sub> SEG9  | I/O | O <sub>4</sub>  | I/O |
| 50      | R5 <sub>/</sub> SEG10 | I/O | O <sub>4</sub>  | I/O |
| 51      | R5 <sub>/</sub> SEG11 | I/O | O <sub>3</sub>  | I/O |
| 52      | R5 <sub>/</sub> SEG12 | I/O | O <sub>2</sub>  | I/O |
| 53      | R6 <sub>/</sub> SEG13 | I/O | O <sub>1</sub>  | I/O |
| 54      | R6 <sub>/</sub> SEG14 | I/O | O <sub>0</sub>  | I/O |
| 55      | R6 <sub>/</sub> SEG15 | I/O |                 |     |
| 56      | R6 <sub>/</sub> SEG16 | I/O |                 |     |
| 57      | SEG17                 | O   |                 |     |
| 58      | SEG18                 | O   |                 |     |
| 59      | SEG19                 | O   |                 |     |
| 60      | SEG20                 | O   |                 |     |
| 61      | SEG21                 | O   |                 |     |
| 62      | SEG22                 | O   |                 |     |
| 63      | SEG23                 | O   |                 |     |
| 64      | SEG24                 | O   |                 |     |
| 65      | SEG25                 | O   |                 |     |
| 66      | SEG26                 | O   |                 |     |
| 67      | SEG27                 | O   |                 |     |
| 68      | SEG28                 | O   |                 |     |
| 69      | SEG29                 | O   |                 |     |
| 70      | SEG30                 | O   |                 |     |
| 71      | SEG31                 | O   |                 |     |
| 72      | SEG32                 | O   |                 |     |
| 73      | COM1                  | O   |                 |     |
| 74      | COM2                  | O   |                 |     |
| 75      | COM3                  | O   |                 |     |
| 76      | COM4                  | O   |                 |     |
| 77      | V3                    | —   |                 |     |
| 78      | V2                    | —   |                 |     |
| 79      | V1                    | —   | V <sub>CC</sub> | —   |
| 80      | V0                    | —   | V <sub>CC</sub> | —   |

HD4074869

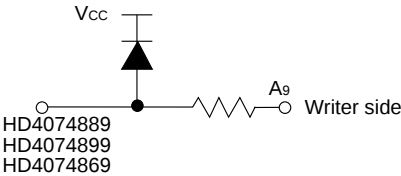
| Pin No. |        | MCU Mode                         |     | PROM Mode       |     |
|---------|--------|----------------------------------|-----|-----------------|-----|
| FP-64A  | DP-64S | Pin Name                         | I/O | Pin Name        | I/O |
| 1       | 8      | R7 <sub>7</sub> /AN0             | I/O | V <sub>CC</sub> | —   |
| 2       | 9      | R7 <sub>7</sub> /AN1             | I/O | V <sub>CC</sub> | —   |
| 3       | 10     | R7 <sub>7</sub> /AN2             | I/O |                 |     |
| 4       | 11     | R7 <sub>7</sub> /AN3             | I/O |                 |     |
| 5       | 12     | TEST                             | I   | V <sub>PP</sub> | —   |
| 6       | 13     | OSC1                             | I   | V <sub>CC</sub> | —   |
| 7       | 14     | OSC2                             | O   |                 |     |
| 8       | 15     | GND                              | —   | GND             | —   |
| 9       | 16     | X2                               | O   |                 |     |
| 10      | 17     | X1                               | I   | GND             | —   |
| 11      | 18     | RESET                            | I   | RESET           | I   |
| 12      | 19     | V <sub>CC</sub>                  | —   | V <sub>CC</sub> | —   |
| 13      | 20     | D <sub>0</sub> /INT <sub>0</sub> | I/O | A <sub>0</sub>  | I   |
| 14      | 21     | D <sub>1</sub> /INT <sub>1</sub> | I/O |                 |     |
| 15      | 22     | D <sub>2</sub>                   | I/O | A <sub>5</sub>  | I   |
| 16      | 23     | D <sub>3</sub>                   | I/O | A <sub>6</sub>  | I   |
| 17      | 24     | D <sub>4</sub>                   | I/O | A <sub>7</sub>  | I   |
| 18      | 25     | D <sub>5</sub>                   | I/O | A <sub>8</sub>  | I   |
| 19      | 26     | D <sub>6</sub>                   | I/O | A <sub>9</sub>  | I   |
| 20      | 27     | D <sub>7</sub>                   | I/O | A <sub>10</sub> | I   |
| 21      | 28     | D <sub>8</sub>                   | I/O | A <sub>11</sub> | I   |
| 22      | 29     | D <sub>9</sub>                   | I/O | A <sub>12</sub> | I   |
| 23      | 30     | R0 <sub>0</sub> /WU <sub>0</sub> | I/O | V <sub>CC</sub> | —   |
| 24      | 31     | R0 <sub>0</sub> /WU <sub>1</sub> | I/O |                 |     |
| 25      | 32     | R0 <sub>0</sub> /WU <sub>2</sub> | I/O |                 |     |
| 26      | 33     | R1 <sub>0</sub> /EVNB            | I/O |                 |     |
| 27      | 34     | R1 <sub>0</sub>                  | I/O | A <sub>13</sub> | I   |
| 28      | 35     | R1 <sub>0</sub> /BUZZ            | I/O | M0              | I   |
| 29      | 36     | R1 <sub>0</sub> /TOB             | I/O | CE              | I   |
| 30      | 37     | R2 <sub>0</sub> /TOC             | I/O | XM1             | O   |
| 31      | 38     | R2 <sub>0</sub> /SCKN            | I/O | OE              | I   |
| 32      | 39     | R2 <sub>0</sub> /SI/SO           | I/O | XM0             | O   |

| Pin No. |        | MCU Mode               |     | PROM Mode       |     |
|---------|--------|------------------------|-----|-----------------|-----|
| FP-64A  | DP-64S | Pin Name               | I/O | Pin Name        | I/O |
| 33      | 40     | R2 <sub>0</sub>        | I/O | A <sub>14</sub> | I   |
| 34      | 41     | R3 <sub>0</sub> /SEG1  | I/O | A <sub>1</sub>  | I   |
| 35      | 42     | R3 <sub>0</sub> /SEG2  | I/O | A <sub>2</sub>  | I   |
| 36      | 43     | R3 <sub>0</sub> /SEG3  | I/O | A <sub>3</sub>  | I   |
| 37      | 44     | R3 <sub>0</sub> /SEG4  | I/O | A <sub>4</sub>  | I   |
| 38      | 45     | R4 <sub>0</sub> /SEG5  | I/O | O <sub>0</sub>  | I/O |
| 39      | 46     | R4 <sub>0</sub> /SEG6  | I/O | O <sub>1</sub>  | I/O |
| 40      | 47     | R4 <sub>0</sub> /SEG7  | I/O | O <sub>2</sub>  | I/O |
| 41      | 48     | R4 <sub>0</sub> /SEG8  | I/O | O <sub>3</sub>  | I/O |
| 42      | 49     | R5 <sub>0</sub> /SEG9  | I/O | O <sub>4</sub>  | I/O |
| 43      | 50     | R5 <sub>0</sub> /SEG10 | I/O | O <sub>4</sub>  | I/O |
| 44      | 51     | R5 <sub>0</sub> /SEG11 | I/O | O <sub>3</sub>  | I/O |
| 45      | 52     | R5 <sub>0</sub> /SEG12 | I/O | O <sub>2</sub>  | I/O |
| 46      | 53     | R6 <sub>0</sub> /SEG13 | I/O | O <sub>1</sub>  | I/O |
| 47      | 54     | R6 <sub>0</sub> /SEG14 | I/O | O <sub>0</sub>  | I/O |
| 48      | 55     | R6 <sub>0</sub> /SEG15 | I/O |                 |     |
| 49      | 56     | R6 <sub>0</sub> /SEG16 | I/O |                 |     |
| 50      | 57     | SEG17                  | O   |                 |     |
| 51      | 58     | SEG18                  | O   |                 |     |
| 52      | 59     | SEG19                  | O   |                 |     |
| 53      | 60     | SEG20                  | O   |                 |     |
| 54      | 61     | SEG21                  | O   |                 |     |
| 55      | 62     | SEG22                  | O   |                 |     |
| 56      | 63     | SEG23                  | O   |                 |     |
| 57      | 64     | SEG24                  | O   |                 |     |
| 58      | 1      | COM1                   | O   |                 |     |
| 59      | 2      | COM2                   | O   |                 |     |
| 60      | 3      | COM3                   | O   |                 |     |
| 61      | 4      | COM4                   | O   |                 |     |
| 62      | 5      | V <sub>3</sub>         | —   |                 |     |
| 63      | 6      | V <sub>2</sub>         | —   |                 |     |
| 64      | 7      | V <sub>1</sub>         | —   | V <sub>CC</sub> | —   |

- Notes:
1. I/O: I/O pin, I: Input-only pin, O: Output-only pin
  2. As there are two each of pins O<sub>0</sub> to O<sub>4</sub>, the respective pairs should be shorted.
  3. Unused data pins (O<sub>5</sub> to O<sub>7</sub>) on the PROM programmer side should be handled as shown below on the socket.



4. Pin A<sub>9</sub> should be handled as shown below on the socket.



## 2. Pin Functions in PROM Mode

### **$V_{PP}$ :**

Applies the on-chip PROM programming voltage (12.5 V  $\pm$ 0.3 V).

### **$\overline{CE}$ :**

Inputs a control signal to set the on-chip PROM to the write/verify enabled state.

### **$\overline{OE}$ :**

Inputs a data output control signal during verification.

### **$A_0$ to $A_{14}$ :**

On-chip PROM address input pins.

### **$O_0$ to $O_4$ :**

On-chip PROM data bus I/O pins.

As there are two each of pins  $O_0$  to  $O_4$ , the respective pairs should be shorted.

### **$\overline{M}_0$ , $\overline{M}_1$ , $\overline{RESET}$ , $\overline{TEST}$ :**

PROM mode setting pins. PROM mode is set by driving the  $\overline{M}_0$ ,  $\overline{M}_1$ , and  $\overline{RESET}$  pins low (or by driving the  $\overline{M}_0$ , and  $\overline{RESET}$  pins low in the HD4074869), and driving the  $\overline{TEST}$  pin to the  $V_{PP}$  level.

### **Other pins:**

$V_{CC}$ ,  $AV_{CC}$ ,  $R7_0/AN_0$ ,  $R7_1/AN_1$ ,  $OSC_1$ ,  $V_0$ , and  $V_1$  should be connected to  $V_{CC}$  potential.

$GND$ ,  $AV_{SS}$ , and  $X1$  should be connected to  $GND$  potential.

Other pins should be left open.

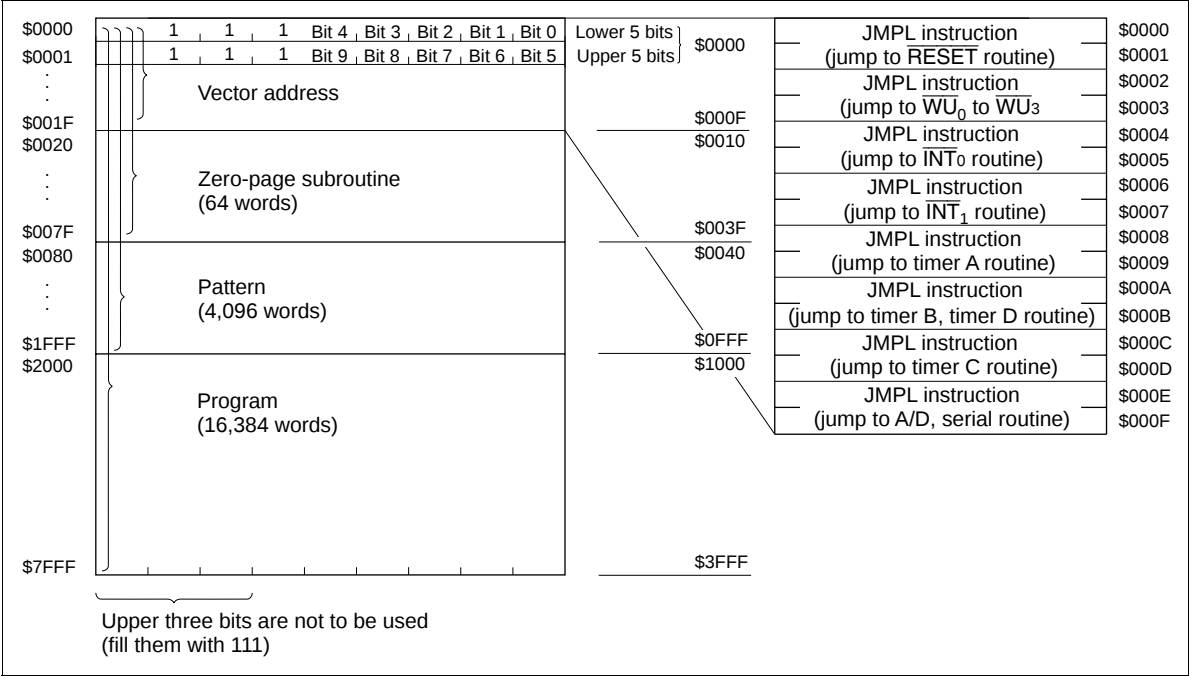


Figure 95 Memory Map in PROM Mode

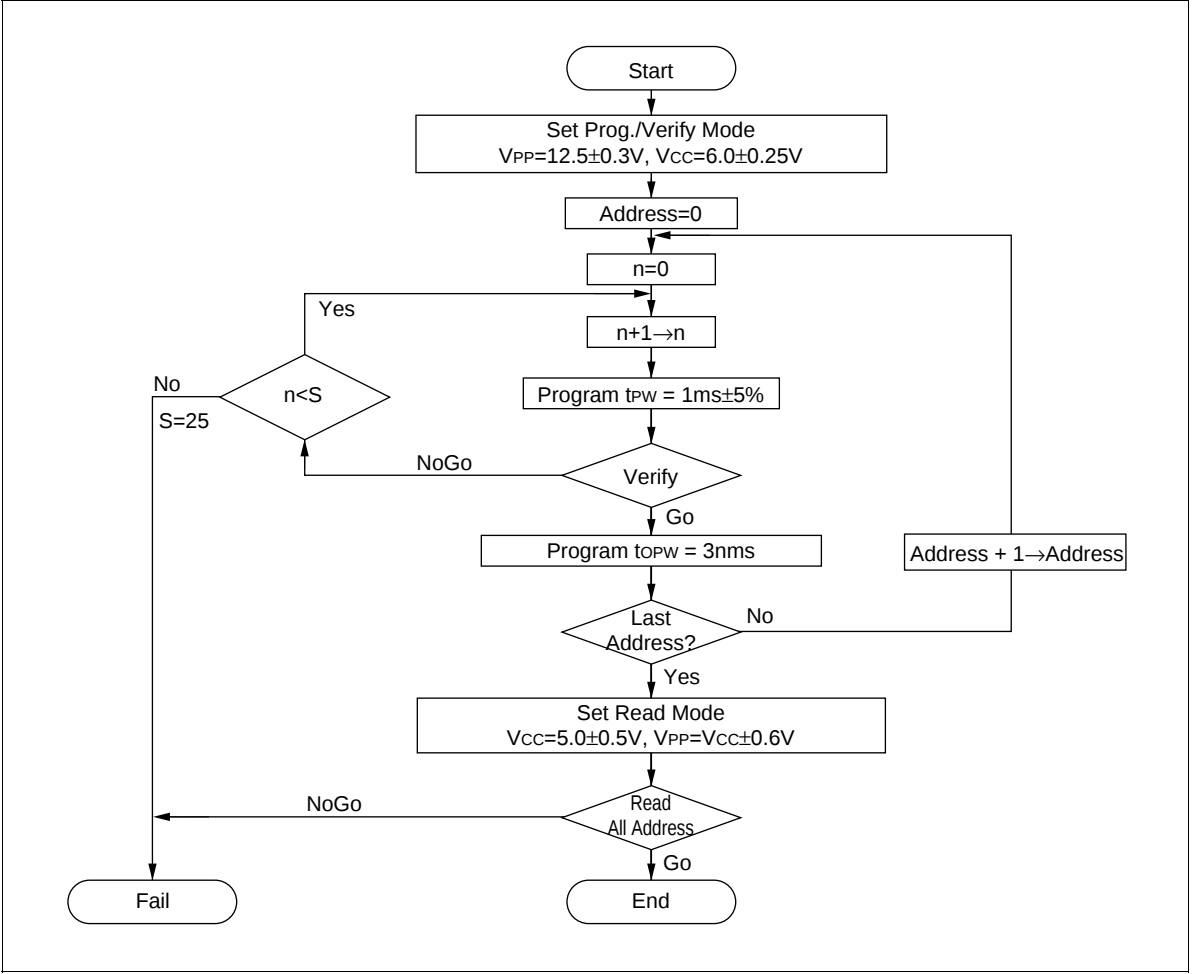


Figure 96 Flowchart of High-Speed Programming

## Programming Electrical Characteristics

**DC Characteristics** ( $V_{CC} = 6V \pm 0.25V$ ,  $V_{PP} = 12.5V \pm 0.3V$ ,  $V_{SS} = 0V$ ,  $T_a = 25^\circ C \pm 5^\circ C$ , unless otherwise specified)

| Item                  |                                                                           | Symbol     | Test Conditions       | min  | typ | max          | Unit    |
|-----------------------|---------------------------------------------------------------------------|------------|-----------------------|------|-----|--------------|---------|
| Input high voltage    | $O_0$ to $O_4$ , $A_0$ to $A_{14}$ ,<br>$\overline{OE}$ , $\overline{CE}$ | $V_{IH}$   |                       | 2.2  | —   | $V_{CC}+0.3$ | V       |
| Input low voltage     | $O_0$ to $O_4$ , $A_0$ to $A_{14}$ ,<br>$\overline{OE}$ , $\overline{CE}$ | $V_{IL}$   |                       | -0.3 | —   | 0.8          | V       |
| Output high voltage   | $O_0$ to $O_4$                                                            | $V_{OH}$   | $I_{OH} = -200\mu A$  | 2.4  | —   | —            | V       |
| Output low voltage    | $O_0$ to $O_4$                                                            | $V_{OL}$   | $I_{OL} = 1.6mA$      | —    | —   | 0.4          | V       |
| Input leakage current | $O_0$ to $O_4$ , $A_0$ to $A_{14}$ ,<br>$\overline{OE}$ , $\overline{CE}$ | $ I_{IL} $ | $V_{in} = 5.25V/0.5V$ | —    | —   | 2            | $\mu A$ |
| $V_{CC}$ current      |                                                                           | $I_{CC}$   |                       | —    | —   | 30           | mA      |
| $V_{PP}$ current      |                                                                           | $I_{PP}$   |                       | —    | —   | 40           | mA      |

**AC Characteristics** ( $V_{CC} = 6V \pm 0.25V$ ,  $V_{PP} = 12.5V \pm 0.3V$ ,  $T_a = 25^\circ C \pm 5^\circ C$ , unless otherwise specified)

| Item                                               | Symbol    | Test Conditions | min  | typ | max   | Unit    |
|----------------------------------------------------|-----------|-----------------|------|-----|-------|---------|
| Address setup time                                 | $t_{AS}$  | See figure 89   | 2    | —   | —     | $\mu s$ |
| $\overline{OE}$ setup time                         | $t_{OES}$ |                 | 2    | —   | —     | $\mu s$ |
| Data setup time                                    | $t_{DS}$  |                 | 2    | —   | —     | $\mu s$ |
| Address hold time                                  | $t_{AH}$  |                 | 0    | —   | —     | $\mu s$ |
| Data hold time                                     | $t_{DH}$  |                 | 2    | —   | —     | $\mu s$ |
| Data output disable time                           | $t_{DF}$  |                 | —    | —   | 130   | ns      |
| $V_{PP}$ setup time                                | $t_{VPS}$ |                 | 2    | —   | —     | $\mu s$ |
| Program pulse width                                | $t_{PW}$  |                 | 0.95 | 1.0 | 1.05  | ms      |
| $\overline{CE}$ pulse width during overprogramming | $t_{OPW}$ |                 | 2.85 | —   | 78.75 | ms      |
| $V_{CC}$ setup time                                | $t_{VCS}$ |                 | 2    | —   | —     | $\mu s$ |
| Data output delay time                             | $t_{OE}$  |                 | 0    | —   | 500   | ns      |

Notes: Input pulse level: 0.8 V to 2.2 V

Input rise/fall times:  $\leq 20ns$

Input timing reference levels: 1.0 V, 2.0 V

Output timing reference levels: 0.8 V, 2.0 V

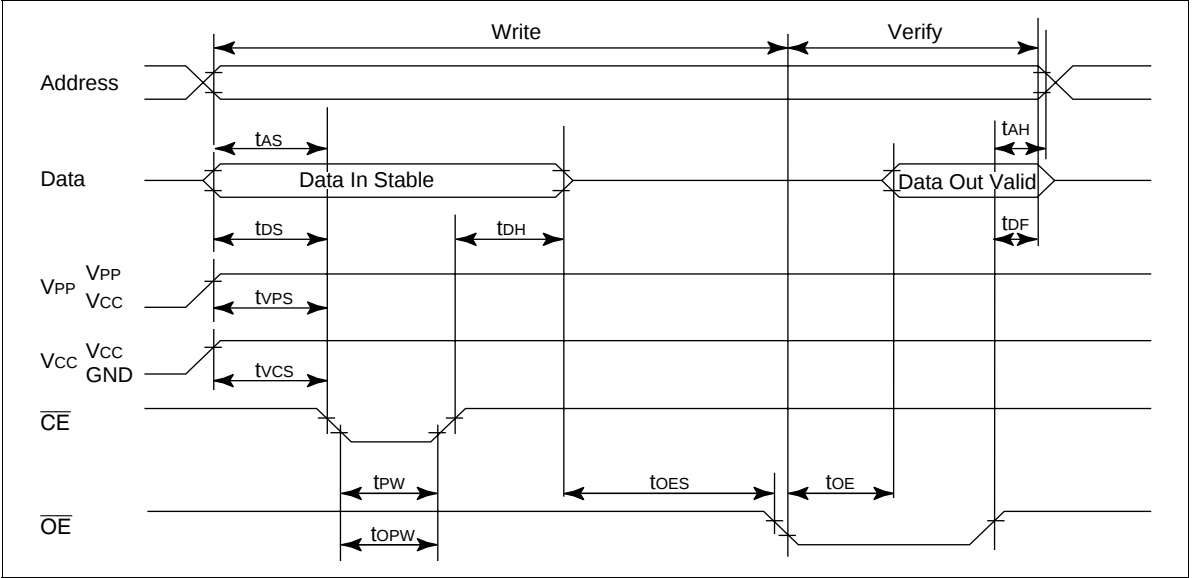


Figure 97 PROM Write/Verify Timing

## Notes on PROM Programming

**Principles of Programming/Erase:** A memory cell in a ZTAT™ microcomputer is the same as an EPROM cell; it is programmed by applying a high voltage between its control gate and drain to inject hot electrons into its floating gate. These electrons are stable, surrounded by an energy barrier formed by an  $\text{SiO}_2$  film. The change in threshold voltage of a memory cell with a charged floating gate makes the corresponding bit appear as 0; a cell whose floating gate is not charged appears as a 1 bit (figure 98).

The charge in a memory cell may decrease with time. This decrease is usually due to one of the following causes:

- Ultraviolet light excites electrons, allowing them to escape. This effect is the basis of the erasure principle.
- Heat excites trapped electrons, allowing them to escape.
- High voltages between the control gate and drain may erase electrons.

If the oxide film covering a floating gate is defective, the electron erasure rate will be greater. However, electron erasure does not often occur because defective devices are detected and removed at the testing stage.

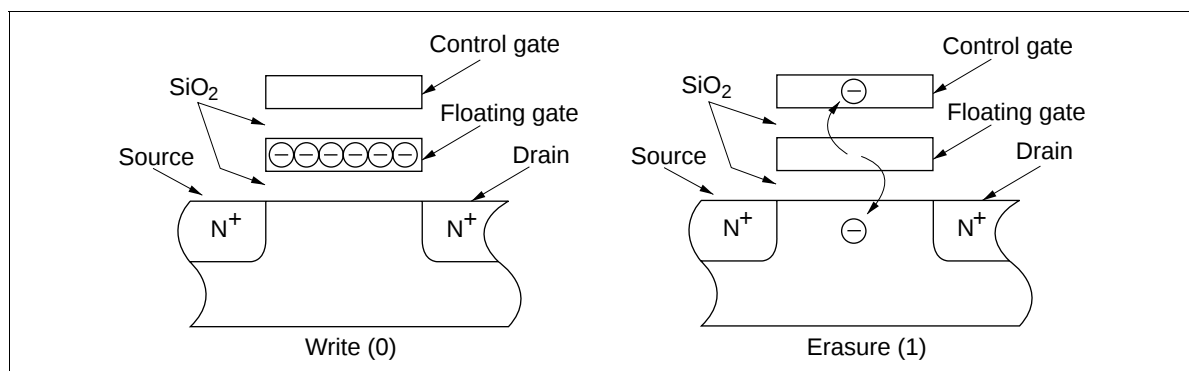


Figure 98 Cross-Sections of a PROM Cell

**PROM Programming:** PROM memory cells must be programmed under specific voltage and timing conditions. The higher the programming voltage  $V_{pp}$  and the longer the programming pulse  $t_{pw}$  is applied, the more electrons are injected into the floating gates. However, if  $V_{pp}$  exceeds specifications, the pn junctions may be permanently damaged. Pay particular attention to overshooting in the PROM programmer. In addition, note that negative voltage noise will produce a parasitic transistor effect that may reduce breakdown voltages.

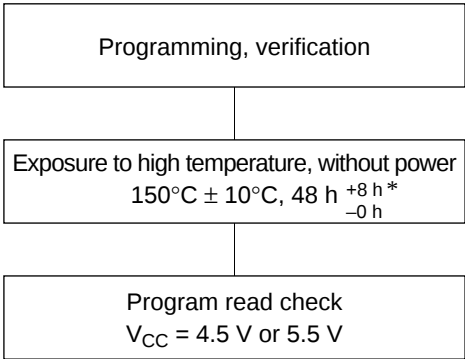
The ZTAT™ microcomputer is electrically connected to the PROM programmer by a socket adapter. Therefore, note the following points:

- Check that the socket adapter is firmly mounted on the PROM programmer.
- Do not touch the socket adapter or the LSI during the programming. Touching them may affect the quality of the contacts, which will cause programming errors.

**PROM Reliability after Programming:** In general, semiconductor devices retain their reliability, provided that some initial defects can be excluded. These initial defects can be detected and rejected by screening. Baking devices under high-temperature conditions is one method of screening that can rapidly eliminate data-hold defects in memory cells. (Refer to the previous Principles of Programming/Erasure section.)

ZTAT™ microcomputer devices are extremely reliable because they have been subjected to such a screening method during the wafer fabrication process, but Hitachi recommends that each device be exposed to 150°C at one atmosphere for at least 48 hours after it is programmed, to ensure its best performance. The recommended screening procedure is shown in figure 99.

Note: If programming errors occur continuously during PROM programming, suspend programming and check for problems in the PROM programmer or socket adapter. If programming verification indicates errors in programming or after high-temperature exposure, please inform Hitachi.



Note: Exposure time is measured from when the temperature in the heater reaches 150°C.

Figure 99 Recommended Screening Procedure

Addressing Modes

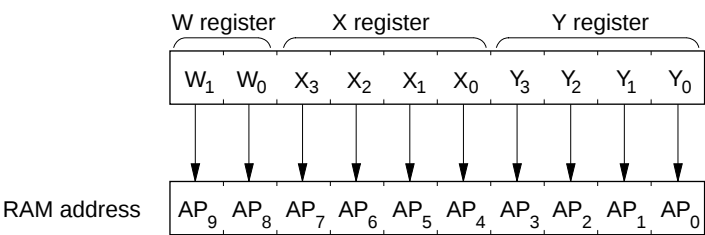
RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 100 and described below.

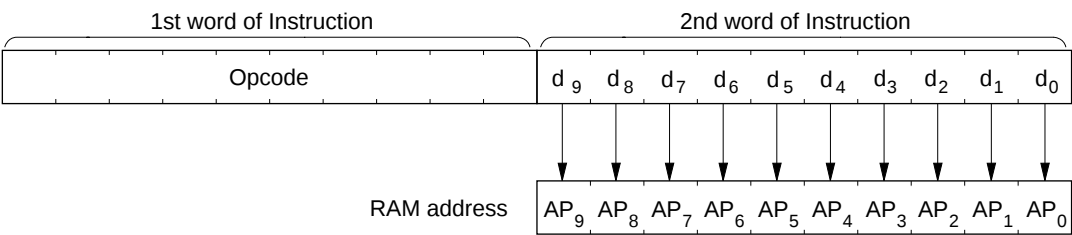
**Register Indirect Addressing Mode:** The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address.

**Direct Addressing Mode:** A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

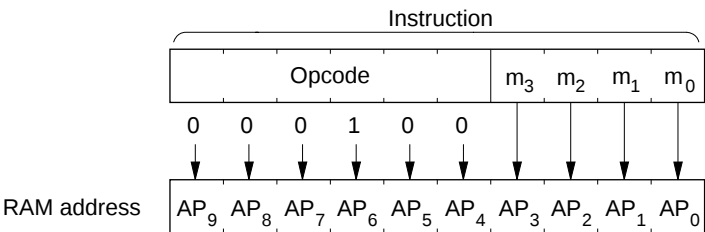
**Memory Register Addressing Mode:** The memory registers (MR), which are located in 16 addresses from \$040 to \$04F, are accessed with the LAMR and XMRA instructions.



Register Indirect Addressing



Direct Addressing



Memory Register Addressing

Figure 100 RAM Addressing Modes

## **ROM Addressing Modes and the P Instruction**

The MCU has four ROM addressing modes, as shown in figure 101 and described below.

**Direct Addressing Mode:** A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC<sub>13</sub>–PC<sub>0</sub>) with 14-bit immediate data.

**Current Page Addressing Mode:** The MCU has 64 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC<sub>7</sub>–PC<sub>0</sub>) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transfers the PC contents to the next physical page, as shown in figure 103. This means that the execution of the BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-series cross assembler has an automatic paging feature for ROM pages.

**Zero-Page Addressing Mode:** A program can branch to the zero-page subroutine area located at \$0000–\$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC<sub>5</sub>–PC<sub>0</sub>), and 0s are placed in the eight high-order bits (PC<sub>13</sub>–PC<sub>6</sub>).

**Table Data Addressing Mode:** A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

**P Instruction:** ROM data addressed in table data addressing mode can be referenced with the P instruction as shown in figure 102. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R1 and R2 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

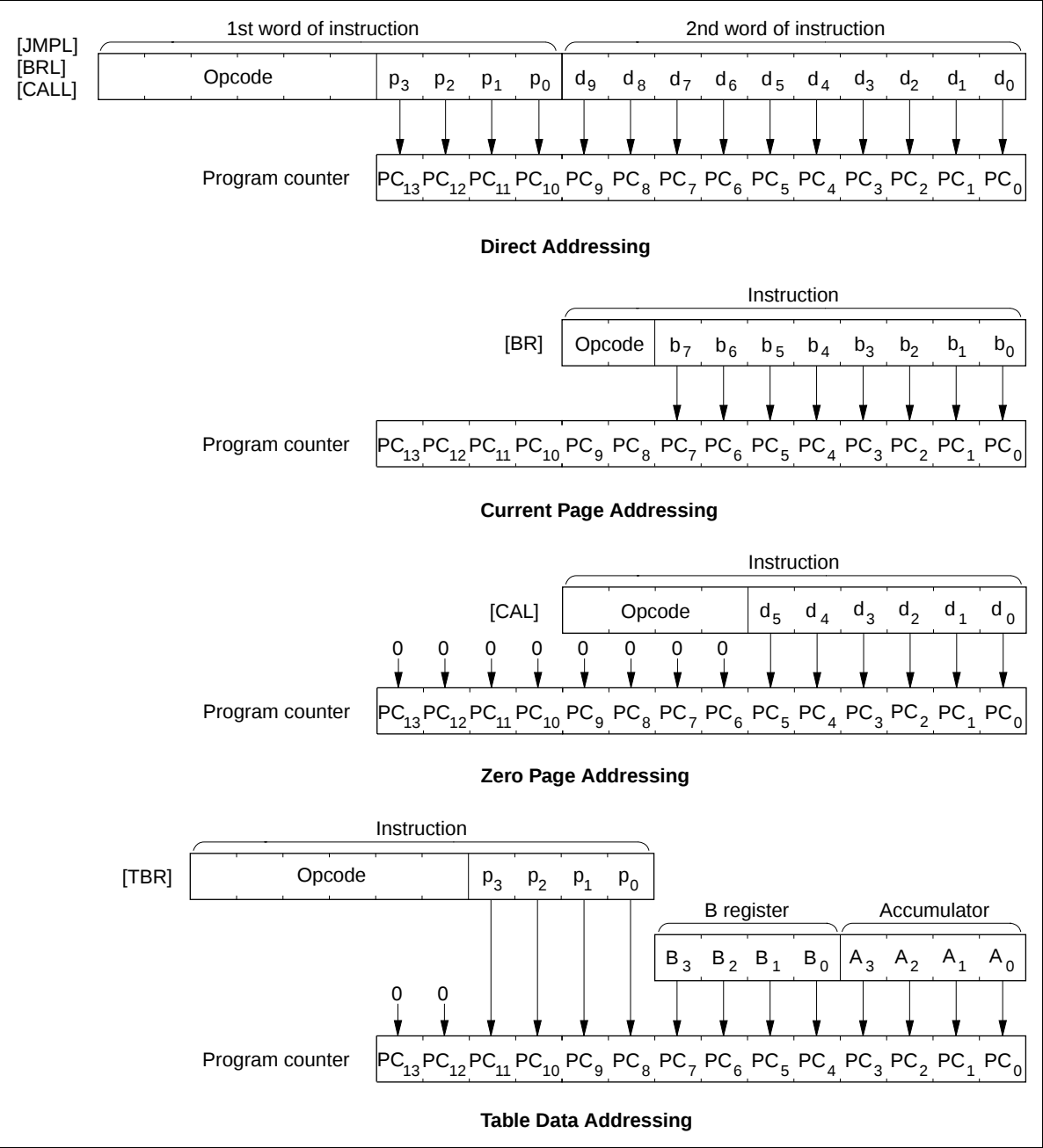


Figure 101 ROM Addressing Modes

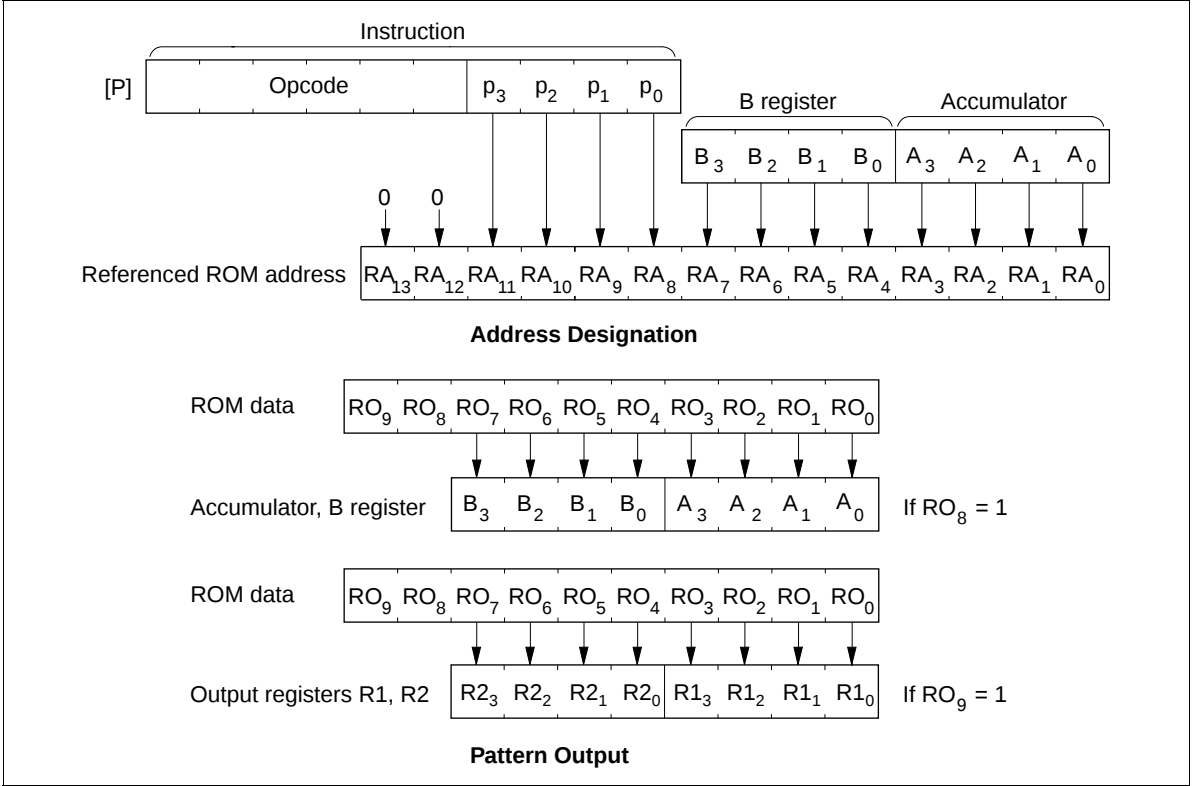


Figure 102 P Instruction

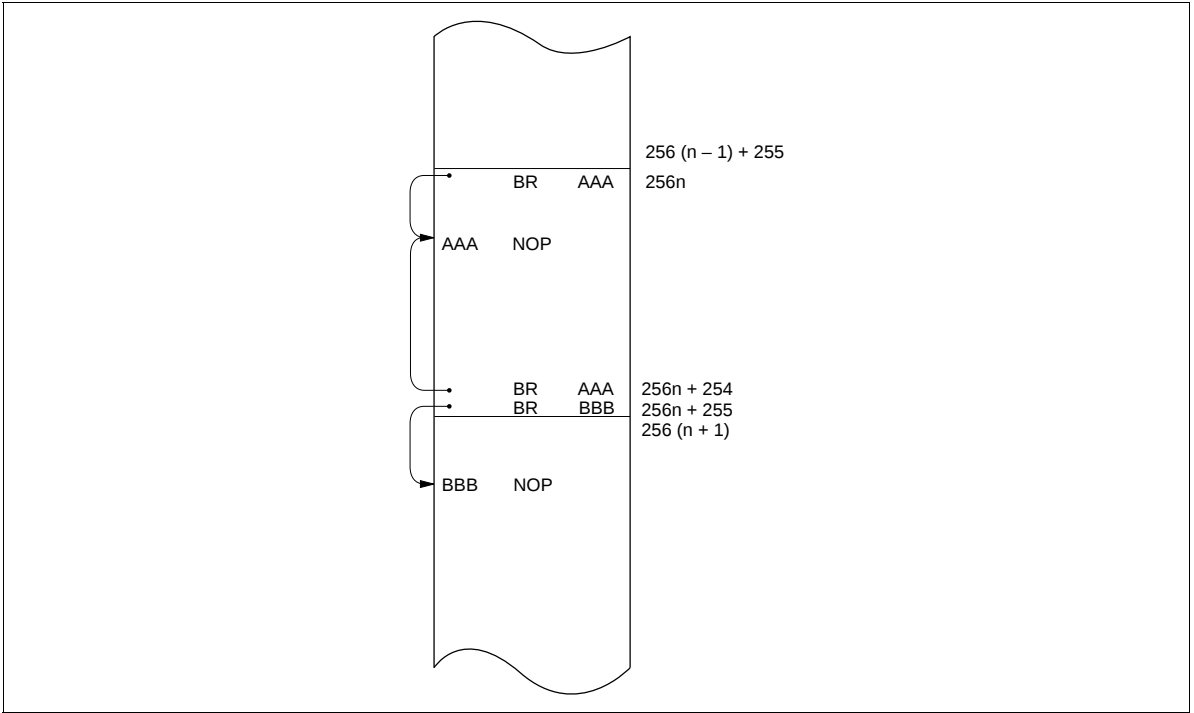


Figure 103 Branching when the Branch Destination is on a Page Boundary

## Instruction Set

The MCU Series has 101 instructions, classified into the following 10 groups:

- Immediate instructions
- Register-to-register instructions
- RAM addressing instructions
- RAM register instructions
- Arithmetic instructions
- Compare instructions
- RAM bit manipulation instructions
- ROM addressing instructions
- Input/output instructions
- Control instructions

The functions of these instructions are listed in tables 31 to 40, and an opcode map is shown in table 41.

**Table 31 Immediate Instructions**

| Operation                               | Mnemonic | Operation Code                                                                                     | Function                               | Status | Words/<br>Cycles |
|-----------------------------------------|----------|----------------------------------------------------------------------------------------------------|----------------------------------------|--------|------------------|
| Load A from immediate                   | LAI i    | 1 0 0 0 1 1 $i_3$ $i_2$ $i_1$ $i_0$                                                                | $i \rightarrow A$                      |        | 1/1              |
| Load B from immediate                   | LBI i    | 1 0 0 0 0 0 $i_3$ $i_2$ $i_1$ $i_0$                                                                | $i \rightarrow B$                      |        | 1/1              |
| Load memory from immediate              | LMID i,d | 0 1 1 0 1 0 $i_3$ $i_2$ $i_1$ $i_0$<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | $i \rightarrow M$                      |        | 2/2              |
| Load memory from immediate, increment Y | LMIIY i  | 1 0 1 0 0 1 $i_3$ $i_2$ $i_1$ $i_0$                                                                | $i \rightarrow M, Y + 1 \rightarrow Y$ | NZ     | 1/1              |

Table 32 Register-Register Instructions

| Operation         | Mnemonic | Operation Code                             | Function                  | Status | Words/<br>Cycles |
|-------------------|----------|--------------------------------------------|---------------------------|--------|------------------|
| Load A from B     | LAB      | 0 0 0 1 0 0 1 0 0 0                        | $B \rightarrow A$         |        | 1/1              |
| Load B from A     | LBA      | 0 0 1 1 0 0 1 0 0 0                        | $A \rightarrow B$         |        | 1/1              |
| Load A from W     | LAW      | 0 1 0 0 0 0 0 0 0 0<br>0 0 0 0 0 0 0 0 0 0 | $W \rightarrow A$         |        | 2/2*             |
| Load A from Y     | LAY      | 0 0 1 0 1 0 1 1 1 1                        | $Y \rightarrow A$         |        | 1/1              |
| Load A from SPX   | LASPX    | 0 0 0 1 1 0 1 0 0 0                        | $SPX \rightarrow A$       |        | 1/1              |
| Load A from SPY   | LASPY    | 0 0 0 1 0 1 1 0 0 0                        | $SPY \rightarrow A$       |        | 1/1              |
| Load A from MR    | LAMR m   | 1 0 0 1 1 1 $m_3 m_2 m_1 m_0$              | $MR(m) \rightarrow A$     |        | 1/1              |
| Exchange MR and A | XMRA m   | 1 0 1 1 1 1 $m_3 m_2 m_1 m_0$              | $MR(m) \leftrightarrow A$ |        | 1/1              |

Note: The assembler automatically provides an operand for the second word of the LAW instruction.

Table 33 RAM Address Instructions

| Operation                        | Mnemonic | Operation Code                             | Function                                       | Status | Words/<br>Cycles |
|----------------------------------|----------|--------------------------------------------|------------------------------------------------|--------|------------------|
| Load W from immediate            | LWI i    | 0 0 1 1 1 1 0 0 $i_1 i_0$                  | $i \rightarrow W$                              |        | 1/1              |
| Load X from immediate            | LXI i    | 1 0 0 0 1 0 $i_3 i_2 i_1 i_0$              | $i \rightarrow X$                              |        | 1/1              |
| Load Y from immediate            | LYI i    | 1 0 0 0 0 1 $i_3 i_2 i_1 i_0$              | $i \rightarrow Y$                              |        | 1/1              |
| Load W from A                    | LWA      | 0 1 0 0 0 1 0 0 0 0<br>0 0 0 0 0 0 0 0 0 0 | $A \rightarrow W$                              |        | 2/2*             |
| Load X from A                    | LXA      | 0 0 1 1 1 0 1 0 0 0                        | $A \rightarrow X$                              |        | 1/1              |
| Load Y from A                    | LYA      | 0 0 1 1 0 1 1 0 0 0                        | $A \rightarrow Y$                              |        | 1/1              |
| Increment Y                      | IY       | 0 0 0 1 0 1 1 1 0 0                        | $Y + 1 \rightarrow Y$                          | NZ     | 1/1              |
| Decrement Y                      | DY       | 0 0 1 1 0 1 1 1 1 1                        | $Y - 1 \rightarrow Y$                          | NB     | 1/1              |
| Add A to Y                       | AYY      | 0 0 0 1 0 1 0 1 0 0                        | $Y + A \rightarrow Y$                          | OVF    | 1/1              |
| Subtract A from Y                | SY Y     | 0 0 1 1 0 1 0 1 0 0                        | $Y - A \rightarrow Y$                          | NB     | 1/1              |
| Exchange X and SPX               | XSPX     | 0 0 0 0 0 0 0 0 0 1                        | $X \leftrightarrow SPX$                        |        | 1/1              |
| Exchange Y and SPY               | XSPY     | 0 0 0 0 0 0 0 0 1 0                        | $Y \leftrightarrow SPY$                        |        | 1/1              |
| Exchange X and SPX,<br>Y and SPY | XSPXY    | 0 0 0 0 0 0 0 0 1 1                        | $X \leftrightarrow SPX, Y \leftrightarrow SPY$ |        | 1/1              |

Note: The assembler automatically provides an operand for the second word of the LWA instruction.

**Table 34 RAM Register Instructions**

| Operation                          | Mnemonic | Operation Code                                                                     | Function                                                            | Status | Words/<br>Cycles |
|------------------------------------|----------|------------------------------------------------------------------------------------|---------------------------------------------------------------------|--------|------------------|
| Load A from memory                 | LAM      | 0 0 1 0 0 1 0 0 0 0                                                                | $M \rightarrow A$                                                   |        | 1/1              |
|                                    | LAMX     | 0 0 1 0 0 1 0 0 0 1                                                                | $M \rightarrow A$<br>$X \leftrightarrow SPX$                        |        |                  |
|                                    | LAMY     | 0 0 1 0 0 1 0 0 1 0                                                                | $M \rightarrow A$<br>$Y \leftrightarrow SPY$                        |        |                  |
|                                    | LAMXY    | 0 0 1 0 0 1 0 0 1 1                                                                | $M \rightarrow A$<br>$X \leftrightarrow SPX, Y \leftrightarrow SPY$ |        |                  |
| Load A from memory                 | LAMD d   | 0 1 1 0 0 1 0 0 0 0<br>$d_9 \ d_8 \ d_7 \ d_6 \ d_5 \ d_4 \ d_3 \ d_2 \ d_1 \ d_0$ | $M \rightarrow A$                                                   |        | 2/2              |
| Load B from memory                 | LBM      | 0 0 0 1 0 0 0 0 0 0                                                                | $M \rightarrow B$                                                   |        | 1/1              |
|                                    | LBMX     | 0 0 0 1 0 0 0 0 0 1                                                                | $M \rightarrow B$<br>$X \leftrightarrow SPX$                        |        |                  |
|                                    | LBMY     | 0 0 0 1 0 0 0 0 1 0                                                                | $M \rightarrow B$<br>$Y \leftrightarrow SPY$                        |        |                  |
|                                    | LBMXY    | 0 0 0 1 0 0 0 0 1 1                                                                | $M \rightarrow B$<br>$X \leftrightarrow SPX, Y \leftrightarrow SPY$ |        |                  |
| Load memory from A                 | LMA      | 0 0 1 0 0 1 0 1 0 0                                                                | $A \rightarrow M$                                                   |        | 1/1              |
|                                    | LMAX     | 0 0 1 0 0 1 0 1 0 1                                                                | $A \rightarrow M$<br>$X \leftrightarrow SPX$                        |        |                  |
|                                    | LMA Y    | 0 0 1 0 0 1 0 1 1 0                                                                | $A \rightarrow M$<br>$Y \leftrightarrow SPY$                        |        |                  |
|                                    | LMAXY    | 0 0 1 0 0 1 0 1 1 1                                                                | $A \rightarrow M$<br>$X \leftrightarrow SPX, Y \leftrightarrow SPY$ |        |                  |
| Load memory from A                 | LMAD d   | 0 1 1 0 0 1 0 1 0 0<br>$d_9 \ d_8 \ d_7 \ d_6 \ d_5 \ d_4 \ d_3 \ d_2 \ d_1 \ d_0$ | $A \rightarrow M$                                                   |        | 2/2              |
| Load memory from A,<br>increment Y | LMAIY    | 0 0 0 1 0 1 0 0 0 0                                                                | $A \rightarrow M, Y + 1 \rightarrow Y$                              | NZ     | 1/1              |
|                                    | LMAIYX   | 0 0 0 1 0 1 0 0 0 1                                                                | $A \rightarrow M, Y + 1 \rightarrow Y$<br>$X \leftrightarrow SPX$   |        |                  |
| Load memory from A,<br>decrement Y | LMADY    | 0 0 1 1 0 1 0 0 0 0                                                                | $A \rightarrow M, Y - 1 \rightarrow Y$                              | NB     | 1/1              |
|                                    | LMADYX   | 0 0 1 1 0 1 0 0 0 1                                                                | $A \rightarrow M, Y - 1 \rightarrow Y$<br>$X \leftrightarrow SPX$   |        |                  |

Table 34 RAM Register Instructions (cont)

| Operation                | Mnemonic | Operation Code                                                                                                                                                                 | Function                  | Status | Words/<br>Cycles |
|--------------------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|--------|------------------|
| Exchange memory<br>and A | XMA      | 0 0 1 0 0 0 0 0 0 0 0                                                                                                                                                          | M ↔ A                     |        | 1/1              |
|                          | XMAX     | 0 0 1 0 0 0 0 0 0 0 1                                                                                                                                                          | M ↔ A<br>X ↔ SPX          |        |                  |
|                          | XMAY     | 0 0 1 0 0 0 0 0 0 1 0                                                                                                                                                          | M ↔ A<br>Y ↔ SPY          |        |                  |
|                          | XMAXY    | 0 0 1 0 0 0 0 0 0 1 1                                                                                                                                                          | M ↔ A<br>X ↔ SPX, Y ↔ SPY |        |                  |
| Exchange memory<br>and A | XMAD d   | 0 1 1 0 0 0 0 0 0 0 0<br>d <sub>9</sub> d <sub>8</sub> d <sub>7</sub> d <sub>6</sub> d <sub>5</sub> d <sub>4</sub> d <sub>3</sub> d <sub>2</sub> d <sub>1</sub> d <sub>0</sub> | M ↔ A                     |        | 2/2              |
| Exchange memory<br>and B | XMB      | 0 0 1 1 0 0 0 0 0 0 0                                                                                                                                                          | M ↔ B                     |        | 1/1              |
|                          | XMBX     | 0 0 1 1 0 0 0 0 0 0 1                                                                                                                                                          | M ↔ B<br>X ↔ SPX          |        |                  |
|                          | XMBY     | 0 0 1 1 0 0 0 0 0 1 0                                                                                                                                                          | M ↔ B<br>Y ↔ SPY          |        |                  |
|                          | XMBXY    | 0 0 1 1 0 0 0 0 0 1 1                                                                                                                                                          | M ↔ B<br>X ↔ SPX, Y ↔ SPY |        |                  |

**Table 35     Arithmetic Instructions**

| Operation                         | Mnemonic | Operation Code                                                                     | Function                                                | Status | Words/<br>Cycles |
|-----------------------------------|----------|------------------------------------------------------------------------------------|---------------------------------------------------------|--------|------------------|
| Add immediate to A                | AI i     | 1 0 1 0 0 0 $i_3$ $i_2$ $i_1$ $i_0$                                                | $A + i \rightarrow A$                                   | OVF    | 1/1              |
| Increment B                       | IB       | 0 0 0 1 0 0 1 1 0 0                                                                | $B + 1 \rightarrow B$                                   | NZ     | 1/1              |
| Decrement B                       | DB       | 0 0 1 1 0 0 1 1 1 1                                                                | $B - 1 \rightarrow B$                                   | NB     | 1/1              |
| Decimal adjust for addition       | DAA      | 0 0 1 0 1 0 0 1 1 0                                                                |                                                         |        | 1/1              |
| Decimal adjust for subtraction    | DAS      | 0 0 1 0 1 0 1 0 1 0                                                                |                                                         |        | 1/1              |
| Negate A                          | NEGA     | 0 0 0 1 1 0 0 0 0 0                                                                | $\bar{A} + 1 \rightarrow A$                             |        | 1/1              |
| Complement B                      | COMB     | 0 1 0 1 0 0 0 0 0 0                                                                | $\bar{B} \rightarrow B$                                 |        | 1/1              |
| Rotate right A with carry         | ROTR     | 0 0 1 0 1 0 0 0 0 0                                                                |                                                         |        | 1/1              |
| Rotate left A with carry          | ROTL     | 0 0 1 0 1 0 0 0 0 1                                                                |                                                         |        | 1/1              |
| Set carry                         | SEC      | 0 0 1 1 1 0 1 1 1 1                                                                | $1 \rightarrow CA$                                      |        | 1/1              |
| Reset carry                       | REC      | 0 0 1 1 1 0 1 1 0 0                                                                | $0 \rightarrow CA$                                      |        | 1/1              |
| Test carry                        | TC       | 0 0 0 1 1 0 1 1 1 1                                                                |                                                         | CA     | 1/1              |
| Add A to memory                   | AM       | 0 0 0 0 0 0 1 0 0 0                                                                | $M + A \rightarrow A$                                   | OVF    | 1/1              |
| Add A to memory                   | AMD d    | 0 1 0 0 0 0 1 0 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | $M + A \rightarrow A$                                   | OVF    | 2/2              |
| Add A to memory with carry        | AMC      | 0 0 0 0 0 1 1 0 0 0                                                                | $M + A + CA \rightarrow A$<br>$OVF \rightarrow CA$      | OVF    | 1/1              |
| Add A to memory with carry        | AMCD d   | 0 1 0 0 0 1 1 0 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | $M + A + CA \rightarrow A$<br>$OVF \rightarrow CA$      | OVF    | 2/2              |
| Subtract A from memory with carry | SMC      | 0 0 1 0 0 1 1 0 0 0                                                                | $M - A - \bar{CA} \rightarrow A$<br>$NB \rightarrow CA$ | NB     | 1/1              |
| Subtract A from memory with carry | SMCD d   | 0 1 1 0 0 1 1 0 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | $M - A - \bar{CA} \rightarrow A$<br>$NB \rightarrow CA$ | NB     | 2/2              |
| OR A and B                        | OR       | 0 1 0 1 0 0 0 1 0 0                                                                | $A \cup B \rightarrow A$                                |        | 1/1              |
| AND memory with A                 | ANM      | 0 0 1 0 0 1 1 1 0 0                                                                | $A \cap M \rightarrow A$                                | NZ     | 1/1              |
| AND memory with A                 | ANMD d   | 0 1 1 0 0 1 1 1 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | $A \cap M \rightarrow A$                                | NZ     | 2/2              |
| OR memory with A                  | ORM      | 0 0 0 0 0 0 1 1 0 0                                                                | $A \cup M \rightarrow A$                                | NZ     | 1/1              |
| OR memory with A                  | ORMD d   | 0 1 0 0 0 0 1 1 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | $A \cup M \rightarrow A$                                | NZ     | 2/2              |
| EOR memory with A                 | EORM     | 0 0 0 0 0 1 1 1 0 0                                                                | $A \oplus M \rightarrow A$                              | NZ     | 1/1              |
| EOR memory with A                 | EORMD d  | 0 1 0 0 0 1 1 1 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | $A \oplus M \rightarrow A$                              | NZ     | 2/2              |

Table 36 Compare Instructions

| Operation                              | Mnemonic  | Operation Code                                                                                     | Function   | Status | Words/<br>Cycles |
|----------------------------------------|-----------|----------------------------------------------------------------------------------------------------|------------|--------|------------------|
| Immediate not equal to memory          | INEM i    | 0 0 0 0 1 0 $i_3$ $i_2$ $i_1$ $i_0$                                                                | $i \neq M$ | NZ     | 1/1              |
| Immediate not equal to memory          | INEMD i,d | 0 1 0 0 1 0 $i_3$ $i_2$ $i_1$ $i_0$<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | $i \neq M$ | NZ     | 2/2              |
| A not equal to memory                  | ANEM      | 0 0 0 0 0 0 0 1 0 0                                                                                | $A \neq M$ | NZ     | 1/1              |
| A not equal to memory                  | ANEMD d   | 0 1 0 0 0 0 0 1 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$                 | $A \neq M$ | NZ     | 2/2              |
| B not equal to memory                  | BNEM      | 0 0 0 1 0 0 0 1 0 0                                                                                | $B \neq M$ | NZ     | 1/1              |
| Y not equal to immediate               | YNEI i    | 0 0 0 1 1 1 $i_3$ $i_2$ $i_1$ $i_0$                                                                | $Y \neq i$ | NZ     | 1/1              |
| Immediate less than or equal to memory | ILEM i    | 0 0 0 0 1 1 $i_3$ $i_2$ $i_1$ $i_0$                                                                | $i \leq M$ | NB     | 1/1              |
| Immediate less than or equal to memory | ILEMD i,d | 0 1 0 0 1 1 $i_3$ $i_2$ $i_1$ $i_0$<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | $i \leq M$ | NB     | 2/2              |
| A less than or equal to memory         | ALEM      | 0 0 0 0 0 1 0 1 0 0                                                                                | $A \leq M$ | NB     | 1/1              |
| A less than or equal to memory         | ALEMD d   | 0 1 0 0 0 1 0 1 0 0<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$                 | $A \leq M$ | NB     | 2/2              |
| B less than or equal to memory         | BLEM      | 0 0 1 1 0 0 0 1 0 0                                                                                | $B \leq M$ | NB     | 1/1              |
| A less than or equal to immediate      | ALEI i    | 1 0 1 0 1 1 $i_3$ $i_2$ $i_1$ $i_0$                                                                | $A \leq i$ | NB     | 1/1              |

Table 37 RAM Bit Manipulation Instructions

| Operation        | Mnemonic | Operation Code                                                                             | Function             | Status | Words/<br>Cycles |
|------------------|----------|--------------------------------------------------------------------------------------------|----------------------|--------|------------------|
| Set memory bit   | SEM n    | 0 0 1 0 0 0 0 1 $n_1$ $n_0$                                                                | $i \rightarrow M(n)$ |        | 1/1              |
| Set memory bit   | SEMD n,d | 0 1 1 0 0 0 0 1 $n_1$ $n_0$<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | $i \rightarrow M(n)$ |        | 2/2              |
| Reset memory bit | REM n    | 0 0 1 0 0 0 1 0 $n_1$ $n_0$                                                                | $0 \rightarrow M(n)$ |        | 1/1              |
| Reset memory bit | REMD n,d | 0 1 1 0 0 0 1 0 $n_1$ $n_0$<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ | $0 \rightarrow M(n)$ |        | 2/2              |
| Test memory bit  | TM n     | 0 0 1 0 0 0 1 1 $n_1$ $n_0$                                                                |                      | M (n)  | 1/1              |
| Test memory bit  | TM n,d   | 0 1 1 0 0 0 1 1 $n_1$ $n_0$<br>$d_9$ $d_8$ $d_7$ $d_6$ $d_5$ $d_4$ $d_3$ $d_2$ $d_1$ $d_0$ |                      | M (n)  | 2/2              |

**Table 38 ROM Address Instructions**

| Operation                        | Mnemonic | Operation Code                                                                                                                                                                                                                   | Function                  | Status | Words/<br>Cycles |
|----------------------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|--------|------------------|
| Branch on status 1               | BR b     | 1 1 b <sub>7</sub> b <sub>6</sub> b <sub>5</sub> b <sub>4</sub> b <sub>3</sub> b <sub>2</sub> b <sub>1</sub> b <sub>0</sub>                                                                                                      |                           | 1      | 1/1              |
| Long branch on status 1          | BRL u    | 0 1 0 1 1 1 p <sub>3</sub> p <sub>2</sub> p <sub>1</sub> p <sub>0</sub><br>d <sub>9</sub> d <sub>8</sub> d <sub>7</sub> d <sub>6</sub> d <sub>5</sub> d <sub>4</sub> d <sub>3</sub> d <sub>2</sub> d <sub>1</sub> d <sub>0</sub> |                           | 1      | 2/2              |
| Long jump unconditionally        | JMPL u   | 0 1 0 1 0 1 p <sub>3</sub> p <sub>2</sub> p <sub>1</sub> p <sub>0</sub><br>d <sub>9</sub> d <sub>8</sub> d <sub>7</sub> d <sub>6</sub> d <sub>5</sub> d <sub>4</sub> d <sub>3</sub> d <sub>2</sub> d <sub>1</sub> d <sub>0</sub> |                           |        | 2/2              |
| Subroutine jump on status 1      | CAL a    | 0 1 1 1 a <sub>5</sub> a <sub>4</sub> a <sub>3</sub> a <sub>2</sub> a <sub>1</sub> a <sub>0</sub>                                                                                                                                |                           | 1      | 1/2              |
| Long subroutine jump on status 1 | CALL u   | 0 1 0 1 1 0 p <sub>3</sub> p <sub>2</sub> p <sub>1</sub> p <sub>0</sub><br>d <sub>9</sub> d <sub>8</sub> d <sub>7</sub> d <sub>6</sub> d <sub>5</sub> d <sub>4</sub> d <sub>3</sub> d <sub>2</sub> d <sub>1</sub> d <sub>0</sub> |                           | 1      | 2/2              |
| Table branch                     | TBR p    | 0 0 1 0 1 1 p <sub>3</sub> p <sub>2</sub> p <sub>1</sub> p <sub>0</sub>                                                                                                                                                          |                           | 1      | 1/1              |
| Return from subroutine           | RTN      | 0 0 0 0 0 1 0 0 0 0                                                                                                                                                                                                              |                           |        | 1/3              |
| Return from interrupt            | RTNI     | 0 0 0 0 0 1 0 0 0 1                                                                                                                                                                                                              | 1 → IE,<br>carry restored | ST     | 1/1              |

**Table 39 Input/Output Instructions**

| Operation                       | Mnemonic | Operation Code                                                          | Function  | Status | Words/<br>Cycles |
|---------------------------------|----------|-------------------------------------------------------------------------|-----------|--------|------------------|
| Set discrete I/O latch          | SED      | 0 0 1 1 1 0 0 1 0 0                                                     | 1 → D (Y) |        | 1/1              |
| Set discrete I/O latch direct   | SEDD m   | 1 0 1 1 1 0 m <sub>3</sub> m <sub>2</sub> m <sub>1</sub> m <sub>0</sub> | 1 → D (m) |        | 1/1              |
| Reset discrete I/O latch        | RED      | 0 0 0 1 1 0 0 1 0 0                                                     | 0 → D (Y) |        | 1/1              |
| Reset discrete I/O latch direct | REDD m   | 1 0 0 1 1 0 m <sub>3</sub> m <sub>2</sub> m <sub>1</sub> m <sub>0</sub> | 0 → D (m) |        | 1/1              |
| Test discrete I/O latch         | TD       | 0 0 1 1 1 0 0 0 0 0                                                     |           | D (Y)  | 1/1              |
| Test discrete I/O latch direct  | TDD m    | 1 0 1 0 1 0 m <sub>3</sub> m <sub>2</sub> m <sub>1</sub> m <sub>0</sub> |           | D (m)  | 1/1              |
| Load A from R-port register     | LAR m    | 1 0 0 1 0 1 m <sub>3</sub> m <sub>2</sub> m <sub>1</sub> m <sub>0</sub> | R (m) → A |        | 1/1              |
| Load B from R-port register     | LBR m    | 1 0 0 1 0 0 m <sub>3</sub> m <sub>2</sub> m <sub>1</sub> m <sub>0</sub> | R (m) → B |        | 1/1              |
| Load R-port register from A     | LRA m    | 1 0 1 1 0 1 m <sub>3</sub> m <sub>2</sub> m <sub>1</sub> m <sub>0</sub> | A → R (m) |        | 1/1              |
| Load R-port register from B     | LRB m    | 1 0 1 1 0 0 m <sub>3</sub> m <sub>2</sub> m <sub>1</sub> m <sub>0</sub> | B → R (m) |        | 1/1              |
| Pattern generation              | P p      | 0 1 1 0 1 1 p <sub>3</sub> p <sub>2</sub> p <sub>1</sub> p <sub>0</sub> |           |        | 1/2              |

Table 40 Control Instructions

| Operation                | Mnemonic | Operation Code      | Function | Status | Words/<br>Cycles |
|--------------------------|----------|---------------------|----------|--------|------------------|
| No operation             | NOP      | 0 0 0 0 0 0 0 0 0 0 |          |        | 1/1              |
| Start serial             | STS      | 0 1 0 1 0 0 1 0 0 0 |          |        | 1/1              |
| Standby mode/watch mode* | SBY      | 0 1 0 1 0 0 1 1 0 0 |          |        | 1/1              |
| Stop mode/watch mode     | STOP     | 0 1 0 1 0 0 1 1 0 1 |          |        | 1/1              |

Note: Only after a transition from subactive mode.

**Table 41    Opcode Map**

| R9<br>H | R8<br>L | 0          |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|---------|---------|------------|------|------|-------|----------|---|-----|---|----------|---|---|-----|---------|---|---|-----|
|         |         | 0          | 1    | 2    | 3     | 4        | 5 | 6   | 7 | 8        | 9 | A | B   | C       | D | E | F   |
| 0       | 0       | NOP        | XSPX | XSPY | XSPXY | ANEM     |   |     |   | AM       |   |   |     | ORM     |   |   |     |
|         | 1       | RTN        | RTNI |      |       | ALEM     |   |     |   | AMC      |   |   |     | EORM    |   |   |     |
|         | 2       | INEM i(4)  |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | 3       | ILEM i(4)  |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | 4       | LBM(XY)    |      |      |       | BNEM     |   |     |   | LAB      |   |   |     | IB      |   |   |     |
|         | 5       | LMAIY(X)   |      |      |       | AYY      |   |     |   | LASPY    |   |   |     | IY      |   |   |     |
|         | 6       | NEGA       |      |      |       | RED      |   |     |   | LASPX    |   |   |     |         |   |   | TC  |
|         | 7       | YNEI i(4)  |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | 8       | XMA(XY)    |      |      |       | SEM n(2) |   |     |   | REM n(2) |   |   |     | TM n(2) |   |   |     |
|         | 9       | LAM(XY)    |      |      |       | LMA(XY)  |   |     |   | SMC      |   |   |     | ANM     |   |   |     |
|         | A       | ROTR       | ROTL |      |       |          |   | DAA |   |          |   |   | DAS |         |   |   | LAY |
|         | B       | TBR p(4)   |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | C       | XMB(XY)    |      |      |       | BLEM     |   |     |   | LBA      |   |   |     |         |   |   | DB  |
|         | D       | LMADY(X)   |      |      |       | SYI      |   |     |   | LYA      |   |   |     |         |   |   | DY  |
|         | E       | TD         |      |      |       | SED      |   |     |   | LXA      |   |   |     | REC     |   |   | SEC |
|         | F       | LWI i(2)   |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
| 1       | 0       | LBI i(4)   |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | 1       | LYI i(4)   |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | 2       | LXI i(4)   |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | 3       | LAI i(4)   |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | 4       | LBR m(4)   |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | 5       | LAR m(4)   |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | 6       | REDD m(4)  |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | 7       | LAMR m(4)  |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | 8       | AI i(4)    |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | 9       | LMIIY i(4) |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | A       | TDD m(4)   |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | B       | ALEI i(4)  |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | C       | LRB m(4)   |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | D       | LRA m(4)   |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | E       | SEDD m(4)  |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |
|         | F       | XMRA m(4)  |      |      |       |          |   |     |   |          |   |   |     |         |   |   |     |



1-word/2-cycle instruction



1-word/3-cycle instruction



RAM direct address instruction  
(2-word/2-cycle)



2-word/2-cycle instruction

Table 41 Opcode Map (cont)

| R9 | R8 | 1          |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|----|----|------------|---|---|---|-------|---|---|---|-----------|---|---|---|-----------|------|---|----------|
|    |    | 0          | 1 | 2 | 3 | 4     | 5 | 6 | 7 | 8         | 9 | A | B | C         | D    | E | F        |
| 0  | 0  | LAW        |   |   |   | ANEMD |   |   |   | AMD       |   |   |   | ORMD      |      |   |          |
|    | 1  | LWA        |   |   |   | ALEMD |   |   |   | AMCD      |   |   |   | EORMD     |      |   |          |
|    | 2  | INEMD i(4) |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | 3  | ILEMD i(4) |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | 4  | COMB       |   |   |   | OR    |   |   |   | STS       |   |   |   | SBY       | STOP |   |          |
|    | 5  | JEMPL p(4) |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | 6  | CALL p(4)  |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | 7  | BRL p(4)   |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | 8  | XMAD       |   |   |   |       |   |   |   | SEMD n(2) |   |   |   | REMD n(2) |      |   | TMD n(2) |
|    | 9  | LAMD       |   |   |   | LMAD  |   |   |   | SMCD      |   |   |   | ANMD      |      |   |          |
|    | A  | LMID i(4)  |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | B  | P p(4)     |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | C  | CAL a(6)   |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | D  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | E  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | F  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
| 1  | 0  | BR b(8)    |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | 1  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | 2  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | 3  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | 4  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | 5  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | 6  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | 7  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | 8  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | 9  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | A  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | B  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | C  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | D  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | E  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |
|    | F  |            |   |   |   |       |   |   |   |           |   |   |   |           |      |   |          |

1-word/2-cycle instruction

1-word/3-cycle instruction

RAM direct address instruction (2-word/2-cycle)

2-word/2-cycle instruction

## Absolute Maximum Ratings

| Item                               | Symbol      | Value                | Unit | Notes |
|------------------------------------|-------------|----------------------|------|-------|
| Power supply voltage               | $V_{CC}$    | -0.3 to +7.0         | V    |       |
| Programming voltage                | $V_{PP}$    | -0.3 to +14.0        | V    | 1     |
| Pin voltage                        | $V_T$       | -0.3 to $V_{CC}+0.3$ | V    |       |
| Allowable input current (total)    | $\sum I_o$  | 100                  | mA   | 2     |
| Allowable output current (total)   | $-\sum I_o$ | 50                   | mA   | 3     |
| Allowable input current (per pin)  | $I_o$       | 4                    | mA   | 4,5   |
|                                    |             | 30                   | mA   | 4,6   |
| Allowable output current (per pin) | $-I_o$      | 4                    | mA   | 7,8   |
|                                    |             | 20                   | mA   | 7,9   |
| Operating temperature              | Topr        | -20 to +75           | °C   | 10    |
| Storage temperature                | Tstg        | -55 to +125          | °C   | 11    |

Notes: Permanent damage may occur if these maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Applies to the HD4074889, HD4074899, and HD4074869 TEST ( $V_{PP}$ ) pin.
2. The allowable input current (total) is the sum of all currents flowing from I/O pins to ground at the same time.
3. The allowable output current (total) is the sum of all currents flowing from  $V_{CC}$  to I/O pins.
4. The allowable input current (per pin) is the maximum current allowed to flow from any one I/O pin to ground.
5. Applies to pins  $D_0$  to  $D_3$  and R0 to R8.
6. Applies to pins  $D_4$  to  $D_{11}$ .
7. The allowable output current (per pin) is the maximum current allowed to flow from  $V_{CC}$  to any one I/O pin.
8. Applies to pins  $D_4$  to  $D_{11}$  and R0 to R8.
9. Applies to pins  $D_0$  to  $D_3$ .
10. The operating temperature indicates the temperature range in which power can be supplied to the LSI (voltage  $V_{CC}$  shown in the electrical characteristics tables can be applied).
11. In the case of chips, the storage specification differs from that of the package products. Please consult your Hitachi sales representative for details.

# Electrical Characteristics

DC Characteristics (HD404888, HD4048812, HD404889, HD404898, HD4048912, HD404899, HD404874, HD404878, HD404864, HD404868:  $V_{CC}=1.8V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-20^{\circ}C$  to  $+75^{\circ}C$ ; HCD404889, HCD404899, HCD404878:  $V_{CC}=1.8V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=+75^{\circ}C$ ; HD4074889, HD4074899, HD4074869:  $V_{CC}=2.0V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-20^{\circ}C$  to  $+75^{\circ}C$ , unless otherwise specified)

| Item                               | Symbol     | Pins                                                                                                                                                    | min.         | typ. | max.         | Unit    | Test conditions                             | Notes |
|------------------------------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------|--------------|---------|---------------------------------------------|-------|
| Input high voltage                 | $V_{IH}$   | $\overline{RESET}, \overline{SCK}, SI, \overline{INT_0}, \overline{INT_1}, \overline{WU_0}$ to $\overline{WU_3}, EVNB, EVND$                            | $0.90V_{CC}$ | —    | $V_{CC}+0.3$ | V       |                                             |       |
|                                    |            | $OSC_1$                                                                                                                                                 | $V_{CC}-0.3$ | —    | $V_{CC}+0.3$ | V       | External clock operation                    |       |
| Input low voltage                  | $V_{IL}$   | $\overline{RESET}, \overline{SCK}, SI, \overline{INT_0}, \overline{INT_1}, \overline{WU_0}$ to $\overline{WU_3}, EVNB, EVND$                            | -0.3         | —    | $0.10V_{CC}$ | V       |                                             |       |
|                                    |            | $OSC_1$                                                                                                                                                 | -0.3         | —    | 0.3          | V       | External clock operation                    |       |
| Output high voltage                | $V_{OH}$   | $\overline{SCK}, SO, BUZZ, TOB, TOC$                                                                                                                    | $V_{CC}-0.5$ | —    | —            | V       | $-I_{OH}=0.3mA$                             |       |
| Output low voltage                 | $V_{OL}$   | $\overline{SCK}, SO, BUZZ, TOB, TOC$                                                                                                                    | —            | —    | 0.4          | V       | $I_{OL}=0.4mA$                              |       |
| I/O leakage current                | $ I_{IL} $ | $\overline{RESET}, \overline{SCK}, SI, \overline{INT_0}, \overline{INT_1}, \overline{WU_0}$ to $\overline{WU_3}, EVNB, EVND, OSC_1, TOB, TOC, SO, BUZZ$ | —            | —    | 1            | $\mu A$ | $V_{in}=0V$ to $V_{CC}$                     | 1     |
| Active mode current dissipation    | $I_{CC1}$  | $V_{CC}$                                                                                                                                                | —            | 3.0  | 5.0          | mA      | $V_{CC}=5V, f_{OSC}=4MHz$                   | 2     |
|                                    | $I_{CC2}$  |                                                                                                                                                         | —            | 0.4  | 1.0          | mA      | $V_{CC}=3V, f_{OSC}=800kHz$                 | 2     |
| Standby mode current dissipation   | $I_{SBY1}$ | $V_{CC}$                                                                                                                                                | —            | 1.0  | 2.0          | mA      | $V_{CC}=5V, f_{OSC}=4MHz, LCD$ on           | 3     |
|                                    | $I_{SBY2}$ |                                                                                                                                                         | —            | 0.3  | 0.6          | mA      | $V_{CC}=3V, f_{OSC}=800kHz$ LCD on          | 3     |
| Subactive mode current dissipation | $I_{SUB}$  | $V_{CC}$ (HD404888, HD4048812, HD404889, HCD404889, HD404898, HD4048912, HD404899, HCD404899, HD404874, HD404878, HCD404878, HD404864, HD404868)        | —            | 35   | 60           | $\mu A$ | $V_{CC}=3V, LCD$ on, 32 kHz oscillator used | 4,5   |
|                                    |            | $V_{CC}$ (HD4074889, HD4074899, HD4074869)                                                                                                              | —            | 70   | 120          | $\mu A$ |                                             | 4,5   |

| Item                           | Symbol     | Pins     | min. | typ. | max. | Unit    | Test Conditions                                  | Notes |
|--------------------------------|------------|----------|------|------|------|---------|--------------------------------------------------|-------|
| Watch mode current dissipation | $I_{WTC1}$ | $V_{CC}$ | —    | 15   | 30   | $\mu A$ | $V_{CC} = 3 V$ , LCD on, 32 kHz oscillator used  | 4,5   |
|                                | $I_{WTC2}$ | $V_{CC}$ | —    | 5    | 8    | $\mu A$ | $V_{CC} = 3 V$ , LCD off, 32 kHz oscillator used | 5     |
| Stop mode current dissipation  | $I_{STOP}$ | $V_{CC}$ | —    | —    | 5    | $\mu A$ | $V_{CC} = 3 V$ , no 32 kHz oscillator            | 5     |
| Stop mode retention voltage    | $V_{STOP}$ | $V_{CC}$ | 1.5  | —    | —    | V       | no 32 kHz oscillator                             | 6     |

- Notes:
1. Excludes output buffer current.
  2. Power supply current when the MCU is in the reset state and there are no I/O currents.

|                 |            |                                                                                                  |
|-----------------|------------|--------------------------------------------------------------------------------------------------|
| Test Conditions | MCU State  | <ul style="list-style-type: none"> <li>Reset state</li> </ul>                                    |
|                 | Pin States | <ul style="list-style-type: none"> <li><math>\overline{RESET}</math>, TEST: At ground</li> </ul> |

3. Power supply current when the on-chip timers are operating and there are no I/O currents.

|                 |            |                                                                                                                                                                                                                                                 |
|-----------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Test Conditions | MCU State  | <ul style="list-style-type: none"> <li>I/O: Same as reset state</li> <li>Standby mode</li> <li><math>f_{cyc} = f_{OSC}/4</math></li> </ul>                                                                                                      |
|                 | Pin States | <ul style="list-style-type: none"> <li><math>\overline{RESET}</math>: At <math>V_{CC}</math></li> <li>TEST: At ground</li> <li><math>D_0</math> to <math>D_{11}</math>, <math>R_0</math> to <math>R_8</math>: At <math>V_{CC}</math></li> </ul> |

4. Applies when the LCD power supply dividing resistor is connected.
5. Power supply current when there are no I/O currents.

|                 |            |                                                                                                                                                                                                                                                 |
|-----------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Test Conditions | Pin States | <ul style="list-style-type: none"> <li><math>\overline{RESET}</math>: At <math>V_{CC}</math></li> <li>TEST: At ground</li> <li><math>D_0</math> to <math>D_{11}</math>, <math>R_0</math> to <math>R_8</math>: At <math>V_{CC}</math></li> </ul> |
|-----------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

6. Voltage needed to retain RAM data.

**HD404889/HD404899/HD404878/HD404868 Series**

I/O Characteristics for Standard Pins (HD404888, HD4048812, HD404889, HD404898, HD4048912, HD404899, HD404874, HD404878, HD404864, HD404868:  $V_{CC}=1.8V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-20^{\circ}C$  to  $+75^{\circ}C$ ; HCD404889, HCD404899, HCD404878:  $V_{CC} =1.8V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=+75^{\circ}C$ ; HD4074889, HD4074899, HD4074869:  $V_{CC}=2.0V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-20^{\circ}C$  to  $+75^{\circ}C$ , unless otherwise specified)

| Item                | Symbol     | Pins     | min.         | typ. | max.         | Unit    | Test conditions           | Notes |
|---------------------|------------|----------|--------------|------|--------------|---------|---------------------------|-------|
| Input high voltage  | $V_{IH}$   | R0 to R8 | $0.7V_{CC}$  | —    | $V_{CC}+0.3$ | V       |                           | 1     |
|                     |            | R0 to R7 |              |      |              |         |                           | 2     |
| Input low voltage   | $V_{IL}$   | R0 to R8 | $-0.3$       | —    | $0.3V_{CC}$  | V       |                           | 1     |
|                     |            | R0 to R7 |              |      |              |         |                           | 2     |
| Output high voltage | $V_{OH}$   | R0 to R8 | $V_{CC}-0.5$ | —    | —            | V       | $-I_{OH}=0.3mA$           | 1     |
|                     |            | R0 to R7 |              |      |              |         |                           | 2     |
| Output low voltage  | $V_{OL}$   | R0 to R8 | —            | —    | 0.4          | V       | $I_{OL}=0.4mA$            | 1     |
|                     |            | R0 to R7 |              |      |              |         |                           | 2     |
| I/O leakage current | $ I_{IL} $ | R0 to R8 | —            | —    | 1            | $\mu A$ | $V_{IN}=0V$ to $V_{CC}$   | 1, 3  |
|                     |            | R0 to R7 |              |      |              |         |                           | 2, 3  |
| MOS pull-up current | $-I_{PU}$  | R0 to R8 | 10           | 50   | 150          | $\mu A$ | $V_{CC}=3V$ , $V_{IN}=0V$ | 1     |
|                     |            | R0 to R7 |              |      |              |         |                           | 2     |

- Notes: 1. Applies to the HD404889, HD404899, and HD404878 Series.  
2. Applies to the HD404868 Series.  
3. Excludes the current flowing in the output buffer.

# HD404889/HD404899/HD404878/HD404868 Series

**I/O Characteristics for High-Current Pins (HD404888, HD4048812, HD404889, HD404898, HD4048912, HD404899, HD404874, HD404878, HD404864, HD404868:  $V_{CC}=1.8V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-20^{\circ}C$  to  $+75^{\circ}C$ ; HCD404889, HCD404899, HCD404878:  $V_{CC}=1.8V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=+75^{\circ}C$ ; HD4074889, HD4074899, HD4074869:  $V_{CC}=2.0V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-20^{\circ}C$  to  $+75^{\circ}C$ , unless otherwise specified)**

| Item                | Symbol     | Pins              | min.         | typ. | max.         | Unit    | Test conditions                            | Notes |
|---------------------|------------|-------------------|--------------|------|--------------|---------|--------------------------------------------|-------|
| Input high voltage  | $V_{IH}$   | $D_0$ to $D_{11}$ | $0.7V_{CC}$  | —    | $V_{CC}+0.3$ | V       |                                            | 1     |
|                     |            | $D_0$ to $D_9$    |              |      |              |         |                                            | 2     |
| Input low voltage   | $V_{IL}$   | $D_0$ to $D_{11}$ | $-0.3$       | —    | $0.3V_{CC}$  | V       |                                            | 1     |
|                     |            | $D_0$ to $D_9$    |              |      |              |         |                                            | 2     |
| Output high voltage | $V_{OH}$   | $D_4$ to $D_{11}$ | $V_{CC}-0.5$ | —    | —            | V       | $-I_{OH}=0.3mA$                            | 1     |
|                     |            | $D_4$ to $D_9$    |              |      |              |         |                                            | 2     |
|                     |            | $D_0$ to $D_3$    | $V_{CC}-2.0$ | —    | —            | V       | $-I_{OH}=10mA$ ,<br>$V_{CC}=4.5$ to $5.5V$ |       |
| Output low voltage  | $V_{OL}$   | $D_0$ to $D_3$    | —            | —    | 0.4          | V       | $I_{OL}=0.4mA$                             |       |
|                     |            | $D_4$ to $D_{11}$ | —            | —    | 2.0          | V       | $I_{OL}=15mA$                              | 1     |
|                     |            | $D_4$ to $D_9$    |              |      |              |         | $V_{CC}=4.5V$ to $5.5V$                    | 2     |
| I/O leakage current | $ I_{IL} $ | $D_0$ to $D_{11}$ | —            | —    | 1            | $\mu A$ | $V_{IN}=0V$ to $V_{CC}$                    | 1, 3  |
|                     |            | $D_0$ to $D_9$    |              |      |              |         |                                            | 2, 3  |
| MOS pull-up current | $-I_{PU}$  | $D_0$ to $D_{11}$ | 10           | 50   | 150          | $\mu A$ | $V_{CC}=3V$ , $V_{IN}=0V$                  | 1     |
|                     |            | $D_0$ to $D_9$    |              |      |              |         |                                            | 2     |

Notes: 1. Applies to the HD404889, HD404899, and HD404878 Series.

2. Applies to the HD404868 Series.

3. Excludes the current flowing in the output buffer.

HD404889/HD404899/HD404878/HD404868 Series

LCD Circuit Characteristics (HD404888, HD4048812, HD404889, HD404898, HD4048912, HD404899, HD404874, HD404878, HD404864, HD404868:  $V_{CC}=1.8V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-20^{\circ}C$  to  $+75^{\circ}C$ ; HCD404889, HCD404899, HCD404878:  $V_{CC}=1.8V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=+75^{\circ}C$ ; HD4074889, HD4074899, HD4074869:  $V_{CC}=2.0V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-20^{\circ}C$  to  $+75^{\circ}C$ , unless otherwise specified)

| Item                                 | Symbol    | Pins          | min. | typ. | max.     | Unit       | Test conditions                     | Notes |
|--------------------------------------|-----------|---------------|------|------|----------|------------|-------------------------------------|-------|
| Segment driver voltage drop          | $V_{DS}$  | SEG1 to SEG32 | —    | —    | 0.6      | V          | $I_d=3\mu A$<br>$V_1=2.7$ to $5.5V$ | 1, 2  |
|                                      |           | SEG1 to SEG24 |      |      |          |            |                                     | 1, 3  |
| Common driver voltage drop           | $V_{DC}$  | COM1 to COM4  | —    | —    | 0.3      | V          | $I_d=3\mu A$<br>$V_1=2.7$ to $5.5V$ | 1     |
| LCD power supply dividing resistance | $R_W$     |               | 50   | 300  | 900      | k $\Omega$ | $V_1-GND$                           |       |
| LCD voltage                          | $V_{LCD}$ | $V_1$         | 2.2  | —    | $V_{CC}$ | V          |                                     | 4, 5  |

- Notes:
1. The voltage drop from power supply pins  $V_1$ ,  $V_2$ ,  $V_3$ , and  $GND$  to each segment pin or each common pin.
  2. Applies to the HD404889, HD404899, and HD404878 Series.
  3. Applies to the HD404868 Series.
  4. In the HD404889, HD404899, and HD404878 Series, when  $V_{LCD}$  is supplied by the internal power supply,  $V_0$  and  $V_1$  should be shorted. When  $V_{LCD}$  is supplied by an external power supply, the relationship  $V_{CC} \geq V_{LCD} \geq 2.2V$  should be maintained. In this case, the  $V_0$  pin should be fixed at  $V_{CC}$ .
  5. In the HD404868 Series, when  $V_{LCD}$  is supplied by an external power supply, the relationship  $V_{CC} \geq V_{LCD} \geq 2.2V$  should be maintained.

## HD404889/HD404899/HD404878/HD404868 Series

**A/D Converter Characteristics (HD404888, HD4048812, HD404889:  $V_{CC}=1.8V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-20^{\circ}C$  to  $+75^{\circ}C$ ; HCD404889:  $V_{CC}=1.8V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=+75^{\circ}C$ ; HD4074889:  $V_{CC}=2.0V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-20^{\circ}C$  to  $+75^{\circ}C$ , unless otherwise specified)**

| Item                        | Symbol    | Pins             | min.         | typ.     | max.         | Unit      | Test conditions                 | Notes |
|-----------------------------|-----------|------------------|--------------|----------|--------------|-----------|---------------------------------|-------|
| Analog power supply voltage | $AV_{CC}$ | $AV_{CC}$        | $V_{CC}-0.3$ | $V_{CC}$ | $V_{CC}+0.3$ | V         |                                 | 1     |
| Analog input voltage        | $AV_{in}$ | $AN_0$ to $AN_5$ | $AV_{SS}$    | —        | $AV_{CC}$    | V         |                                 |       |
| $AV_{CC}-AV_{SS}$ current   | $I_{AD}$  |                  | —            | —        | 500          | $\mu A$   | $V_{CC}=AV_{CC}=5.0V$           |       |
| Analog input capacitance    | $CA_{in}$ | $AN_0$ to $AN_5$ | —            | 15       | —            | pF        |                                 |       |
| Resolution                  |           |                  | —            | 8        | —            | bit       |                                 |       |
| Number of inputs            |           |                  | 0            | —        | 6            | channel   |                                 |       |
| Absolute accuracy           |           |                  | —            | —        | $\pm 2.0$    | LSB       | $V_{CC}=AV_{CC}=2.7V$ to $5.5V$ |       |
|                             |           |                  | —            | —        | $\pm 3.0$    | LSB       | $V_{CC}=AV_{CC}=1.8V$ to $2.7V$ | 2     |
| Conversion time             |           |                  | 65           | —        | 125          | $t_{cyc}$ |                                 |       |
| Input impedance             |           | $AN_0$ to $AN_5$ | 1            | —        | —            | $M\Omega$ |                                 |       |

- Notes: 1. Connect to the  $V_{CC}$  pin when the A/D converter is not used. The  $AV_{CC}$  setting ranges are  $1.8V \leq AV_{CC} \leq 5.5V$  (HD404888, HD4048812, HD404889, HCD404889) and  $2.0V \leq AV_{CC} \leq 5.5V$  (HD4074889)
2. The conversion time is  $125t_{cyc}$ .

# HD404889/HD404899/HD404878/HD404868 Series

(HD404898, HD4048912, HD404899:  $V_{CC}=1.8V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-20^{\circ}C$  to  $+75^{\circ}C$ ;

HCD404899:  $V_{CC}=1.8V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=+75^{\circ}C$ ;

HD4074899:  $V_{CC}=2.0V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-20^{\circ}C$  to  $+75^{\circ}C$ , unless otherwise specified)

| Item                          | Symbol    | Pins             | min.         | typ.     | max.         | Unit      | Test conditions                           | Notes |
|-------------------------------|-----------|------------------|--------------|----------|--------------|-----------|-------------------------------------------|-------|
| Analog power supply voltage   | $AV_{CC}$ | $AV_{CC}$        | $V_{CC}-0.3$ | $V_{CC}$ | $V_{CC}+0.3$ | V         |                                           | 1     |
| Analog input voltage          | $AV_{in}$ | $AN_0$ to $AN_5$ | $AV_{SS}$    | —        | $AV_{CC}$    | V         |                                           |       |
| $AV_{CC}$ - $AV_{SS}$ current | $I_{AD}$  |                  | —            | —        | 500          | $\mu A$   | $V_{CC}=AV_{CC}=5.0V$                     |       |
| Analog input capacitance      | $CA_{in}$ | $AN_0$ to $AN_5$ | —            | 15       | —            | pF        |                                           |       |
| Resolution                    |           |                  | —            | 10       | —            | bit       |                                           |       |
| Number of inputs              |           |                  | 0            | —        | 6            | channel   |                                           |       |
| Conversion time               |           |                  | 125          | —        | —            | $t_{cyc}$ | $V_{CC}=AV_{CC}=1.8V$ to less than $2.0V$ | 2     |
|                               |           |                  | 65           | —        | 125          | $t_{cyc}$ | $V_{CC}=AV_{CC}=2.0V$ to $5.5V$           |       |
| Absolute accuracy             |           |                  | —            | —        | $\pm 4.0$    | LSB       |                                           |       |
| Input impedance               |           | $AN_0$ to $AN_5$ | 1            | —        | —            | $M\Omega$ |                                           |       |

- Notes: 1. Connect to the  $V_{CC}$  pin when the A/D converter is not used. The  $AV_{CC}$  setting ranges are  $1.8V \leq AV_{CC} \leq 5.5V$  (HD404898, HD4048912, HD404899, HCD404899) and  $2.0V \leq AV_{CC} \leq 5.5V$  (HD4074899)
2. Applies to HD404898, HD4048912, HD404899, and HCD404899.

(HD404864, HD404868:  $V_{CC}=1.8V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-20^{\circ}C$  to  $+75^{\circ}C$ ; HD4074869:  $V_{CC}=2.0V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-20^{\circ}C$  to  $+75^{\circ}C$ )

| Item                     | Symbol    | Pins             | min.  | typ. | max.      | Unit      | Test conditions                   | Notes |
|--------------------------|-----------|------------------|-------|------|-----------|-----------|-----------------------------------|-------|
| Analog input voltage     | $AV_{in}$ | $AN_0$ to $AN_3$ | $GND$ | —    | $V_{CC}$  | V         |                                   |       |
| Analog input capacitance | $CA_{in}$ | $AN_0$ to $AN_3$ | —     | 15   | —         | pF        |                                   |       |
| Resolution               |           |                  | —     | 10   | —         | bit       |                                   |       |
| Number of inputs         |           |                  | 0     | —    | 4         | channel   |                                   |       |
| Absolute accuracy        |           |                  | —     | —    | $\pm 4.0$ | LSB       |                                   |       |
| Conversion time          |           |                  | 125   | —    | —         | $t_{cyc}$ | $V_{CC}=1.8V$ to less than $2.0V$ | 1     |
|                          |           |                  | 65    | —    | 125       | $t_{cyc}$ | $V_{CC}=2.0V$ to $5.5V$           |       |
| Input impedance          |           | $AN_0$ to $AN_3$ | 1     | —    | —         | $M\Omega$ |                                   |       |

- Note: 1. Applies to HD404864 and HD404868.

# HD404889/HD404899/HD404878/HD404868 Series

**AC Characteristics (HD404888, HD4048812, HD404889, HD404898, HD4048912, HD404899, HD404874, HD404878, HD404864, HD404868:  $V_{CC}=1.8V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-20^{\circ}C$  to  $+75^{\circ}C$ ;, HCD404889, HCD404899, HCD404878:  $V_{CC}=1.8V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=+75^{\circ}C$ ; HD4074889, HD4074899, HD4074869:  $V_{CC}=2.0V$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-20^{\circ}C$  to  $+75^{\circ}C$ , unless otherwise specified)**

| Item                                                                                                         | Symbol       | Pins                                                                                                                                            | min. | typ.   | max. | Unit                 | Test conditions                       | Notes |
|--------------------------------------------------------------------------------------------------------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------|------|--------|------|----------------------|---------------------------------------|-------|
| Clock oscillation frequency                                                                                  | $f_{OSC}$    | OSC <sub>1</sub> , OSC <sub>2</sub>                                                                                                             | 0.4  | —      | 4.5  | MHz                  | Division by 4                         | 1     |
|                                                                                                              |              | X1,X2                                                                                                                                           | —    | 32.768 | —    | kHz                  |                                       |       |
| Instruction cycle time                                                                                       | $t_{cyc}$    |                                                                                                                                                 | 0.89 | —      | 10   | $\mu s$              | Division by 4                         |       |
|                                                                                                              | $t_{subcyc}$ |                                                                                                                                                 | —    | 244.14 | —    | $\mu s$              | 32 kHz oscillator used, division by 8 |       |
|                                                                                                              |              |                                                                                                                                                 | —    | 122.07 | —    | $\mu s$              | 32 kHz oscillator used, division by 4 |       |
| Oscillation settling time(external clock and ceramic oscillator)                                             | $t_{RC}$     | OSC <sub>1</sub> , OSC <sub>2</sub>                                                                                                             | —    | —      | 7.5  | ms                   |                                       | 2     |
| Oscillation settling time(crystal oscillator)                                                                | $t_{RC}$     | OSC <sub>1</sub> , OSC <sub>2</sub>                                                                                                             | —    | —      | 30   | ms                   | $V_{CC}=2.0$ to $5.5V$                | 2     |
|                                                                                                              |              | X1,X2                                                                                                                                           | —    | —      | 2    | s                    | $T_a=-10$ to $+60^{\circ}C$           | 2     |
| External clock high-level width                                                                              | $t_{CPH}$    | OSC <sub>1</sub>                                                                                                                                | 105  | —      | —    | ns                   | $f_{OSC}=4MHz$                        | 3     |
| External clock low-level width                                                                               | $t_{CPL}$    | OSC <sub>1</sub>                                                                                                                                | 105  | —      | —    | ns                   | $f_{OSC}=4MHz$                        | 3     |
| External clock rise time                                                                                     | $t_{CPr}$    | OSC <sub>1</sub>                                                                                                                                | —    | —      | 20   | ns                   | $f_{OSC}=4MHz$                        | 3     |
| External clock fall time                                                                                     | $t_{CPf}$    | OSC <sub>1</sub>                                                                                                                                | —    | —      | 20   | ns                   | $f_{OSC}=4MHz$                        | 3     |
| $\overline{INT}_0$ to INT <sub>1</sub> , EVNB, EVND, $\overline{WU}_0$ to $\overline{WU}_3$ high-level width | $t_{IH}$     | $\overline{INT}_0$ to INT <sub>1</sub> , EVNB, EVND, $\overline{WU}_0$ to $\overline{WU}_3$                                                     | 2    | —      | —    | $t_{cyc}/t_{subcyc}$ |                                       | 4     |
| $\overline{INT}_0$ to INT <sub>1</sub> , EVNB, EVND, $\overline{WU}_0$ to $\overline{WU}_3$ low-level width  | $t_{IL}$     | $\overline{INT}_0$ to INT <sub>1</sub> , EVNB, EVND, $\overline{WU}_0$ to $\overline{WU}_3$                                                     | 2    | —      | —    | $t_{cyc}/t_{subcyc}$ |                                       | 4     |
| $\overline{RESET}$ low-level width                                                                           | $t_{RSTL}$   | $\overline{RESET}$                                                                                                                              | 2    | —      | —    | $t_{cyc}$            |                                       | 5     |
| $\overline{RESET}$ rise time                                                                                 | $t_{RSTr}$   | $\overline{RESET}$                                                                                                                              | —    | —      | 20   | ms                   |                                       | 5     |
| Input capacitance                                                                                            | $C_{in}$     | All input pins except TEST                                                                                                                      | —    | —      | 15   | pF                   | $f=1MHz, V_{in}=0V$                   |       |
|                                                                                                              |              | TEST<br>(HD404888, HD4048812, HD404889, HCD404889, HD404899, HD404898, HD4048912, HCD404899, HD404874, HD404878, HCD404878, HD404864, HD404868) | —    | —      | 15   | pF                   |                                       |       |
|                                                                                                              |              | TEST<br>(HD4074889, HD4074899, HD4074869)                                                                                                       | —    | —      | 40   | pF                   |                                       |       |

# HD404889/HD404899/HD404878/HD404868 Series

- Notes:
1. When the subsystem oscillator (32.768 kHz crystal oscillation) is used, use within the range  $0.4\text{ MHz} \leq f_{\text{OSC}} \leq 1.0\text{ MHz}$  or  $1.6\text{ MHz} \leq f_{\text{OSC}} \leq 4.5\text{ MHz}$ . The SSR1 bit of the system clock select register (SSR) should be set to 0 and 1, respectively.
  2. The oscillation settling time is defined as follows:
    - (1) The time required for the oscillation to settle after  $V_{\text{CC}}$  has reached min. at power-on.
    - (2) The time required for the oscillation to settle after  $\overline{\text{RESET}}$  input has gone low when stop mode is cleared.To ensure enough time for the oscillation to settle at power-on hold the  $\overline{\text{RESET}}$  input low for at least time  $t_{\text{RC}}$ . The oscillation settling time will depend on the circuit constants and stray capacitance. The resonator should be determined in consultation with the resonator manufacturer. With regard to the system clock ( $\text{OSC}_1$ ,  $\text{OSC}_2$ ), bits MIS1 and MIS0 in the miscellaneous register (MIS) should be set according to the oscillation settling time of the resonator used.
  3. See figure 104.
  4. See figure 105.
  5. See figure 106.

**Serial Interface Timing Characteristics (HD404888, HD4048812, HD404889, HD404898, HD4048912, HD404899, HD404874, HD404878, HD404864, HD404868:  $V_{\text{CC}}=1.8\text{V}$  to  $5.5\text{V}$ ,  $\text{GND}=0\text{V}$ ,  $T_a=-20^\circ\text{C}$  to  $+75^\circ\text{C}$ ;, HCD404889, HCD404899, HCD404878:  $V_{\text{CC}}=1.8\text{V}$  to  $5.5\text{V}$ ,  $\text{GND}=0\text{V}$ ,  $T_a=+75^\circ\text{C}$ ; HD4074889, HD4074899, HD4074869:  $V_{\text{CC}}=2.0\text{V}$  to  $5.5\text{V}$ ,  $\text{GND}=0\text{V}$ ,  $T_a=-20^\circ\text{C}$  to  $+75^\circ\text{C}$ , unless otherwise specified)**

| Item                          | Symbol             | Pins                    | min. | typ. | max. | Unit              | Test conditions        | Notes |
|-------------------------------|--------------------|-------------------------|------|------|------|-------------------|------------------------|-------|
| Serial clock cycle time       | $t_{\text{Scyc}}$  | $\overline{\text{SCK}}$ | 1    | —    | —    | $t_{\text{cyc}}$  | See load in figure 108 | 1     |
| Serial clock high-level width | $t_{\text{SCKH}}$  | $\overline{\text{SCK}}$ | 0.4  | —    | —    | $t_{\text{Scyc}}$ | See load in figure 108 | 1     |
| Serial clock low-level width  | $t_{\text{SCKL}}$  | $\overline{\text{SCK}}$ | 0.4  | —    | —    | $t_{\text{Scyc}}$ | See load in figure 108 | 1     |
| Serial clock rise time        | $t_{\text{SC Kr}}$ | $\overline{\text{SCK}}$ | —    | —    | 100  | ns                | See load in figure 108 | 1     |
| Serial clock fall time        | $t_{\text{SCKf}}$  | $\overline{\text{SCK}}$ | —    | —    | 100  | ns                | See load in figure 108 | 1     |
| Serial output data delay time | $t_{\text{DSO}}$   | SO                      | —    | —    | 300  | ns                | See load in figure 108 | 1     |
| Serial input data setup time  | $t_{\text{SSI}}$   | SI                      | 200  | —    | —    | ns                |                        | 1     |
| Serial input data hold time   | $t_{\text{HSI}}$   | SI                      | 200  | —    | —    | ns                |                        | 1     |

During Serial Clock Input

| Item                          | Symbol        | Pins             | min. | typ. | max. | Unit          | Test conditions        | Notes |
|-------------------------------|---------------|------------------|------|------|------|---------------|------------------------|-------|
| Serial clock cycle time       | $t_{S_{cyc}}$ | $\overline{SCK}$ | 1    | —    | —    | $t_{cyc}$     |                        | 1     |
| Serial clock high-level width | $t_{SCKH}$    | $\overline{SCK}$ | 0.4  | —    | —    | $t_{S_{cyc}}$ |                        | 1     |
| Serial clock low-level width  | $t_{SCKL}$    | $\overline{SCK}$ | 0.4  | —    | —    | $t_{S_{cyc}}$ |                        | 1     |
| Serial clock rise time        | $t_{SC\ Kr}$  | $\overline{SCK}$ | —    | —    | 100  | ns            |                        | 1     |
| Serial clock fall time        | $t_{SCKf}$    | $\overline{SCK}$ | —    | —    | 100  | ns            |                        | 1     |
| Serial output data delay time | $t_{DSO}$     | SO               | —    | —    | 300  | ns            | See load in figure 108 | 1     |
| Serial input data setup time  | $t_{SSI}$     | SI               | 200  | —    | —    | ns            |                        | 1     |
| Serial input data hold time   | $t_{HSI}$     | SI               | 200  | —    | —    | ns            |                        | 1     |

Note: 1. See figure 107.

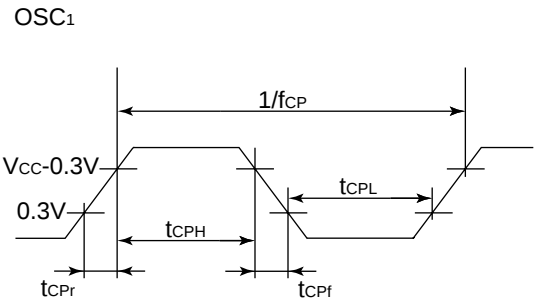


Figure 104 External Clock Input Waveform

$\overline{INT}_0$ ,  $INT_1$ ,  $EVNB$ ,  $EVND$ ,  $\overline{WU}_0$  to  $\overline{WU}_3$

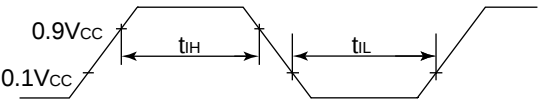


Figure 105 Interrupt Timing

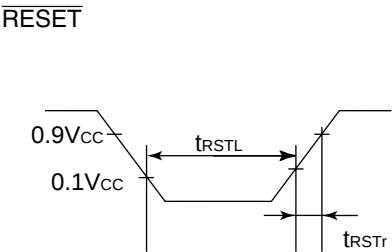
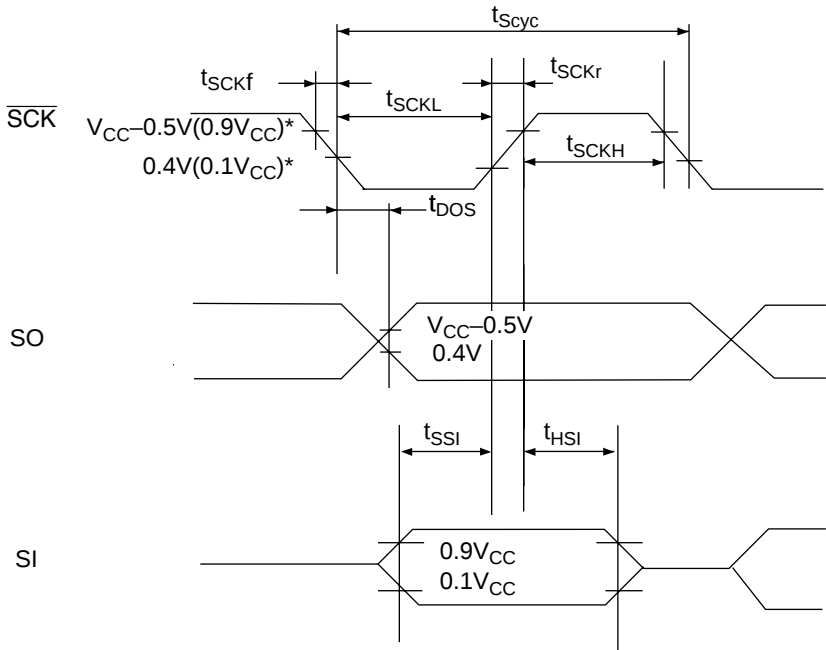
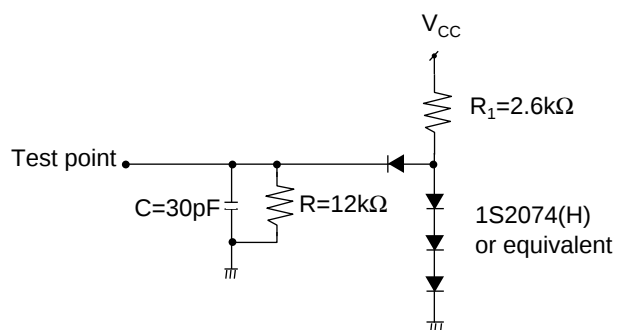


Figure 106 Reset Timing



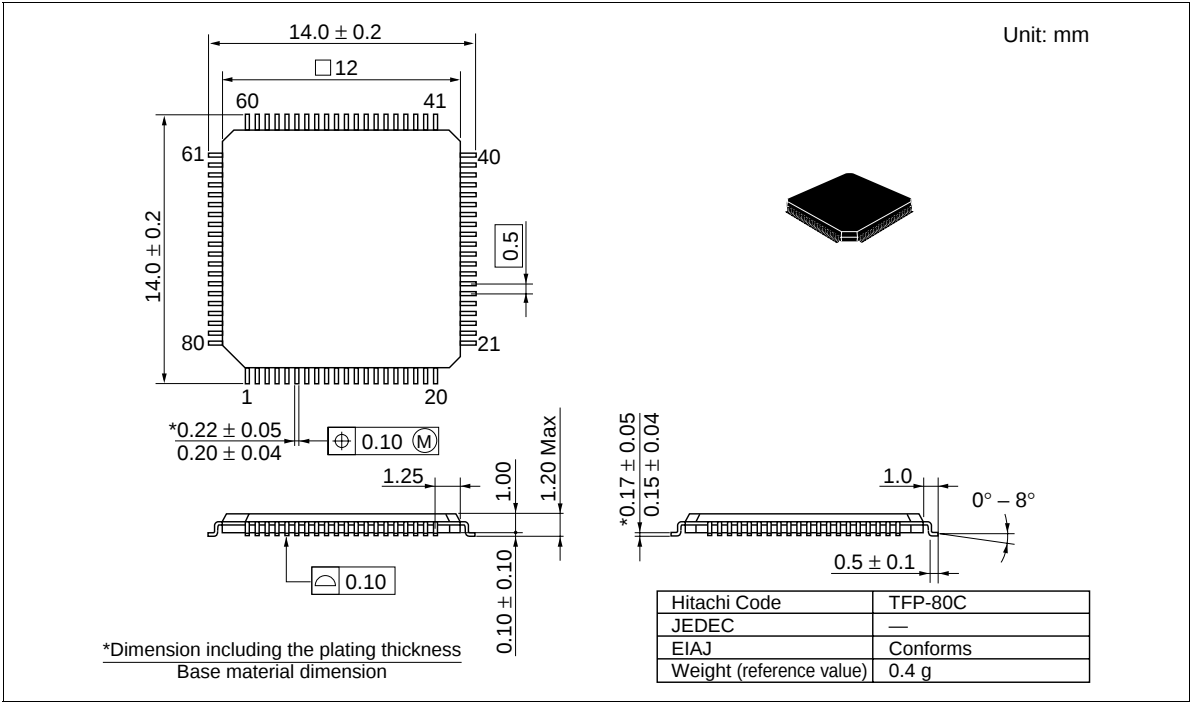
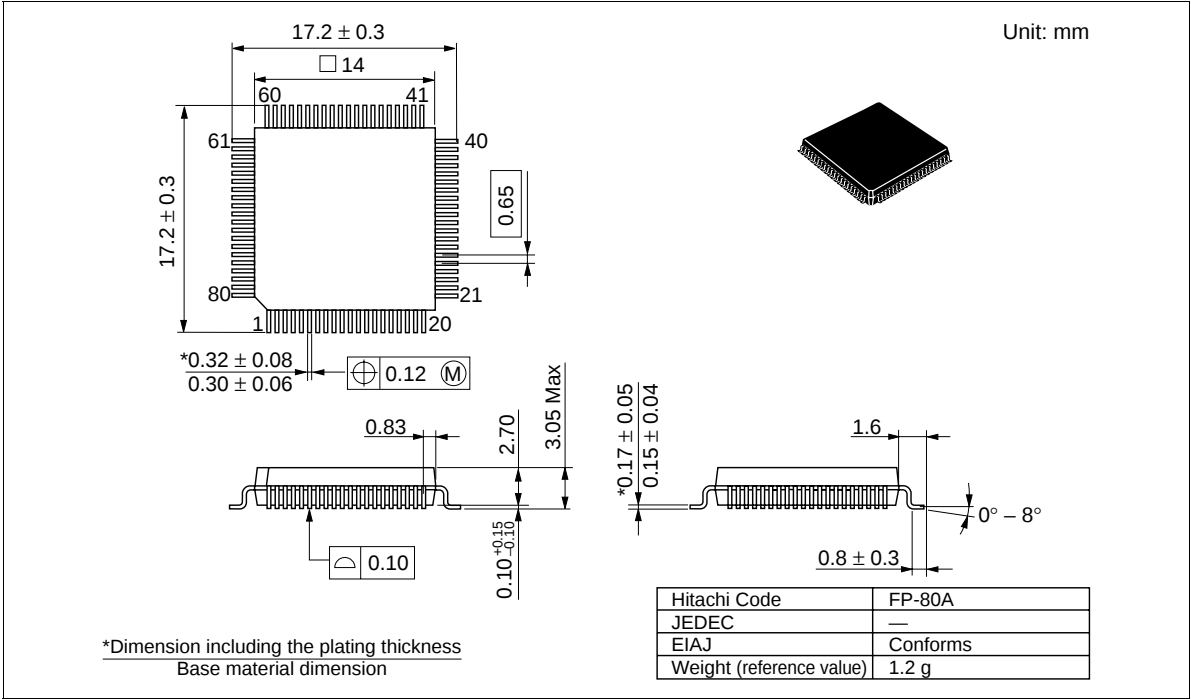
Note :  $V_{CC}-0.5V$  and  $0.4V$  are the voltages during serial clock output.  
 $0.9 V_{CC}$  and  $0.1 V_{CC}$  are the voltages during serial clock input.

Figure 107 Serial Interface Timing

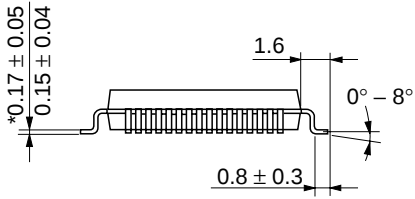
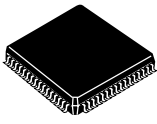
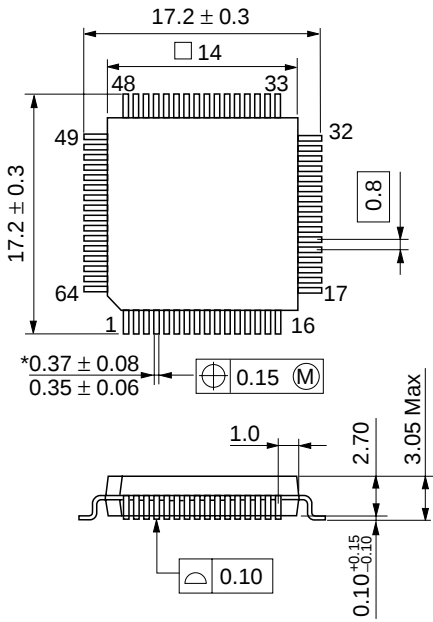


**Figure 108 Timing Load Circuit**

Package Dimensions



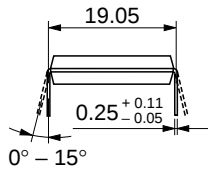
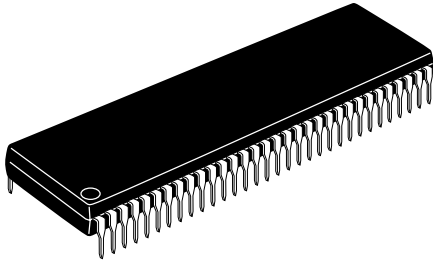
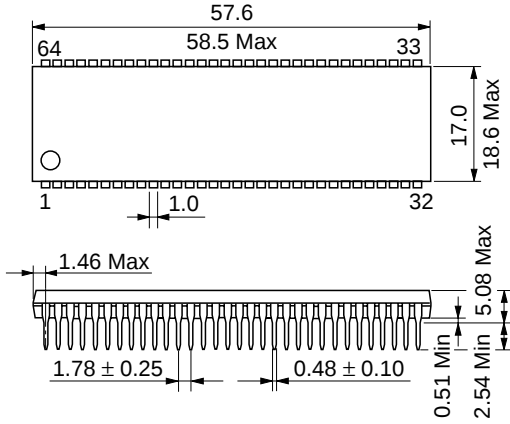
Unit: mm



|                          |          |
|--------------------------|----------|
| Hitachi Code             | FP-64A   |
| JEDEC                    | —        |
| EIAJ                     | Conforms |
| Weight (reference value) | 1.2 g    |

\*Dimension including the plating thickness  
Base material dimension

Unit: mm

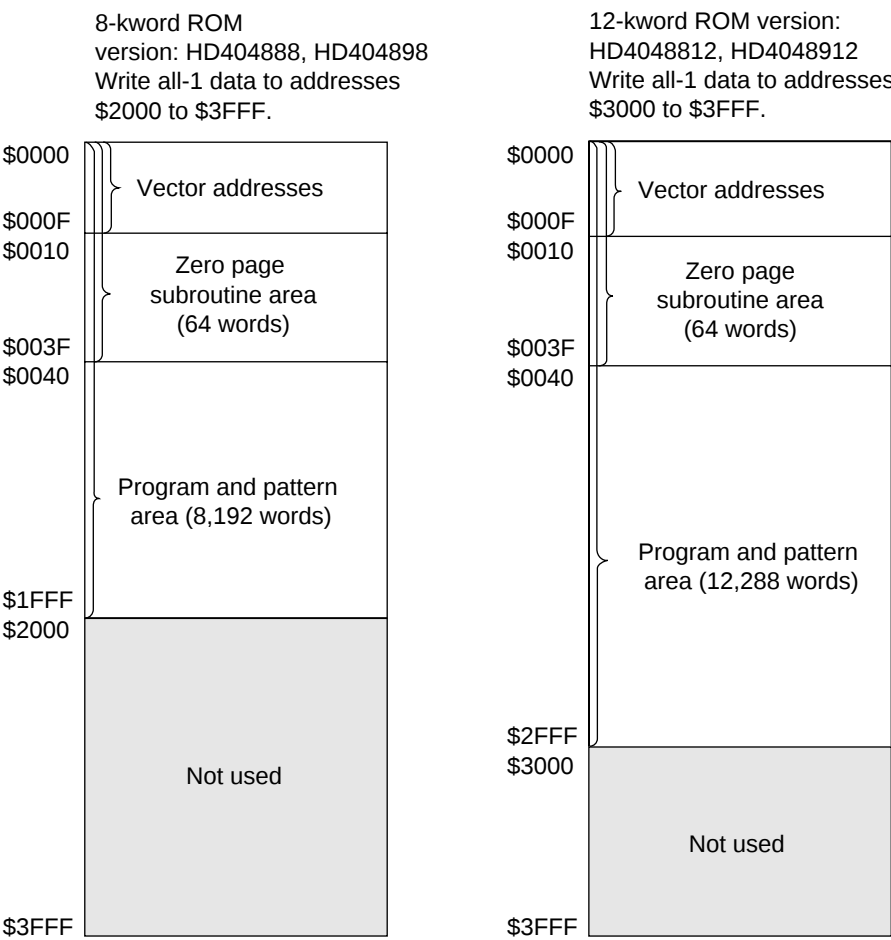


|                          |          |
|--------------------------|----------|
| Hitachi Code             | DP-64S   |
| JEDEC                    | —        |
| EIAJ                     | Conforms |
| Weight (reference value) | 8.8 g    |

Note on ROM Ordering

Please note the following when ordering HD404888, HD4048812, HD404898 or HD4048912 ROM.

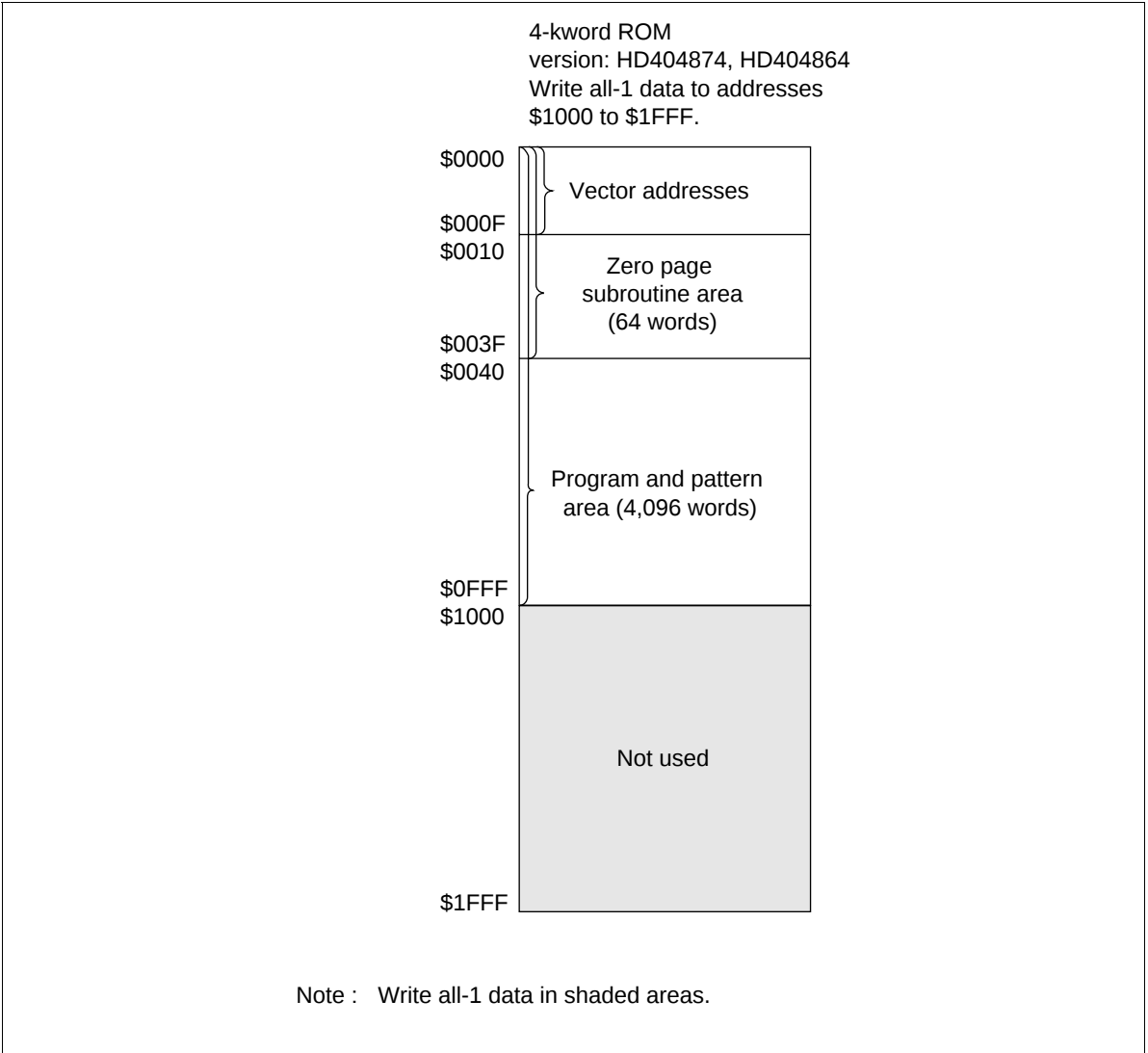
When ordering ROM, please fill the "Not used" areas below with all-1 data, to give the same amount of data as for the 16-kwords version (HD404889, HD404899). The program that converts ROM data to mask drawing data is the same as that used for the 16-kwords version, and therefore the same amount of data is necessary. This applies both to orders using EPROM and orders using data transmission.



Note on ROM Ordering

Please note the following when ordering HD404874 or HD404864 ROM.

When ordering ROM, please fill the "Not used" areas below with all-1 data, to give the same amount of data as for the 8-kwords version (HD404878, HD404868). The program that converts ROM data to mask drawing data is the same as that used for the 8-kwords version, and therefore the same amount of data is necessary. This applies both to orders using EPROM and orders using data transmission.



HD404889/HD404899/HD404878/HD404868 Series

Option List HD404888, HD4048812, HD404889, HCD404889

Please check off the appropriate applications and enter the necessary information.

|                            |      |       |     |
|----------------------------|------|-------|-----|
| Date of order              | Year | Month | Day |
| Customer                   |      |       |     |
| Department                 |      |       |     |
| Name                       |      |       |     |
| ROM code name              |      |       |     |
| LSI number (Hitachi entry) |      |       |     |

1. ROM Size

|                                    |           |
|------------------------------------|-----------|
| <input type="checkbox"/> HD404888  | 8 kwords  |
| <input type="checkbox"/> HD4048812 | 12 kwords |
| <input type="checkbox"/> HD404889  | 16 kwords |
| <input type="checkbox"/> HCD404889 | 16 kwords |

2. Function Options

|                            |                                                      |
|----------------------------|------------------------------------------------------|
| * <input type="checkbox"/> | 32 kHz CPU operation, realtime clock time base       |
| * <input type="checkbox"/> | No 32 kHz CPU operation, realtime clock time base    |
| <input type="checkbox"/>   | No 32 kHz CPU operation, no realtime clock time base |

Note: When an asterisked item is selected, "crystal resonator" is necessary for subsystem oscillator (X1 X2).

3. ROM Code Data Organization

For a microcomputer with EPROM mounted (including a ZTAT™ microcomputer), specify the combined upper/lower type.

|                          |                                                                                                                   |  |
|--------------------------|-------------------------------------------------------------------------------------------------------------------|--|
| <input type="checkbox"/> | Combined lower/upper type                                                                                         |  |
| •                        | Both the lower 5 data bits (L) and the upper 5 data bits (U) are written to a single EPROM in the order LULULU... |  |
| <input type="checkbox"/> | Separate lower/upper type                                                                                         |  |
| •                        | The lower 5 data bits (L) and upper 5 data bits (U) are written to separate EPROMs respectively.                  |  |

4. System Oscillator (OSC1-OSC2)

|                          |                    |     |     |
|--------------------------|--------------------|-----|-----|
| <input type="checkbox"/> | Ceramic oscillator | f = | MHz |
| <input type="checkbox"/> | Crystal oscillator | f = | MHz |
| <input type="checkbox"/> | External clock     | f = | MHz |

5. Subsystem Oscillator (X1 X2)

|                                            |                |
|--------------------------------------------|----------------|
| <input type="checkbox"/> Not used          | —              |
| <input type="checkbox"/> Crystal resonator | f = 32.768 kHz |

6. Stop Mode

|                                        |
|----------------------------------------|
| <input type="checkbox"/> Yes (used)    |
| <input type="checkbox"/> No (not used) |

7. Package

|                                  |
|----------------------------------|
| <input type="checkbox"/> FP-80A  |
| <input type="checkbox"/> TFP-80C |
| <input type="checkbox"/> Chip    |

Note: The specifications of shipped chips differ from those of the package product. Please contact our sales staff for details.

HD404889/HD404899/HD404878/HD404868 Series

Option List HD404898, HD4048912, HD404899, HCD404899

Please check off the appropriate applications and enter the necessary information.

|                            |      |       |     |
|----------------------------|------|-------|-----|
| Date of order              | Year | Month | Day |
| Customer                   |      |       |     |
| Department                 |      |       |     |
| Name                       |      |       |     |
| ROM code name              |      |       |     |
| LSI number (Hitachi entry) |      |       |     |

1. ROM Size

|                                    |           |
|------------------------------------|-----------|
| <input type="checkbox"/> HD404898  | 8 kwords  |
| <input type="checkbox"/> HD4048912 | 12 kwords |
| <input type="checkbox"/> HD404899  | 16 kwords |
| <input type="checkbox"/> HCD404899 | 16 kwords |

2. Function Options

|                          |                                                      |
|--------------------------|------------------------------------------------------|
| <input type="checkbox"/> | 32 kHz CPU operation, realtime clock time base       |
| <input type="checkbox"/> | No 32 kHz CPU operation, realtime clock time base    |
| <input type="checkbox"/> | No 32 kHz CPU operation, no realtime clock time base |

Note: When an asterisked item is selected, "crystal resonator" is necessary for subsystem oscillator (X1 X2).

3. ROM Code Data Organization

For a microcomputer with EPROM mounted (including a ZTAT™ microcomputer), specify the combined upper/lower type.

|                          |                           |                                                                                                                                                                   |
|--------------------------|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <input type="checkbox"/> | Combined lower/upper type | <ul style="list-style-type: none"><li>Both the lower 5 data bits (L) and the upper 5 data bits (U) are written to a single EPROM in the order LULULU...</li></ul> |
| <input type="checkbox"/> | Separate lower/upper type | <ul style="list-style-type: none"><li>The lower 5 data bits (L) and upper 5 data bits (U) are written to separate EPROMs respectively.</li></ul>                  |

4. System Oscillator (OSC1-OSC2)

|                          |                    |     |     |
|--------------------------|--------------------|-----|-----|
| <input type="checkbox"/> | Ceramic oscillator | f = | MHz |
| <input type="checkbox"/> | Crystal oscillator | f = | MHz |
| <input type="checkbox"/> | External clock     | f = | MHz |

5. Subsystem Oscillator (X1 X2)

|                                            |                |
|--------------------------------------------|----------------|
| <input type="checkbox"/> Not used          | —              |
| <input type="checkbox"/> Crystal resonator | f = 32.768 kHz |

6. Stop Mode

|                                        |
|----------------------------------------|
| <input type="checkbox"/> Yes (used)    |
| <input type="checkbox"/> No (not used) |

7. Package

|                                  |
|----------------------------------|
| <input type="checkbox"/> FP-80A  |
| <input type="checkbox"/> TFP-80C |
| <input type="checkbox"/> Chip    |

Note: The specifications of shipped chips differ from those of the package product. Please contact our sales staff for details.

HD404889/HD404899/HD404878/HD404868 Series

Option List HD404874, HD404878, HCD404878

Please check off the appropriate applications and enter the necessary information.

|                            |      |       |     |
|----------------------------|------|-------|-----|
| Date of order              | Year | Month | Day |
| Customer                   |      |       |     |
| Department                 |      |       |     |
| Name                       |      |       |     |
| ROM code name              |      |       |     |
| LSI number (Hitachi entry) |      |       |     |

1. ROM Size

|                                    |          |
|------------------------------------|----------|
| <input type="checkbox"/> HD404874  | 4 kwords |
| <input type="checkbox"/> HD404878  | 8 kwords |
| <input type="checkbox"/> HCD404878 | 8 kwords |

2. Function Options

|                            |                                                      |
|----------------------------|------------------------------------------------------|
| * <input type="checkbox"/> | 32 kHz CPU operation, realtime clock time base       |
| * <input type="checkbox"/> | No 32 kHz CPU operation, realtime clock time base    |
| <input type="checkbox"/>   | No 32 kHz CPU operation, no realtime clock time base |

Note: When an asterisked item is selected, "crystal resonator" is necessary for subsystem oscillator (X1 X2).

3. ROM Code Data Organization

For a microcomputer with EPROM mounted (including a ZTAT™ microcomputer), specify the combined upper/lower type.

|                          |                                                                                                                   |
|--------------------------|-------------------------------------------------------------------------------------------------------------------|
| <input type="checkbox"/> | Combined lower/upper type                                                                                         |
| •                        | Both the lower 5 data bits (L) and the upper 5 data bits (U) are written to a single EPROM in the order LULULU... |
| <input type="checkbox"/> | Separate lower/upper type                                                                                         |
| •                        | The lower 5 data bits (L) and upper 5 data bits (U) are written to separate EPROMs respectively.                  |

4. System Oscillator (OSC1-OSC2)

|                          |                    |     |     |
|--------------------------|--------------------|-----|-----|
| <input type="checkbox"/> | Ceramic oscillator | f = | MHz |
| <input type="checkbox"/> | Crystal oscillator | f = | MHz |
| <input type="checkbox"/> | External clock     | f = | MHz |

5. Subsystem Oscillator (X1 X2)

|                          |                   |                |
|--------------------------|-------------------|----------------|
| <input type="checkbox"/> | Not used          | —              |
| <input type="checkbox"/> | Crystal resonator | f = 32.768 kHz |

6. Stop Mode

|                          |               |
|--------------------------|---------------|
| <input type="checkbox"/> | Yes (used)    |
| <input type="checkbox"/> | No (not used) |

7. Package

|                          |         |
|--------------------------|---------|
| <input type="checkbox"/> | FP-80A  |
| <input type="checkbox"/> | TFP-80C |
| <input type="checkbox"/> | Chip    |

Note: The specifications of shipped chips differ from those of the package product. Please contact our sales staff for details.

Option List HD404864, HD404868

Please check off the appropriate applications and enter the necessary information.

|                            |      |       |     |
|----------------------------|------|-------|-----|
| Date of order              | Year | Month | Day |
| Customer                   |      |       |     |
| Department                 |      |       |     |
| Name                       |      |       |     |
| ROM code name              |      |       |     |
| LSI number (Hitachi entry) |      |       |     |

1. ROM Size

|                                   |          |
|-----------------------------------|----------|
| <input type="checkbox"/> HD404864 | 4 kwords |
| <input type="checkbox"/> HD404868 | 8 kwords |

2. Function Options

|                            |                                                      |
|----------------------------|------------------------------------------------------|
| * <input type="checkbox"/> | 32 kHz CPU operation, realtime clock time base       |
| * <input type="checkbox"/> | No 32 kHz CPU operation, realtime clock time base    |
| <input type="checkbox"/>   | No 32 kHz CPU operation, no realtime clock time base |

Note: When an asterisked item is selected, "crystal resonator" is necessary for subsystem oscillator (X1 X2).

3. ROM Code Data Organization

For a microcomputer with EPROM mounted (including a ZTAT™ microcomputer), specify the combined upper/lower type.

|                          |                                                                                                                   |
|--------------------------|-------------------------------------------------------------------------------------------------------------------|
| <input type="checkbox"/> | Combined lower/upper type                                                                                         |
| •                        | Both the lower 5 data bits (L) and the upper 5 data bits (U) are written to a single EPROM in the order LULULU... |
| <input type="checkbox"/> | Separate lower/upper type                                                                                         |
| •                        | The lower 5 data bits (L) and upper 5 data bits (U) are written to separate EPROMs respectively.                  |

4. System Oscillator (OSC1-OSC2)

|                          |                    |     |     |
|--------------------------|--------------------|-----|-----|
| <input type="checkbox"/> | Ceramic oscillator | f = | MHz |
| <input type="checkbox"/> | Crystal oscillator | f = | MHz |
| <input type="checkbox"/> | External clock     | f = | MHz |

5. Subsystem Oscillator (X1 X2)

|                          |                   |                |
|--------------------------|-------------------|----------------|
| <input type="checkbox"/> | Not used          | —              |
| <input type="checkbox"/> | Crystal resonator | f = 32.768 kHz |

6. Stop Mode

|                          |               |
|--------------------------|---------------|
| <input type="checkbox"/> | Yes (used)    |
| <input type="checkbox"/> | No (not used) |

7. Package

|                          |        |
|--------------------------|--------|
| <input type="checkbox"/> | FP-64A |
| <input type="checkbox"/> | DP-64S |

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