

# HM6207H Series

262,144-word × 1-bit High Speed CMOS Static RAM

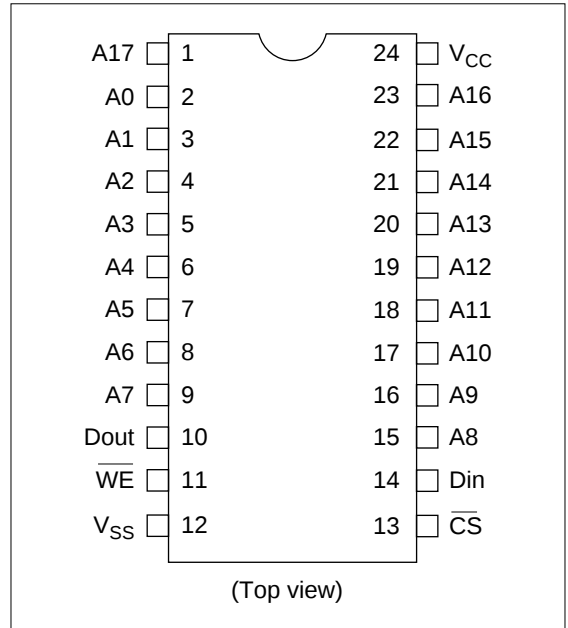
## Features

- Single 5 V supply and high density 24-pin package
- High speed  
Access time: 25/35/45 ns (max)
- Low power
  - Operation: 300 mW (typ)
  - Standby: 100  $\mu$ W (typ)  
30  $\mu$ W (typ) (L-version)
- Completely static memory required, no clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible, all inputs and outputs
- Battery back-up operation capability (L-version)

## Ordering Information

| Type No.      | Access time | Package                              |
|---------------|-------------|--------------------------------------|
| HM6207HP-25   | 25 ns       | 300-mil 24-pin plastic DIP (DP-24NC) |
| HM6207HP-35   | 35 ns       |                                      |
| HM6207HP-45   | 45 ns       |                                      |
| HM6207HLP-25  | 25 ns       | 300-mil 24-pin SOJ (CP-24D)          |
| HM6207HLP-35  | 35 ns       |                                      |
| HM6207HLP-45  | 45 ns       |                                      |
| HM6207HJP-25  | 25 ns       | 300-mil 24-pin SOJ (CP-24D)          |
| HM6207HJP-35  | 35 ns       |                                      |
| HM6207HJP-45  | 45 ns       |                                      |
| HM6207HLJP-25 | 25 ns       | 300-mil 24-pin SOJ (CP-24D)          |
| HM6207HLJP-35 | 35 ns       |                                      |
| HM6207HLJP-45 | 45 ns       |                                      |

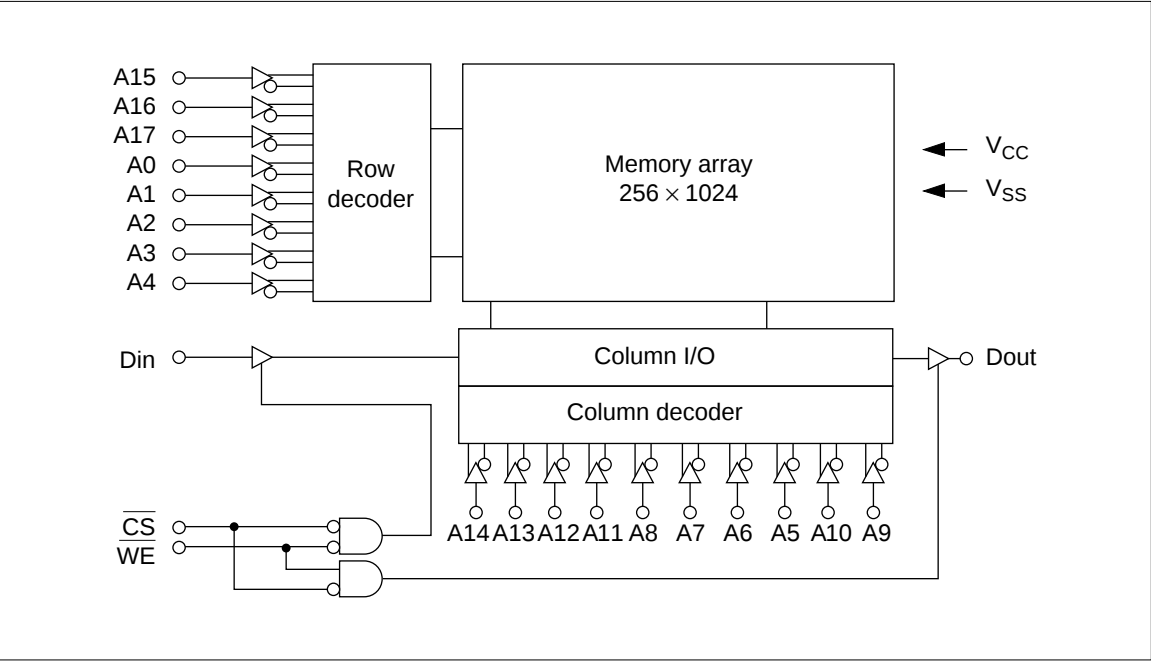
## Pin Arrangement



## Pin Description

| Pin name        | Function     |
|-----------------|--------------|
| A0–A17          | Address      |
| Din             | Data input   |
| Dout            | Data output  |
| $\overline{CS}$ | Chip select  |
| $\overline{WE}$ | Write enable |
| V <sub>CC</sub> | Power supply |
| V <sub>SS</sub> | Ground       |

Block Diagram



## Function Table

| $\overline{\text{CS}}$ | $\overline{\text{WE}}$ | Mode         | $V_{\text{CC}}$ current         | I/O pin | Ref. cycle  |
|------------------------|------------------------|--------------|---------------------------------|---------|-------------|
| H                      | ×                      | Not selected | $I_{\text{SB}}, I_{\text{SB1}}$ | High-Z  | —           |
| L                      | H                      | Read         | $I_{\text{CC}}$                 | Dout    | Read cycle  |
| L                      | L                      | Write        | $I_{\text{CC}}$                 | High-Z  | Write cycle |

Note: × = Don't care.

## Absolute Maximum Ratings

| Parameter                                      | Symbol            | Rating         | Unit |
|------------------------------------------------|-------------------|----------------|------|
| Voltage on any pin relative to $V_{\text{SS}}$ | $V_{\text{in}}$   | −0.5*1 to +7.0 | V    |
| Power dissipation                              | $P_{\text{T}}$    | 1.0            | W    |
| Operating temperature range                    | $T_{\text{opr}}$  | 0 to +70       | °C   |
| Storage temperature range                      | $T_{\text{stg}}$  | −55 to +125    | °C   |
| Storage temperature range under bias           | $T_{\text{bias}}$ | −10 to +85     | °C   |

Note: 1.  $V_{\text{in min}}$  = −2.5 V for pulse width < 10 ns.

Recommended DC Operating Conditions ( $T_{\text{a}}$  = 0 to +70°C)

| Parameter                    | Symbol          | Min.   | Typ. | Max. | Unit |
|------------------------------|-----------------|--------|------|------|------|
| Supply voltage               | $V_{\text{CC}}$ | 4.5    | 5.0  | 5.5  | V    |
|                              | $V_{\text{SS}}$ | 0      | 0    | 0    | V    |
| Input high (logic 1) voltage | $V_{\text{IH}}$ | 2.2    | —    | 6.0  | V    |
| Input low (logic 0) voltage  | $V_{\text{IL}}$ | −0.5*1 | —    | 0.8  | V    |

Note: 1.  $V_{\text{IL min}}$  = −2.0 V for pulse width ≤ 10 ns.

**DC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                        | Symbol    | HM6207H-25 |       |      | HM6207H-35/45 |       |      | Unit          | Test conditions                                                                                                            |
|----------------------------------|-----------|------------|-------|------|---------------|-------|------|---------------|----------------------------------------------------------------------------------------------------------------------------|
|                                  |           | Min        | Typ*1 | Max  | Min           | Typ*1 | Max  |               |                                                                                                                            |
| Input leakage current            | $I_{LI}$  | —          | —     | 2.0  | —             | —     | 2.0  | $\mu\text{A}$ | $V_{CC} = \text{Max}$ ,<br>$V_{in} = V_{SS}$ to $V_{CC}$                                                                   |
| Output leakage current           | $I_{LO}$  | —          | —     | 10.0 | —             | —     | 10.0 | $\mu\text{A}$ | $\overline{CS} = V_{IH}$ ,<br>$V_{I/O} = V_{SS}$ to $V_{CC}$                                                               |
| Operating power supply current   | $I_{CC}$  | —          | 60    | 120  | —             | 50    | 100  | $\text{mA}$   | $\overline{CS} = V_{IL}$ , $I_{I/O} = 0\text{ mA}$ ,<br>min cycle, duty = 100%                                             |
|                                  | $I_{CC1}$ | —          | 40    | 80   | —             | 40    | 80   | $\text{mA}$   | $\overline{CS} = V_{IL}$ , $I_{I/O} = 0\text{ mA}$ ,<br>t cycle = 50 ns,<br>duty = 100%                                    |
| Standby power supply current     | $I_{SB}$  | —          | 20    | 40   | —             | 15    | 30   | $\text{mA}$   | $\overline{CS} = V_{IH}$ , min cycle                                                                                       |
| Standby power supply current (1) | $I_{SB1}$ | —          | 0.02  | 2.0  | —             | 0.02  | 2.0  | $\text{mA}$   | $\overline{CS} \geq V_{CC} - 0.2\text{ V}$ ,<br>$0\text{ V} \leq V_{in} < 0.2$ , or<br>$V_{in} \geq V_{CC} - 0.2\text{ V}$ |
|                                  | L-Version | —          | 0.006 | 0.1  | —             | 0.006 | 0.1  |               |                                                                                                                            |
| Output low voltage               | $V_{OL}$  | —          | —     | 0.4  | —             | —     | 0.4  | $\text{V}$    | $I_{OL} = 8\text{ mA}$                                                                                                     |
| Output high voltage              | $V_{OH}$  | 2.4        | —     | —    | 2.4           | —     | —    | $\text{V}$    | $I_{OH} = -4.0\text{ mA}$                                                                                                  |

Note: 1. Typical values are at  $V_{CC} = 5.0\text{ V}$ ,  $T_a = +25^\circ\text{C}$  and not guaranteed.

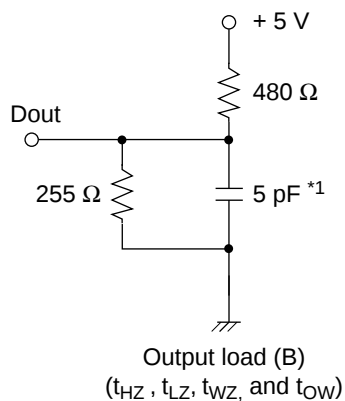
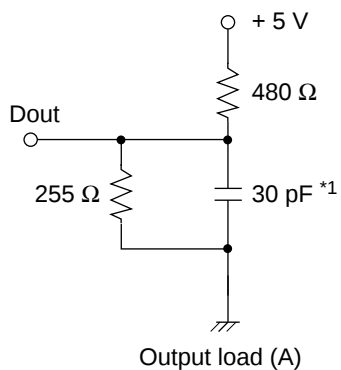
**Capacitance** ( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )\*1

| Parameter          | Symbol    | Min | Max | Unit        | Test conditions        |
|--------------------|-----------|-----|-----|-------------|------------------------|
| Input capacitance  | $C_{in}$  | —   | 6   | $\text{pF}$ | $V_{in} = 0\text{ V}$  |
| Output capacitance | $C_{out}$ | —   | 10  | $\text{pF}$ | $V_{out} = 0\text{ V}$ |

Note: 1. This parameter is sampled and is not 100% tested.

**AC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$  unless otherwise noted)**AC Test Conditions**

- Input pulse levels:  $V_{ss}$  to  $3.0\text{ V}$
- Input and output timing reference levels:  $1.5\text{ V}$
- Input rise and fall times:  $5\text{ ns}$
- Output load: See figures



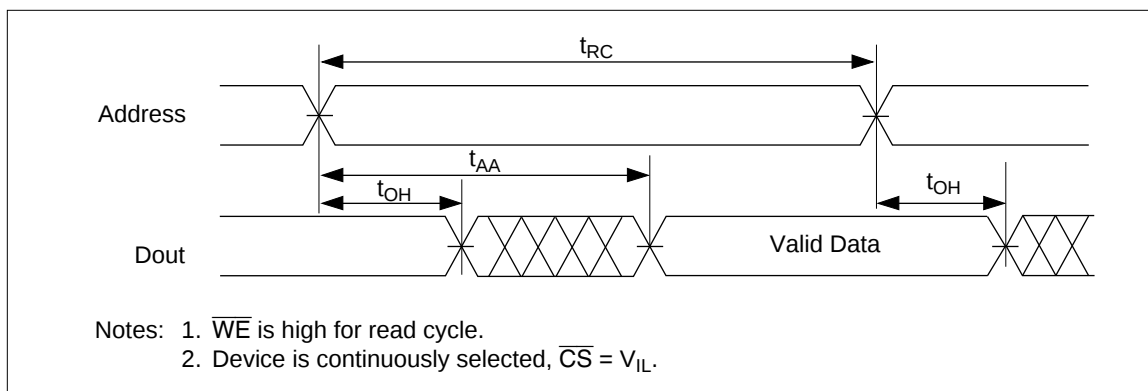
Note: 1. Including scope and jig

## Read Cycle

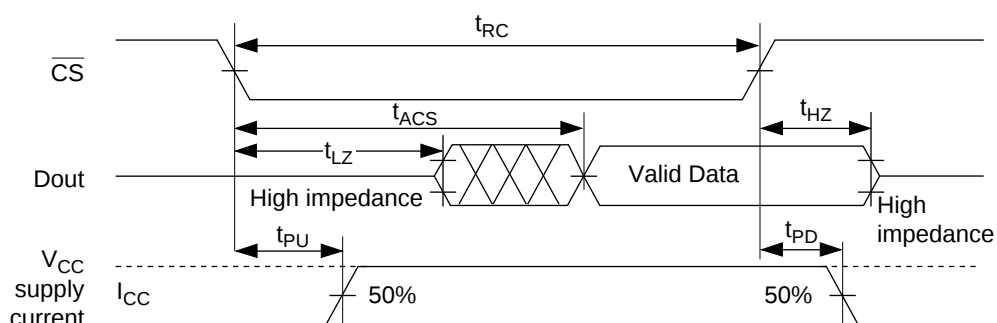
| Parameter                            | Symbol        | HM6207H-25 |     | HM6207H-35 |     | HM6207H-45 |     | Unit |
|--------------------------------------|---------------|------------|-----|------------|-----|------------|-----|------|
|                                      |               | Min        | Max | Min        | Max | Min        | Max |      |
| Read cycle time                      | $t_{RC}$      | 25         | —   | 35         | —   | 45         | —   | ns   |
| Address access time                  | $t_{AA}$      | —          | 25  | —          | 35  | —          | 45  | ns   |
| Chip select access time              | $t_{ACS}$     | —          | 25  | —          | 35  | —          | 45  | ns   |
| Output hold from address change      | $t_{OH}$      | 5          | —   | 5          | —   | 5          | —   | ns   |
| Chip selection to output in low-Z    | $t_{LZ}^{*1}$ | 5          | —   | 5          | —   | 5          | —   | ns   |
| Chip deselection to output in high-Z | $t_{HZ}^{*1}$ | 0          | 15  | 0          | 20  | 0          | 20  | ns   |
| Chip selection to power up time      | $t_{PU}$      | 0          | —   | 0          | —   | 0          | —   | ns   |
| Chip deselection to power down time  | $t_{PD}$      | —          | 15  | —          | 25  | —          | 30  | ns   |

Note: 1. Transition is measured  $\pm 200$  mV from steady-state voltage with Load (B).  
These parameters are sampled and not 100% tested.

## Read Timing Waveform (1)



## Read Timing Waveform (2)



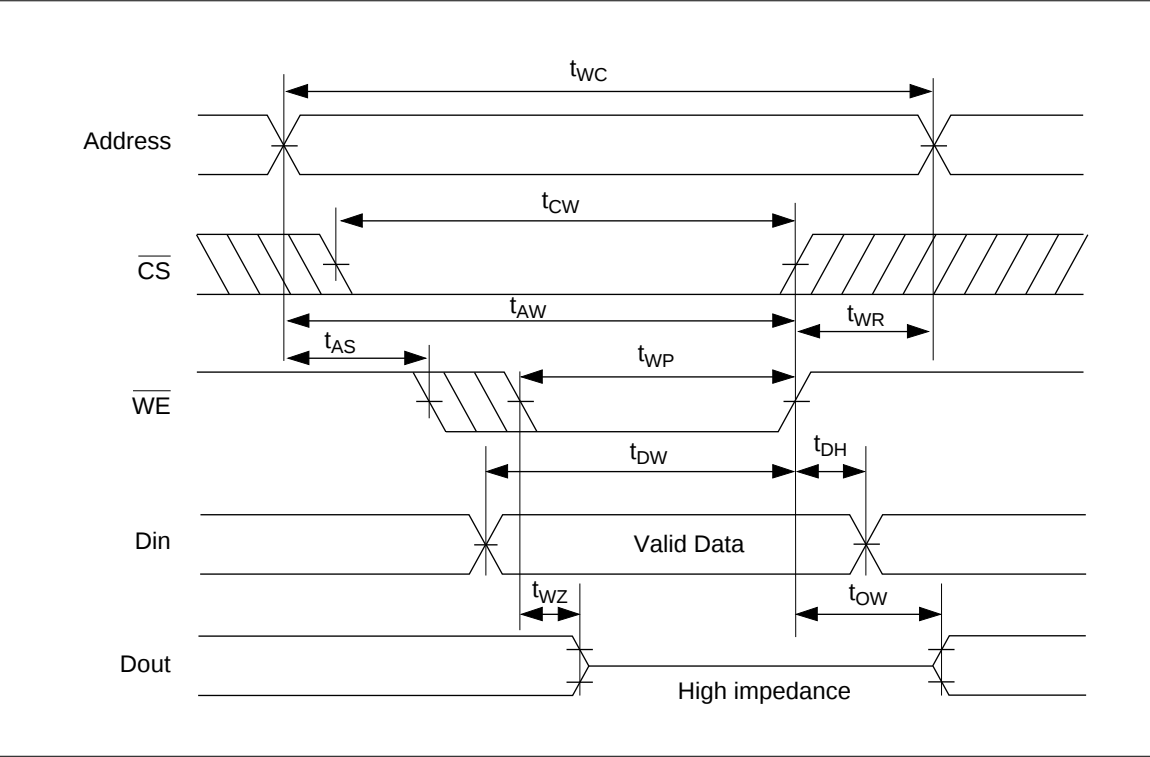
- Notes: 1.  $\overline{WE}$  is high for read cycle.  
2. Address valid prior to coincident with  $\overline{CS}$  transition low.

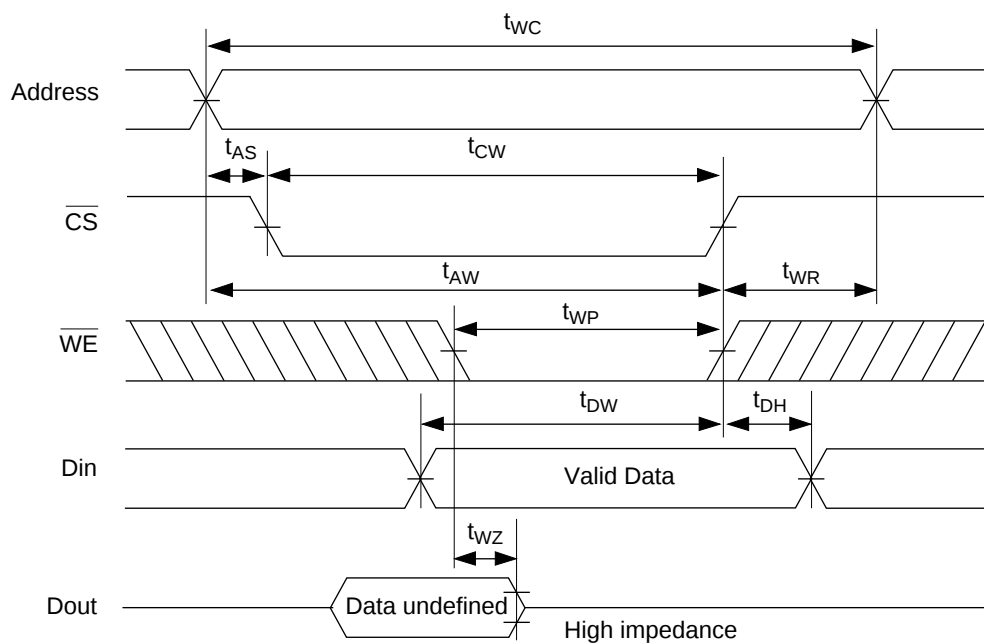
## Write Cycle

| Parameter                         | Symbol        | HM6207H-25 |     | HM6207H-35 |     | HM6207H-45 |     | Unit |
|-----------------------------------|---------------|------------|-----|------------|-----|------------|-----|------|
|                                   |               | Min        | Max | Min        | Max | Min        | Max |      |
| Write cycle time                  | $t_{WC}$      | 25         | —   | 35         | —   | 45         | —   | ns   |
| Chip selection to end of write    | $t_{CW}$      | 20         | —   | 30         | —   | 40         | —   | ns   |
| Address valid to end of write     | $t_{AW}$      | 20         | —   | 30         | —   | 40         | —   | ns   |
| Address setup time                | $t_{AS}$      | 0          | —   | 0          | —   | 0          | —   | ns   |
| Write pulse width                 | $t_{WP}$      | 20         | —   | 25         | —   | 25         | —   | ns   |
| Write recovery time               | $t_{WR}$      | 3          | —   | 3          | —   | 3          | —   | ns   |
| Data valid to end of write        | $t_{DW}$      | 15         | —   | 20         | —   | 20         | —   | ns   |
| Data hold time                    | $t_{DH}$      | 0          | —   | 0          | —   | 0          | —   | ns   |
| Write enabled to output in high-Z | $t_{WZ}^{*1}$ | 0          | 15  | 0          | 20  | 0          | 25  | ns   |
| Output active from end of write   | $t_{OW}^{*1}$ | 0          | —   | 0          | —   | 0          | —   | ns   |

Note: 1. Transition is measured  $\pm 200$  mV from high-impedance voltage with Load (B).  
This parameter is sampled and is not 100% tested.

Write Timing Waveform (1) ( $\overline{\text{WE}}$  Controlled)



Write Timing Waveform (2) ( $\overline{\text{CE}}$  Controlled)

- Notes:
1. A write occurs during the overlap of a low  $\overline{\text{CS}}$  and a low  $\overline{\text{WE}}$ .
  2.  $t_{WR}$  is measured from the earlier of  $\overline{\text{CS}}$  or  $\overline{\text{WE}}$  going high to the end of the write cycle.
  3. If the CS low transition occurs simultaneously with the WE low transition, the output buffers remain in a high impedance state.
  4. Dout has the same phase as write data in this write cycle, if  $t_{WR}$  is long enough.

Low  $V_{CC}$  Data Retention Characteristics ( $T_a = 0$  to  $+70^{\circ}\text{C}$ )

These characteristics are guaranteed for the L-version only.

| Parameter                            | Symbol     | Min | Typ | Max  | Unit          | Test conditions                                                                                                                        |
|--------------------------------------|------------|-----|-----|------|---------------|----------------------------------------------------------------------------------------------------------------------------------------|
| $V_{CC}$ for data retention          | $V_{DR}$   | 2.0 | —   | —    | V             | $\overline{CS} \geq V_{CC} - 0.2\text{ V}$ ,<br>$V_{in} \geq V_{CC} - 0.2\text{ V}$ , or<br>$0\text{ V} \leq V_{in} \leq 0.2\text{ V}$ |
| Data retention current               | $I_{CCDR}$ | —   | 2   | 50*1 | $\mu\text{A}$ |                                                                                                                                        |
| Chip deselect to data retention time | $t_{CDR}$  | 0   | —   | —    | ns            |                                                                                                                                        |
| Operation recovery time              | $t_R$      | 5   | —   | —    | ms            |                                                                                                                                        |

Note: 1.  $V_{CC} = 3.0\text{ V}$

Low  $V_{CC}$  Data Retention Timing Waveform

