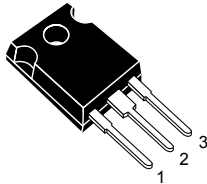
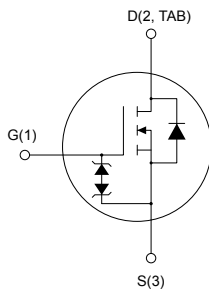


Automotive-grade N-channel 950 V, 280 mΩ typ., 17.5 A MDmesh K5 Power MOSFET in a TO-247 package


TO-247


AM01476v1_tab

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STW22N95K5	950 V	330 mΩ	17.5 A

- AEC-Q101 qualified
- Very low FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected



Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.



Product status link

[STW22N95K5](#)

Product summary

Order code	STW22N95K5
Marking	22N95K5
Package	TO-247
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	17.5	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	11	A
$I_{DM}^{(1)}$	Drain current (pulsed)	70	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	250	W
ESD	Gate-source human body model ($R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$)	2	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_J	Operating junction temperature range	-55 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 17.5\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$; $V_{DS}\text{ peak} \leq V_{(BR)DSS}$.
3. $V_{DS} \leq 760\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.5	$^{\circ}\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	50	$^{\circ}\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by $T_J\text{ max.}$)	6	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	200	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	950			V
I_{DSS}	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 950\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 950\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			50	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 9\text{ A}$		280	330	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1550	-	pF
C_{oss}	Output capacitance		-	140	-	pF
C_{rss}	Reverse transfer capacitance		-	1	-	pF
$C_{o(er)}$ ⁽¹⁾	Equivalent capacitance energy related	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }760\text{ V}$	-	65	-	pF
$C_{o(tr)}$ ⁽²⁾	Equivalent capacitance time related			178	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	3.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 760\text{ V}$, $I_D = 17.5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	48	-	nC
Q_{gs}	Gate-source charge		-	9	-	nC
Q_{gd}	Gate-drain charge		-	32.5	-	nC

1. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

2. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475\text{ V}$, $I_D = 9\text{ A}$, $R_G = 4.7\text{ }\Omega$ $V_{GS} = 10\text{ V}$	-	18	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	65	-	ns
t_f	Fall time		-	18	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		17.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		70	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17.5 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 17.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$	-	513		ns
Q_{rr}	Reverse recovery charge	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	12		μC
I_{RRM}	Reverse recovery current		-	46		A
t_{rr}	Reverse recovery time	$I_{SD} = 17.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$, $T_J = 150^\circ\text{C}$	-	670		ns
Q_{rr}	Reverse recovery charge	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	15		μC
I_{RRM}	Reverse recovery current		-	44		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

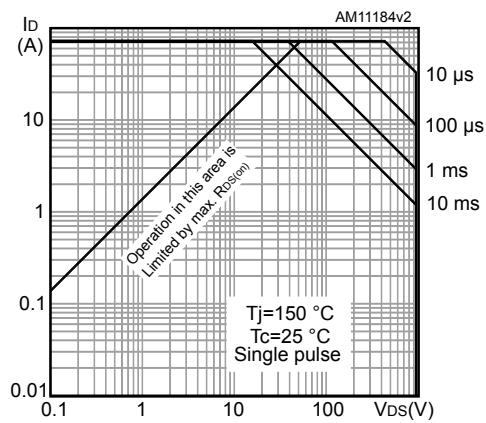


Figure 2. Normalized transient thermal impedance

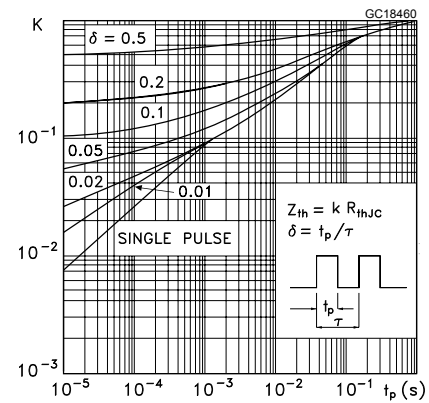


Figure 3. Typical output characteristics

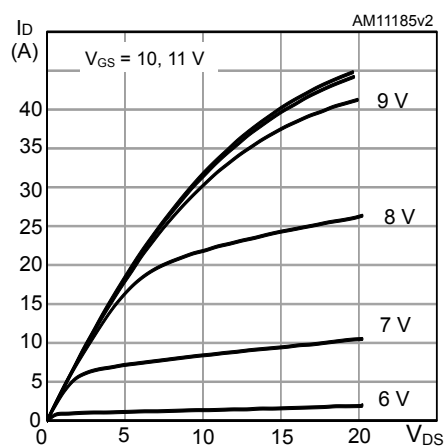


Figure 4. Typical transfer characteristics

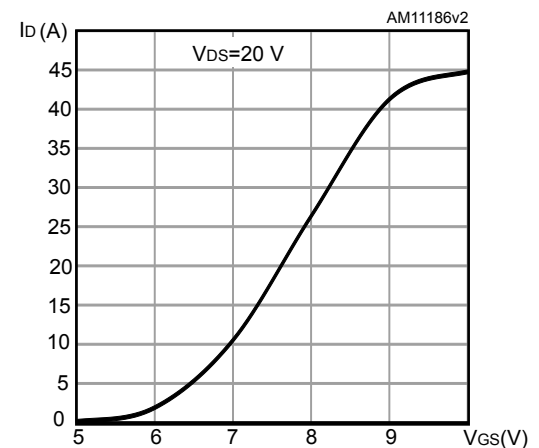


Figure 5. Typical gate charge characteristics

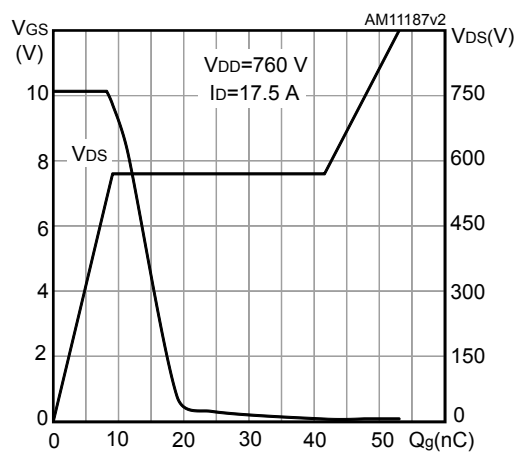


Figure 6. Typical drain-source on-resistance

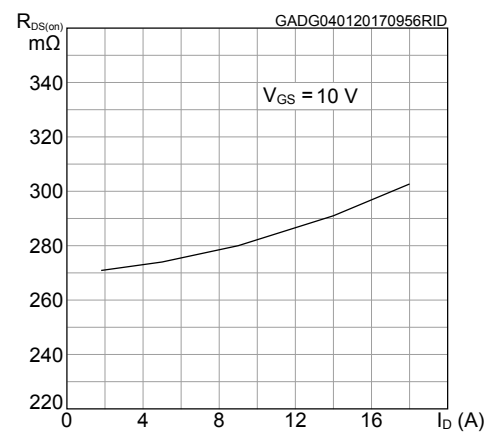


Figure 7. Typical capacitance characteristics

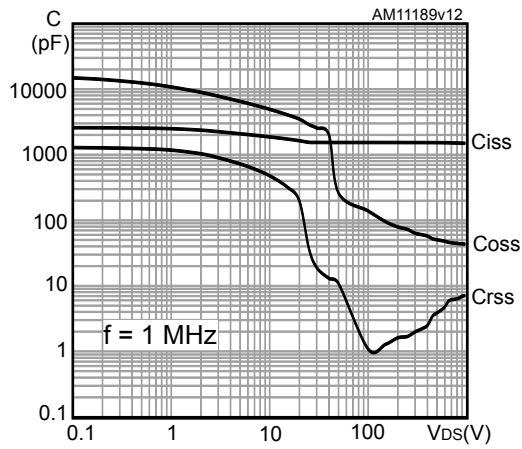


Figure 8. Typical output capacitance stored energy

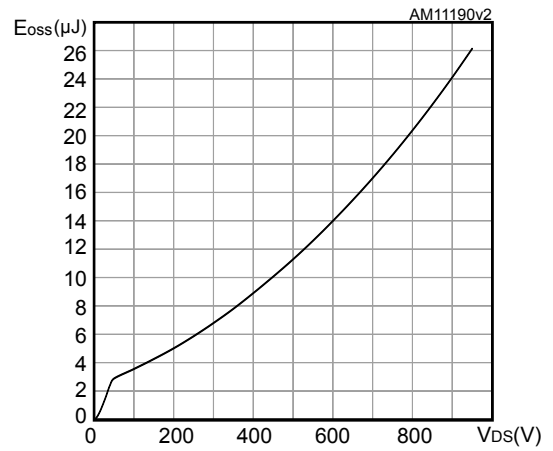


Figure 9. Normalized gate threshold vs temperature

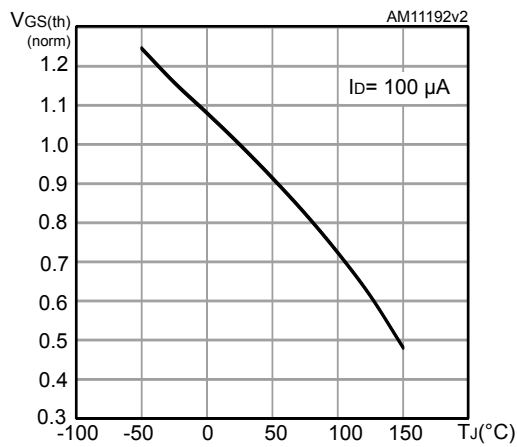


Figure 10. Normalized on-resistance vs temperature

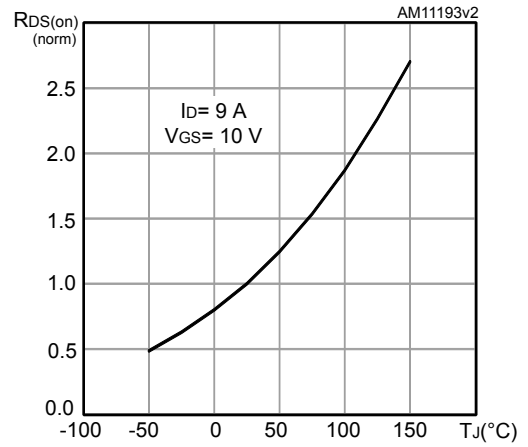


Figure 11. Typical reverse diode forward characteristics

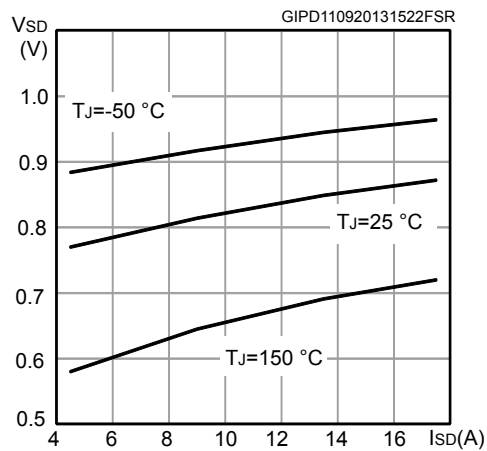


Figure 12. Normalized breakdown voltage vs temperature

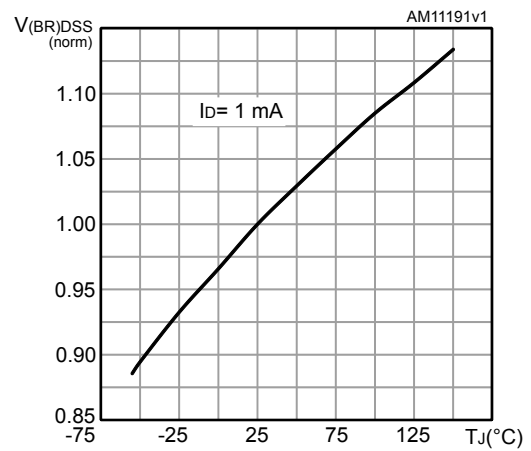
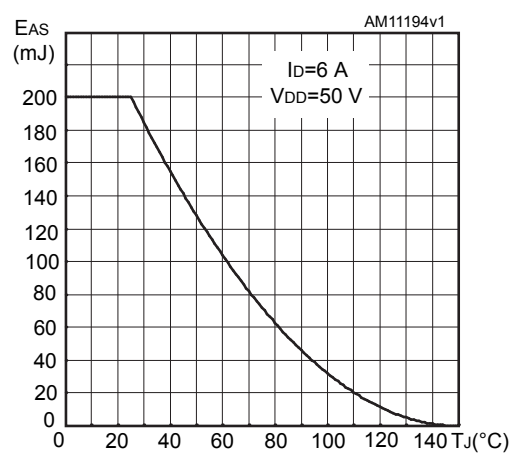


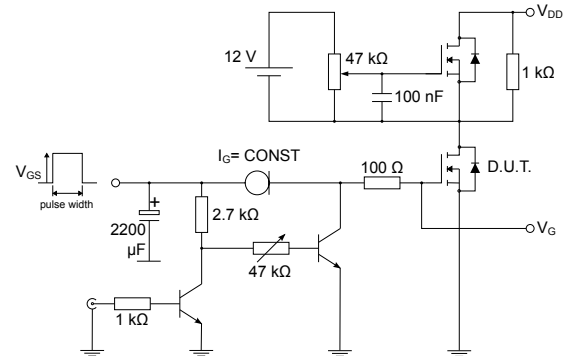
Figure 13. Maximum avalanche energy vs temperature



3 Test circuits

Figure 14. Test circuit for resistive load switching times


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Figure 15. Test circuit for gate charge behavior


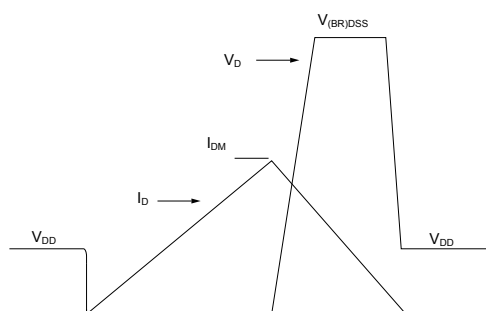
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Figure 16. Test circuit for inductive load switching and diode recovery times

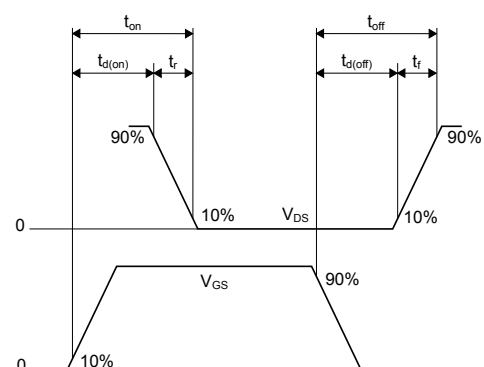

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Figure 17. Unclamped inductive load test circuit


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Figure 18. Unclamped inductive waveform


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Figure 19. Switching time waveform


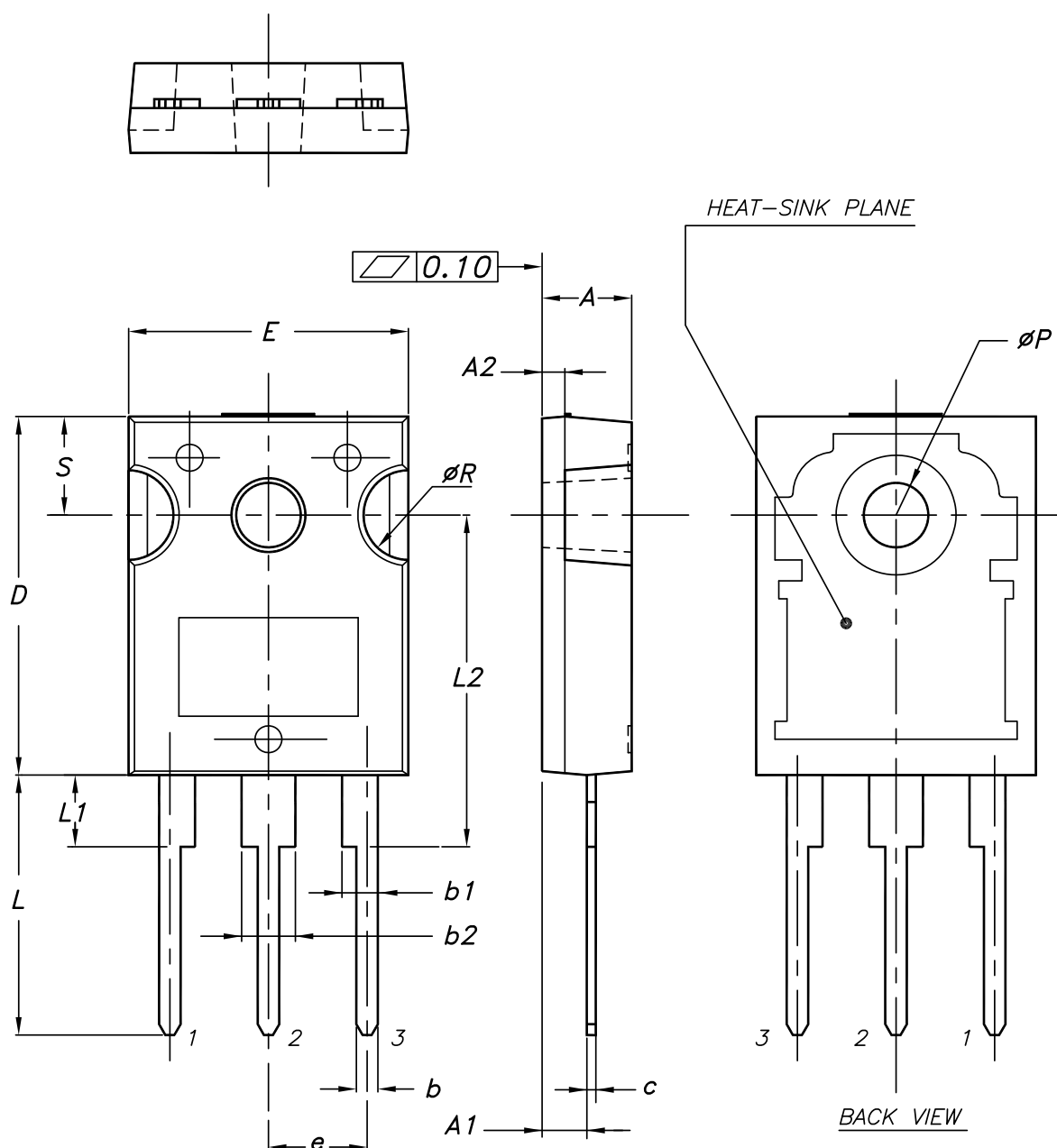
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 package information

Figure 20. TO-247 package outline



0075325_11

Table 8. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
A2		1.27	
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Revision history

Table 9. Document revision history

Date	Version	Changes
17-Oct-2013	1	First release.
19-Dec-2013	2	Datasheet promoted from preliminary to production data Modified: title and Features Minor text changes
20-Mar-2014	3	– Modified: note 3 in Table 2 – Modified: Qgs and Qgd typical values in Table 5 – Modified: typical values in Table 6 and 7 – Updated: Figure 6 – Minor text changes
11-Jan-2017	4	Updated title, features and description in cover page. Minor text changes in Section 1: "Electrical ratings" and Section 2: "Electrical characteristics". Changed Figure 7: "Static drain-source on-resistance".
19-Dec-2025	5	Updated Section 4.1: TO-247 package information . Minor text changes.

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