



# IMPORTANT NOTICE

10 December 2015

## 1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

In this document where the previous NXP references remain, please use the new links as shown below.

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Thank you for your cooperation and understanding,

WeEn Semiconductors





# BT136X-600

4Q Triac

30 April 2015

Product data sheet

## 1. General description

Planar passivated four quadrant triac in a SOT186A "full pack" plastic package intended for use in bidirectional switching and phase control applications.

## 2. Features and benefits

- High blocking voltage capability
- Isolated package
- Less sensitive gate for improved noise immunity
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants

## 3. Applications

- General purpose motor control
- General purpose switching

## 4. Quick reference data

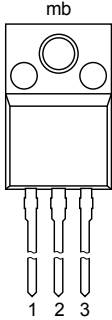
Table 1. Quick reference data

| Symbol                        | Parameter                            | Conditions                                                                                                                          | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| $V_{DRM}$                     | repetitive peak off-state voltage    |                                                                                                                                     | -   | -   | 600 | V    |
| $I_{TSM}$                     | non-repetitive peak on-state current | full sine wave; $T_{J(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a> | -   | -   | 25  | A    |
| $I_{T(RMS)}$                  | RMS on-state current                 | full sine wave; $T_h \leq 92\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>    | -   | -   | 4   | A    |
| <b>Static characteristics</b> |                                      |                                                                                                                                     |     |     |     |      |
| $I_{GT}$                      | gate trigger current                 | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+; $T_J = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 7</a>                    | -   | 5   | 35  | mA   |
|                               |                                      | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-; $T_J = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 7</a>                    | -   | 8   | 35  | mA   |
|                               |                                      | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-; $T_J = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 7</a>                    | -   | 11  | 35  | mA   |
|                               |                                      | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G+; $T_J = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 7</a>                    | -   | 30  | 70  | mA   |



5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description             | Simplified outline                                                                                         | Graphic symbol                                                                      |
|-----|--------|-------------------------|------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| 1   | T1     | main terminal 1         |  <p>TO-220F (SOT186A)</p> |  |
| 2   | T2     | main terminal 2         |                                                                                                            |                                                                                     |
| 3   | G      | gate                    |                                                                                                            |                                                                                     |
| mb  | n.c.   | mounting base; isolated |                                                                                                            |                                                                                     |

6. Ordering information

Table 3. Ordering information

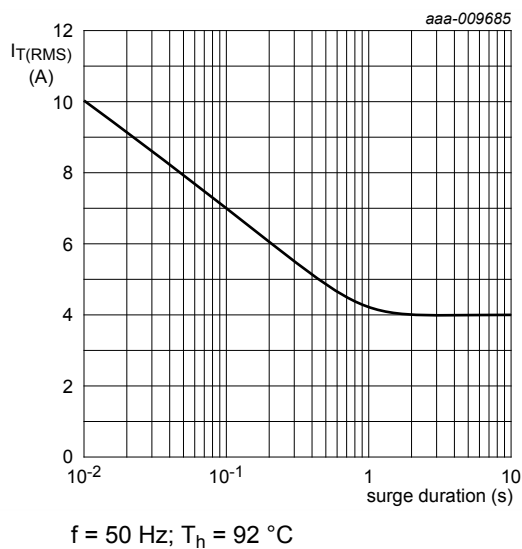
| Type number | Package |                                                                                                     |         |
|-------------|---------|-----------------------------------------------------------------------------------------------------|---------|
|             | Name    | Description                                                                                         | Version |
| BT136X-600  | TO-220F | plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack" | SOT186A |

## 7. Limiting values

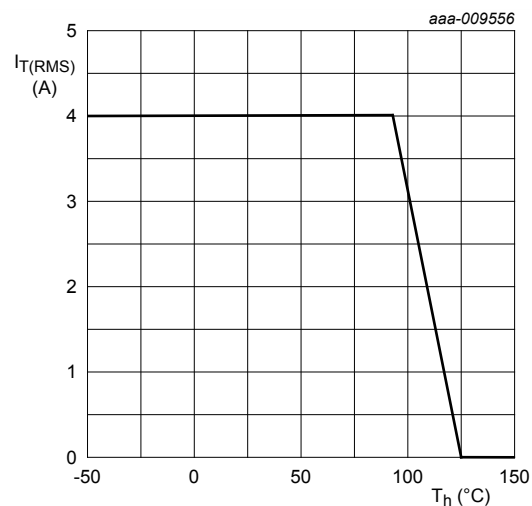
**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol              | Parameter                            | Conditions                                                                                                                       | Min | Max | Unit                   |
|---------------------|--------------------------------------|----------------------------------------------------------------------------------------------------------------------------------|-----|-----|------------------------|
| $V_{\text{DRM}}$    | repetitive peak off-state voltage    |                                                                                                                                  | -   | 600 | V                      |
| $I_{\text{T(RMS)}}$ | RMS on-state current                 | full sine wave; $T_h \leq 92^\circ\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>           | -   | 4   | A                      |
| $I_{\text{TSM}}$    | non-repetitive peak on-state current | full sine wave; $T_{\text{j(init)}} = 25^\circ\text{C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a> | -   | 25  | A                      |
|                     |                                      | full sine wave; $T_{\text{j(init)}} = 25^\circ\text{C}$ ; $t_p = 16.7\text{ ms}$                                                 | -   | 27  | A                      |
| $I^2t$              | $I^2t$ for fusing                    | $t_p = 10\text{ ms}$ ; SIN                                                                                                       | -   | 3.1 | $\text{A}^2\text{s}$   |
| $dl_T/dt$           | rate of rise of on-state current     | $I_G = 70\text{ mA}$ ; T2+ G+                                                                                                    | -   | 50  | $\text{A}/\mu\text{s}$ |
|                     |                                      | $I_G = 70\text{ mA}$ ; T2+ G-                                                                                                    | -   | 50  | $\text{A}/\mu\text{s}$ |
|                     |                                      | $I_G = 140\text{ mA}$ ; T2- G+                                                                                                   | -   | 10  | $\text{A}/\mu\text{s}$ |
|                     |                                      | $I_G = 70\text{ mA}$ ; T2- G-                                                                                                    | -   | 50  | $\text{A}/\mu\text{s}$ |
| $I_{\text{GM}}$     | peak gate current                    |                                                                                                                                  | -   | 2   | A                      |
| $P_{\text{GM}}$     | peak gate power                      |                                                                                                                                  | -   | 5   | W                      |
| $P_{\text{G(AV)}}$  | average gate power                   | over any 20 ms period                                                                                                            | -   | 0.5 | W                      |
| $T_{\text{stg}}$    | storage temperature                  |                                                                                                                                  | -40 | 150 | $^\circ\text{C}$       |
| $T_j$               | junction temperature                 |                                                                                                                                  | -   | 125 | $^\circ\text{C}$       |



**Fig. 1. RMS on-state current as a function of surge duration; maximum values**



**Fig. 2. RMS on-state current as a function of heatsink temperature; maximum values**

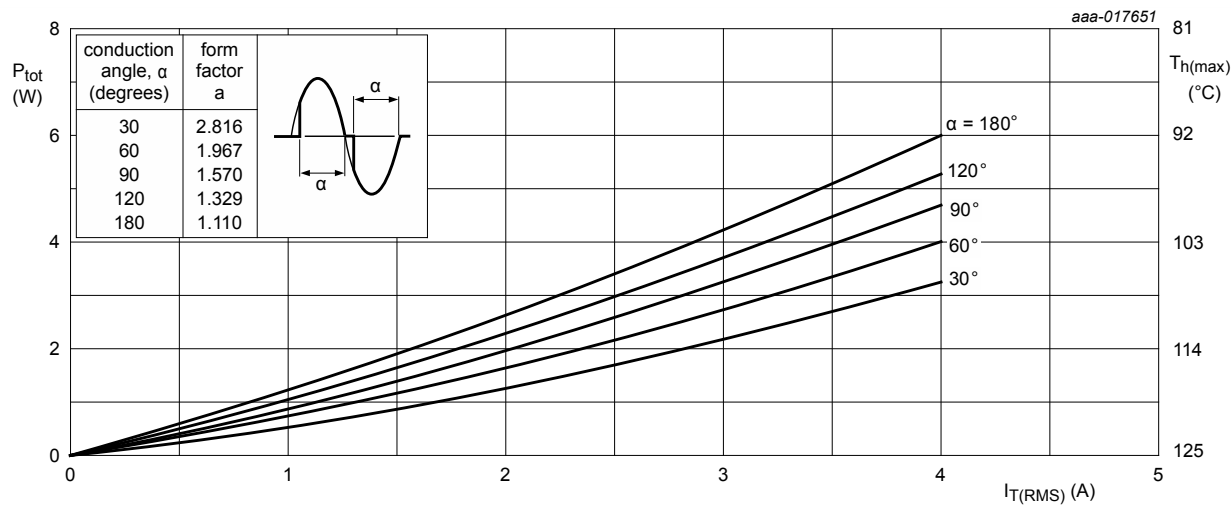


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

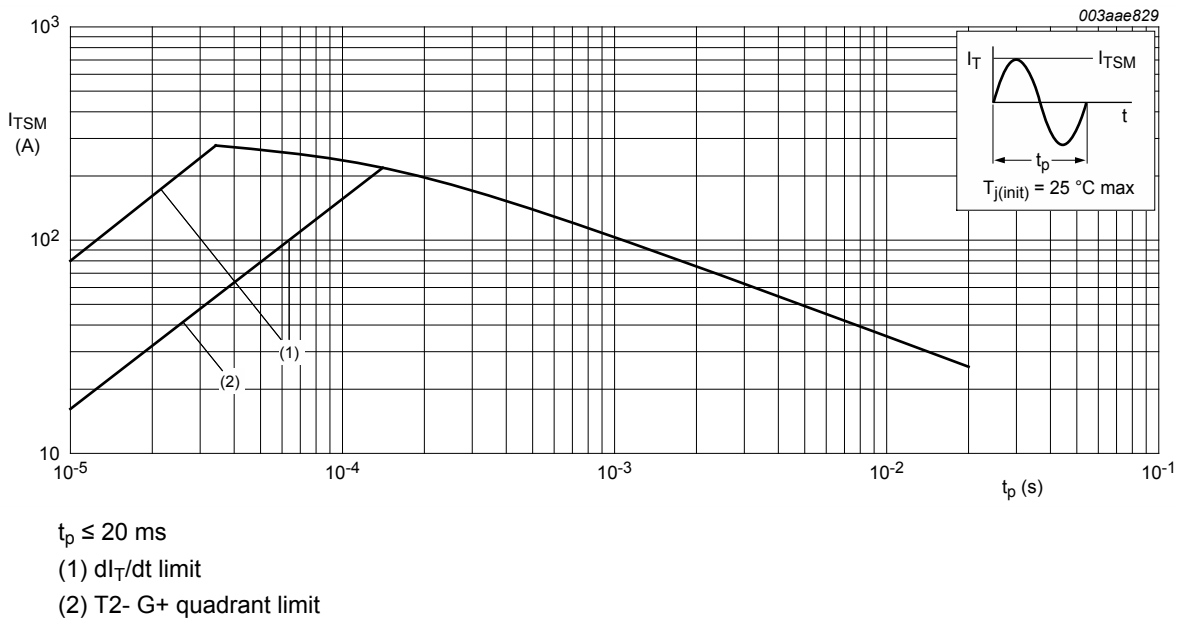
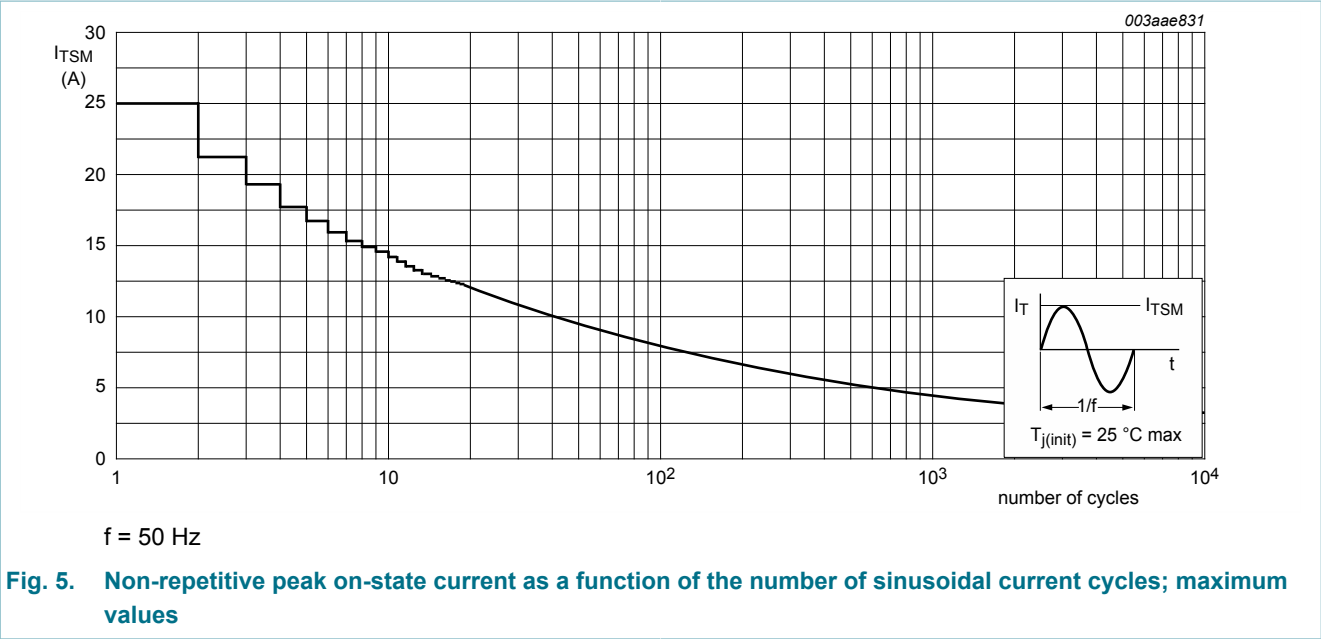


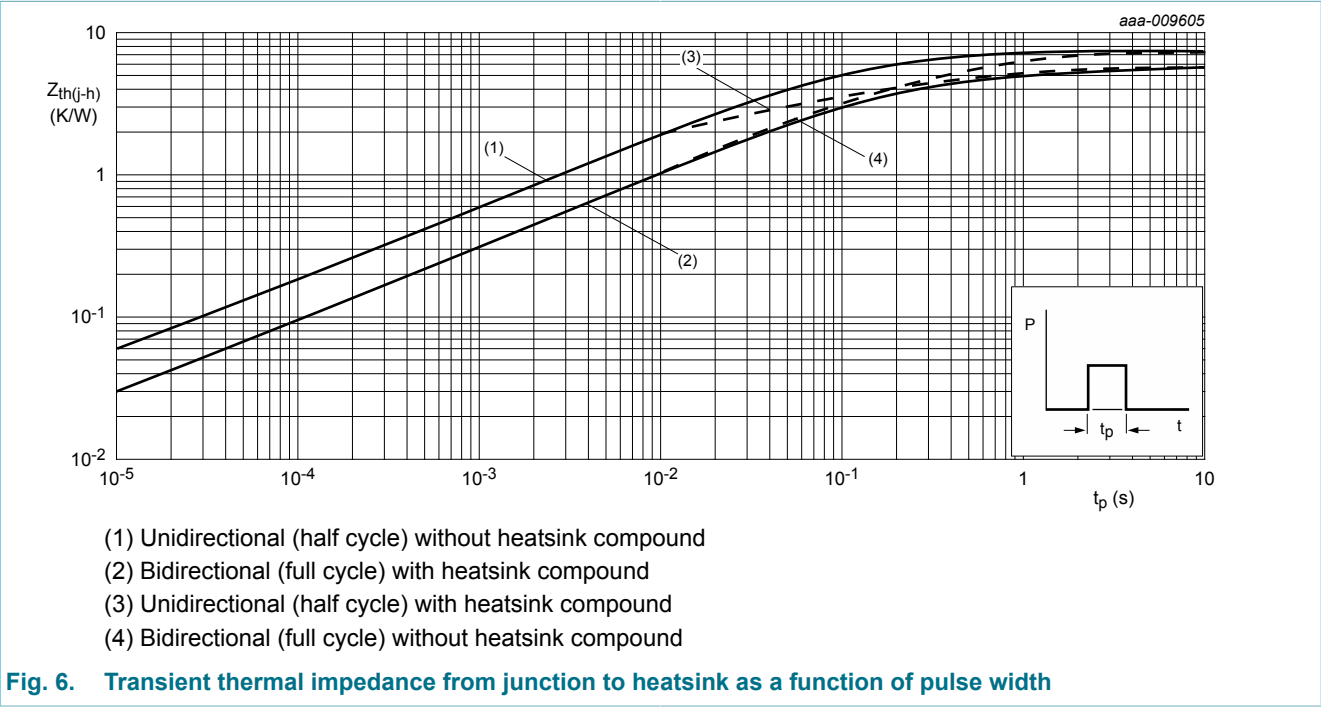
Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol        | Parameter                                    | Conditions                                            | Min | Typ | Max | Unit |
|---------------|----------------------------------------------|-------------------------------------------------------|-----|-----|-----|------|
| $R_{th(j-h)}$ | thermal resistance from junction to heatsink | full or half cycle; with heatsink compound; Fig. 6    | -   | -   | 5.5 | K/W  |
|               |                                              | full or half cycle; without heatsink compound; Fig. 6 | -   | -   | 7.2 | K/W  |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient  | in free air                                           | -   | 55  | -   | K/W  |



9. Isolation characteristics

Table 6. Isolation characteristics

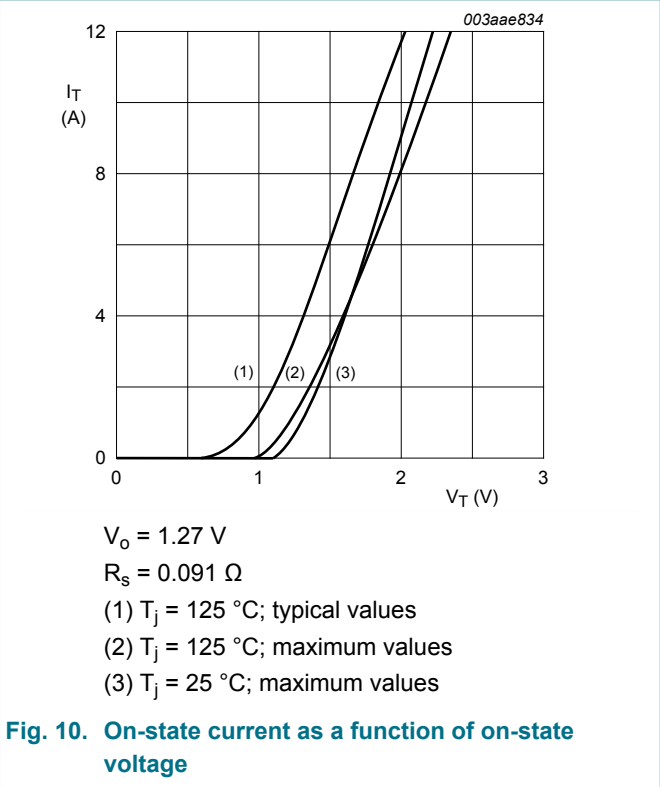
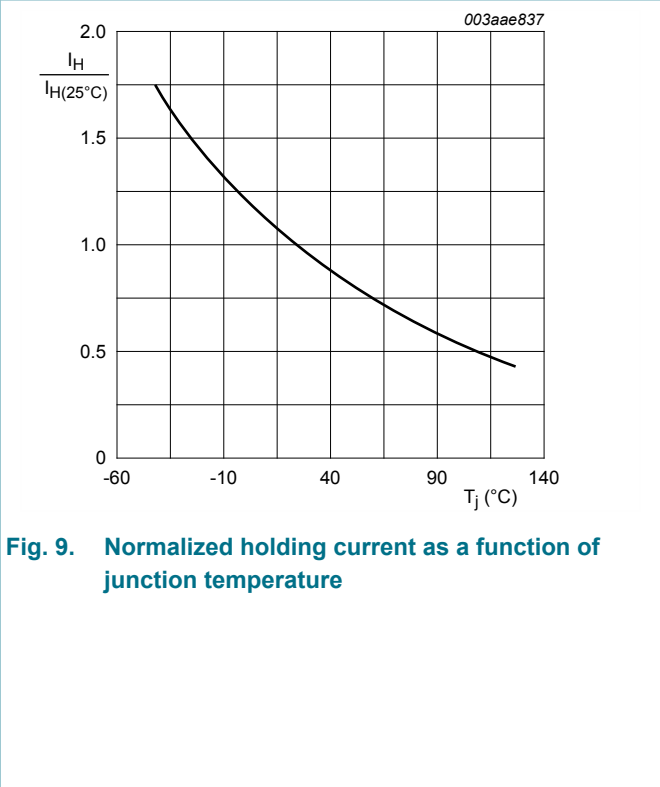
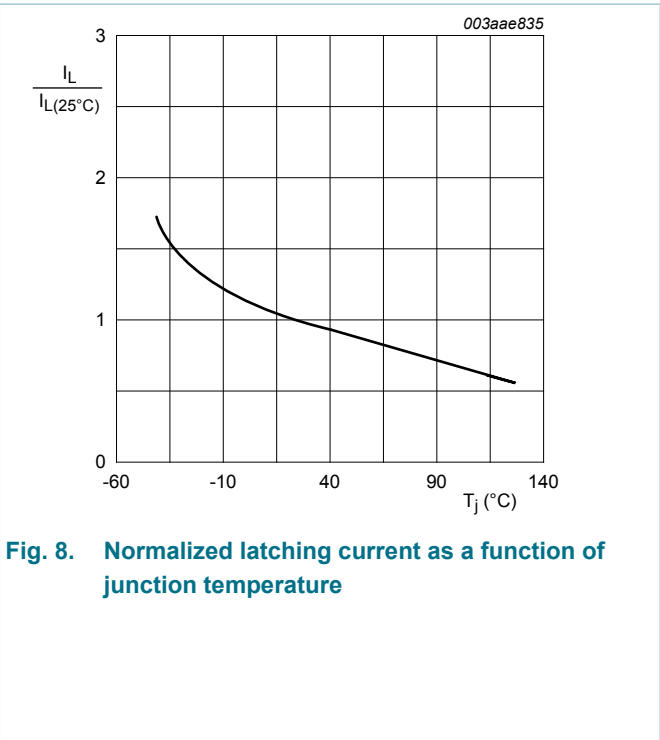
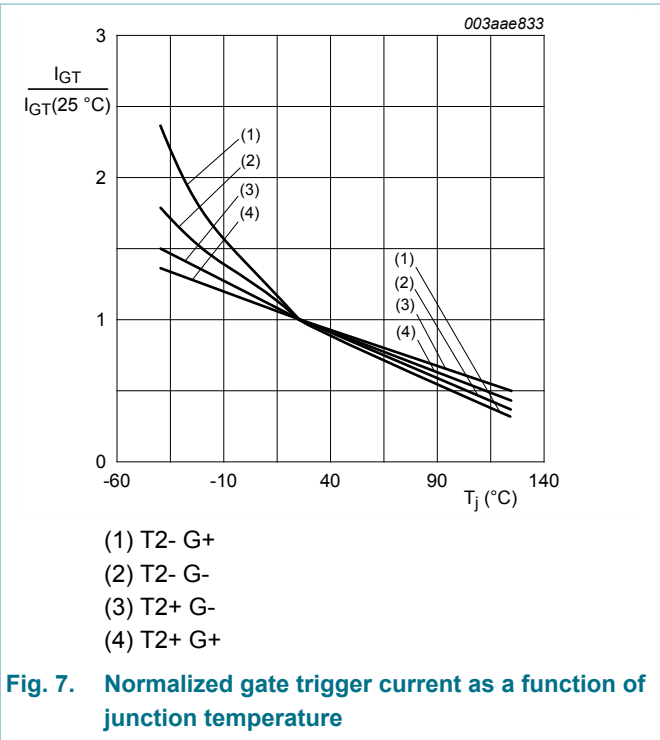
| Symbol          | Parameter             | Conditions                                                                                                                              | Min | Typ | Max  | Unit |
|-----------------|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------|------|
| $V_{isol(RMS)}$ | RMS isolation voltage | from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; T <sub>n</sub> = 25 °C | -   | -   | 2500 | V    |
| $C_{isol}$      | isolation capacitance | from main terminal 2 to external heatsink; f = 1 MHz; T <sub>n</sub> = 25 °C                                                            | -   | 10  | -    | pF   |

## 10. Characteristics

Table 7. Characteristics

| Symbol                         | Parameter                             | Conditions                                                                                                                              | Min  | Typ | Max | Unit             |
|--------------------------------|---------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|------|-----|-----|------------------|
| <b>Static characteristics</b>  |                                       |                                                                                                                                         |      |     |     |                  |
| $I_{GT}$                       | gate trigger current                  | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                       | -    | 5   | 35  | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                       | -    | 8   | 35  | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                       | -    | 11  | 35  | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                       | -    | 30  | 70  | mA               |
| $I_L$                          | latching current                      | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>                       | -    | 7   | 20  | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>                       | -    | 16  | 30  | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>                       | -    | 5   | 20  | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>                       | -    | 7   | 30  | mA               |
| $I_H$                          | holding current                       | $V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>                                                         | -    | 5   | 15  | mA               |
| $V_T$                          | on-state voltage                      | $I_T = 5\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>                                                         | -    | 1.4 | 1.7 | V                |
| $V_{GT}$                       | gate trigger voltage                  | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ;<br><a href="#">Fig. 11</a>                              | -    | 0.7 | 1   | V                |
|                                |                                       | $V_D = 400\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 125\text{ }^\circ\text{C}$ ;<br><a href="#">Fig. 11</a>                            | 0.25 | 0.4 | -   | V                |
| $I_D$                          | off-state current                     | $V_D = 600\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$                                                                                | -    | 0.1 | 0.5 | mA               |
| <b>Dynamic characteristics</b> |                                       |                                                                                                                                         |      |     |     |                  |
| $dV_D/dt$                      | rate of rise of off-state voltage     | $V_{DM} = 402\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit | 100  | 250 | -   | V/ $\mu\text{s}$ |
| $dV_{com}/dt$                  | rate of change of commutating voltage | $V_D = 400\text{ V}$ ; $T_j = 95\text{ }^\circ\text{C}$ ; $dI_{com}/dt = 1.8\text{ A/ms}$ ; $I_T = 4\text{ A}$ ; gate open circuit      | -    | 50  | -   | V/ $\mu\text{s}$ |
| $t_{gt}$                       | gate-controlled turn-on time          | $I_{TM} = 6\text{ A}$ ; $V_D = 600\text{ V}$ ; $I_G = 0.1\text{ A}$ ; $dI_G/dt = 5\text{ A}/\mu\text{s}$                                | -    | 2   | -   | $\mu\text{s}$    |





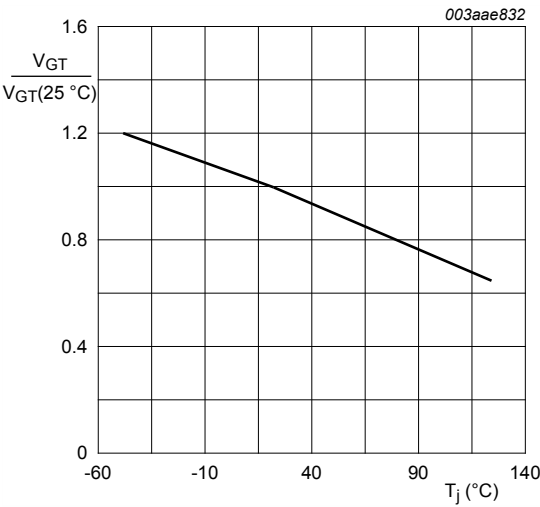


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

# 11. Package outline

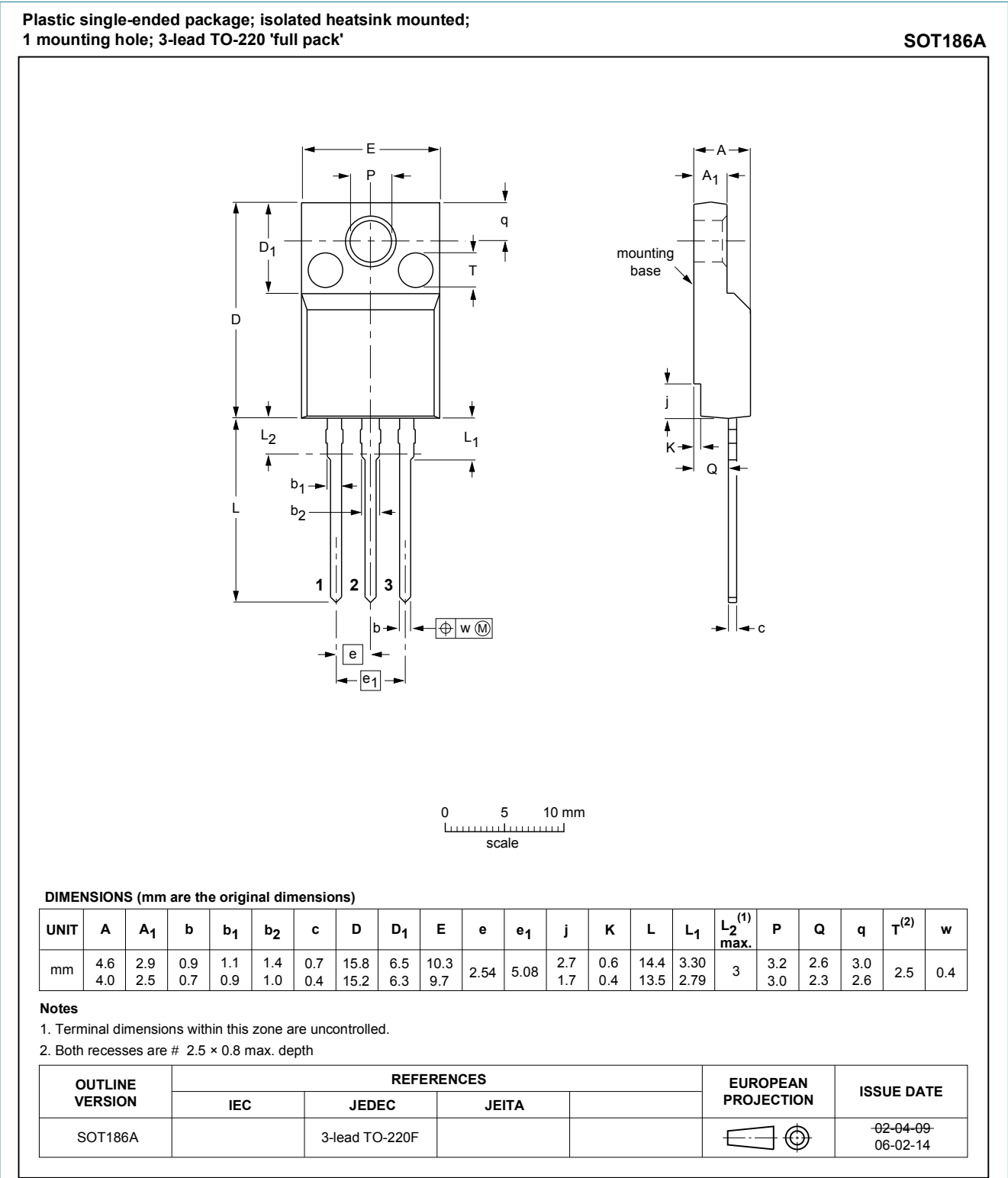


Fig. 12. Package outline TO-220F (SOT186A)

## 12. Legal information

### 12.1 Data sheet status

| Document status [1][2]         | Product status [3] | Definition                                                                            |
|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
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