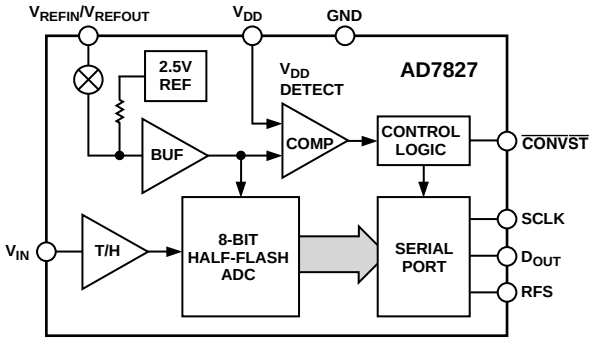
3 V/5 V, 1 MSPS, 8-Bit, Serial Interface Sampling ADC

AD7827

FEATURES

8-Bit Half-Flash ADC with 420 ns Conversion Time
200 ns Acquisition Time
8-Lead Package
On-Chip Track-and-Hold
On-Chip 2.5 V Reference with 2% Tolerance
Operating Supply Range: 3 V ± 10% and 5 V ± 10%
Specifications @ 3 V and 5 V
DSP/Microcontroller Compatible Serial Interface
Automatic Power-Down at End of Conversion
Input Ranges
0 V to 2 V, V_{DD} = 3 V
0 V to 2.5 V, V_{DD} = 5 V

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7827 is a high speed, single channel, low power, analog-to-digital converter with a maximum throughput of 1 MSPS that operates from a single 3 V or 5 V supply. The AD7827 contains a track/hold amplifier, an on-chip 2.5 V reference (2% tolerance), a 420 ns 8-bit half-flash ADC and a serial interface. The serial interface is compatible with the serial interfaces of most DSPs (Digital Signal Processors). The throughput rate of the AD7827 is dependent on the clock speed of the DSP serial interface.

The AD7827 combines the Convert Start and Power Down signals at one pin, i.e., the $\overline{\text{CONVST}}$ pin. This allows a unique automatic power-down at the end of a conversion to be implemented. The logic level on the $\overline{\text{CONVST}}$ pin is sampled at the end of a conversion and, depending on its state, the AD7827 powers down.

The AD7827 has one single-ended analog input with an input span determined by the supply voltage. With a V_{DD} of 3 V, the input range of the AD7827 is 0 V to 2 V and with V_{DD} equal to 5 V, the input range is 0 V to 2.5 V.

The parts are available in a small, 8-lead, 0.3" wide, plastic dual-in-line package (DIP) and an 8-lead, small outline IC (SOIC).

PRODUCT HIGHLIGHTS

1. Fast Conversion Time
   The AD7827 has a conversion time of 420 ns. Faster conversion times maximize the DSP processing time in a real time system.
2. Built-In Track-and-Hold
   The analog input signal is held and a new conversion is initiated on the falling edge of the $\overline{\text{CONVST}}$ signal. The $\overline{\text{CONVST}}$ signal allows the sampling instant to be exactly controlled. This feature is a requirement in many DSP applications.
3. Automatic Power-Down
   The $\overline{\text{CONVST}}$ signal is sampled approximately 100 ns after the end of conversion and depending on its state the AD7827 is powered down.
4. An easy to use, fast serial interface allows direct interfacing to most popular DSPs with no external circuitry.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD7827–SPECIFICATIONS (V_{DD} = +3 V ± 10%, V_{DD} = +5 V ± 10%, GND = 0 V, $V_{REFIN/REFOUT}$ = 2.5 V. All specifications –40°C to +105°C unless otherwise noted.)

Parameter	Version B	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 30 kHz; f_{SAMPLE} = 1 MHz
Signal-to-(Noise + Distortion) Ratio[1]	48	dB min	
Total Harmonic Distortion[1]	–55	dB max	
Peak Harmonic or Spurious Noise[1]	–55	dB max	
Intermodulation Distortion[1]			fa = 29.1 kHz; fb = 29.9 kHz
2nd Order Terms	–65	dB typ	
3rd Order Terms	–65	dB typ	
DC ACCURACY			
Resolution	8	Bits	
Integral Nonlinearity (INL)[1]	±0.5	LSB max	
Differential Nonlinearity (DNL)[1]	±0.5	LSB max	
Offset Error[1]	±1.5	LSB max	
Gain Error[1]	±2	LSB max	
Minimum Resolution for Which			
No Missing Codes are Guaranteed	8	Bits	
ANALOG INPUT[2]			
Input Voltage Range	0	V min	V_{DD} = 5 V
	2.5	V max	
	0	V min	V_{DD} = 3 V
	2	V max	
Input Leakage Current	±1	µA max	
Input Capacitance	10	pF max	
REFERENCE INPUT			
$V_{REFIN}/_{REFOUT}$ Input Voltage Range	2.55	V max	
	2.45	V min	
Input Current	±1	µA typ	
	±50	µA max	
LOGIC INPUTS			
$\overline{CONVST}$, SCLK			
$V_{INH,}$ Input High Voltage	2.4	V min	V_{DD} = 5 V ± 10%
$V_{INL,}$ Input Low Voltage	0.8	V max	V_{DD} = 5 V ± 10%
$V_{INH,}$ Input High Voltage	2.0	V min	V_{DD} = 3 V ± 10%
$V_{INL,}$ Input Low Voltage	0.4	V max	V_{DD} = 3 V ± 10%
Input Current, I_{INH}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance	10	pF max	
LOGIC OUTPUTS			
D_{OUT}, RFS			
$V_{OH,}$ Output High Voltage			I_{SOURCE} = 200 µA
	4	V max	V_{DD} = 5 V ± 10%
	2.4	V min	V_{DD} = 3 V ± 10%
$V_{OL,}$ Output Low Voltage			I_{SINK} = 200 µA
	0.4	V max	V_{DD} = 5 V ± 10%
	0.2	V min	V_{DD} = 3 V ± 10%
High Impedance Leakage Current	±1	µA max	
High Impedance Capacitance	15	pF max	
CONVERSION RATE			
Conversion Time	420	ns max	
Track/Hold Acquisition Time	200	ns max	

Parameter	Version B	Units	Test Conditions/Comments
POWER SUPPLY			
V_{DD}	4.5	V min	5 V ± 10% For Specified Performance
	5.5	V max	
	2.7	V min	3 V ± 10% For Specified Performance
	3.3	V max	
I_{DD}			
Normal Operation	10	mA max	8 mA Typically
Power-Down	1	μA max	Logic Inputs = 0 V or V_{DD}
Power Dissipation			V_{DD} = 3 V
Normal Operation	30	mW max	Typically 24 mW
Power-Down			
200 kSPS	9.58	mW max	
1 MSPS	47.88	mW max	

NOTES
[1]See Terminology section of this data sheet.
[2]Refer to the Analog Input section for an explanation of the Analog Input(s).
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] ($V_{REFIN/REFOUT}$ = 2.5 V, all specifications –40°C to +105°C, unless otherwise noted)

Parameter	5 V ± 10%	3 V ± 10%	Units	Conditions/Comments
$t_{CONVERT}$	420	420	ns max	Conversion Time.
t_1	20	20	ns min	Minimum $\overline{CONVST}$ Pulsewidth.
t_2	$t_{CONVERT}+t_3$	$t_{CONVERT}+t_3$	ns min	Falling edge of $\overline{CONVST}$ to falling edge of RFS.
	$t_{CONVERT}+t_3+t_7+t_8$	$t_{CONVERT}+t_3+t_7+t_8$	ns max	
t_3[3]	14	18	ns max	Rising edge of SCLK to falling edge of RFS.
t_4	14	18	ns max	Rising edge of SCLK to rising edge of RFS.
t_5[3]	20	20	ns max	Rising edge of SCLK to high impedance disabled.
t_6[3]	14	18	ns max	Rising edge of SCLK to D_{OUT} valid delay.
t_7	25	25	ns min	Minimum high SCLK pulse duration.
t_8	25	25	ns min	Minimum low SCLK pulse duration.
t_9[4]	20	20	ns min	Bus relinquish time after SCLK falling edge.
	35	35	ns max	
t_{10}	20	20	ns max	Maximum delay from falling edge $\overline{CONVST}$ to rising edge RFS if RFS reset by $\overline{CONVST}$.
t_{11}	30	30	ns min	Minimum time between end of serial read and next falling edge of $\overline{CONVST}$.
$t_{POWER-UP}$	1	1	μs max	Power-up time from rising edge of $\overline{CONVST}$ using external 2.5 V reference.
$t_{POWER-UP}$	25	25	μs max	Power-up time from rising edge of $\overline{CONVST}$ using on-chip reference.

NOTES
[1]Sample tested to ensure compliance.
[2]See Figures 13, 14 and 15.
[3]Measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V with V_{DD} = 5 V ± 10% and time required for an output to cross 0.4 V or 2.0 V with V_{DD} = 3 V ± 10%.
[4]Derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_9, quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

Specifications subject to change without notice.

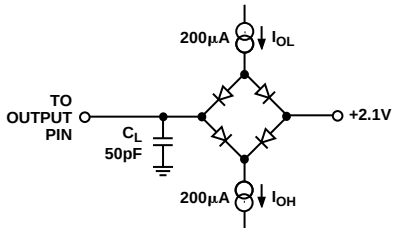


Figure 1. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND ..... –0.3 V to +7 V
Digital Input Voltage to GND
($\overline{CONVST}$, SCLK) ..... –0.3 V, V_{DD} + 0.3 V
Digital Output Voltage to GND
(D_{OUT}, RFS) ..... –0.3 V, V_{DD} + 0.3 V
V_{REF} to GND ..... –0.3 V, V_{DD} + 0.3 V
Analog Input Voltage to AGND ..... –0.3 V, V_{DD} + 0.3 V
Operating Temperature Range
Industrial (B Version) ..... –40°C to +105°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Plastic DIP Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... +105°C/W
Lead Temperature, (Soldering 10 sec) ..... +260°C
SOIC Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... +75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C
ESD ..... 2.0 kV

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

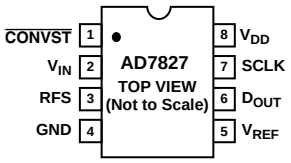
ORDERING GUIDE

Model	Linearity Error (LSB)	Package Description	Package Option
AD7827BN	±0.5 LSB	Plastic DIP	N-8
AD7827BR	±0.5 LSB	Small Outline IC	SO-8

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	$\overline{CONVST}$	Convert Start. Puts the track-and-hold into hold mode and initiates a conversion. The state of this pin at the end of conversion also determines whether or not the part is powered down.
2	V_{IN}	Analog Input is applied here.
3	RFS	Receive Frame Sync. This is an output. When this signal goes logic high at the end of a conversion, the DSP starts latching in data on the next cycle of SCLK.
4	GND	Ground reference for analog and digital circuitry.
5	V_{REF}	Reference Input.
6	D_{OUT}	Serial Data is shifted out on this pin. Data is clocked out by the rising edges of SCLK.
7	SCLK	Serial Clock. An external serial clock is applied here. The clock must be continuous so the RFS (frame SYNC) can be synchronized to the clock for high speed data transfers. (See Microprocessor Interfacing section.)
8	V_{DD}	Positive Supply Voltage 3 V/5 V ± 10%.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7827 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

Signal-to-(Noise + Distortion) Ratio

This is the measured ratio of signal-to-(noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal-to-(Noise + Distortion)} = (6.02N + 1.76)\ dB$$

Thus for an 8-bit converter, this is 50 dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7827 it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7827 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Relative Accuracy

Relative accuracy or endpoint nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the 128th code transition (01111111) to (10000000) from the ideal, i.e., $V_{REF}/2$ (V_{DD} = 5 V), 0.8 $V_{REF}/2$ (V_{DD} = 3 V).

Zero Scale Error

This is the deviation of the first code transition (00000000) to (00000001) from the ideal, i.e., $V_{REF}/2$ –1.25 V + 1 LSB (V_{DD} = 5 V ± 10%), or 0.8 $V_{REF}/2$ –1.0 V + 1 LSB (V_{DD} = 3 V ± 10%).

Full-Scale Error

This is the deviation of the last code transition (11111110) to (11111111) from the ideal, i.e., V_{MID} + 1.25 V – 1 LSB (V_{DD} = 5 V ± 10%), or V_{MID} + 1.0 V – 1 LSB (V_{DD} = 3 V ± 10%).

Gain Error

This is the deviation of the last code transition (1111 . . . 110) to (1111 . . . 111) from the ideal, i.e., V_{REF} – 1 LSB, after the offset error has been adjusted out.

Track/Hold Acquisition Time

Track/hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the point at which the track/hold returns to track mode. This happens approximately 120 ns after the falling edge of $\overline{\text{CONVST}}$.

It also applies when there is a step input change on the input voltage applied to the V_{IN} input of the AD7827. It means that the user must wait for the duration of the track/hold acquisition time after the end of conversion or after a step input change to V_{IN} before starting another conversion, to ensure that the part operates to specification.

CIRCUIT DESCRIPTION

The AD7827 consists of a track-and-hold amplifier followed by a half-flash analog-to-digital converter. This device uses a half-flash conversion technique where one 4-bit flash ADC is used to achieve an 8-bit result. The 4-bit flash ADC contains a sampling capacitor followed by 15 comparators that compare the unknown input to a reference ladder to get a 4-bit result. This first flash, i.e., coarse conversion, provides the 4 MSBs. For a full 8-bit reading to be realized, a second flash, i.e., a fine conversion, must be performed to provide the 4 LSBs. The 8-bit word is then placed in the serial shift register.

Figures 2 and 3 below show simplified schematics of the ADC. When the ADC starts a conversion, the track-and-hold goes into hold mode and holds the analog input for 120 ns. This is the acquisition phase as shown in Figure 2 when Switch 2 is in Position A. At the point when the track-and-hold returns to its track mode, this signal is sampled by the sampling capacitor as Switch 2 moves into Position B. The first flash occurs at this instant and is then followed by the second flash. Typically the first flash is complete after 100 ns, i.e., at 220 ns, while the end of the second flash, and hence the 8-bit conversion result, is available at 330 ns. As shown in Figure 4 the track-and-hold returns to track mode after 120 ns, and so starts the next acquisition before the end of the current conversion. Figure 6 shows the ADC transfer function.

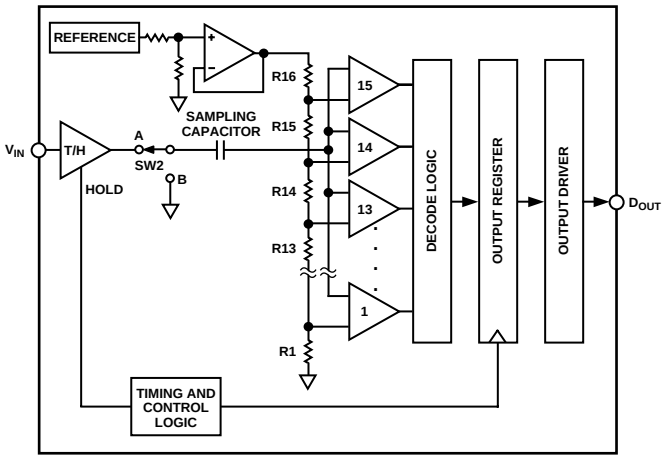


Figure 2. ADC Acquisition Phase

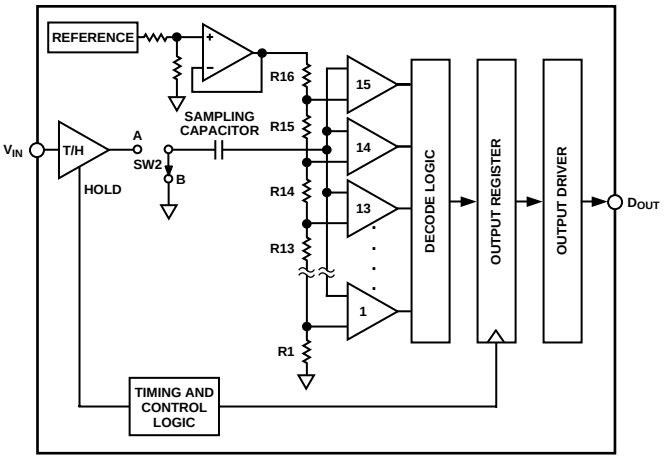


Figure 3. ADC Conversion Phase

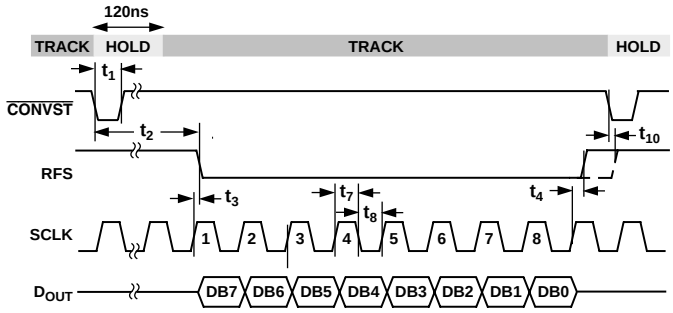


Figure 4. Track-and-Hold Timing

TYPICAL CONNECTION DIAGRAM

Figure 5 shows a typical connection diagram for the AD7827. The serial interface is implemented using three wires; the RFS is a logic output and the serial clock is continuous. The Receive Frame Sync signal (RFS) idles high, the falling edge of $\overline{\text{CONVST}}$ initiates a conversion and the first rising edge of the serial clock after the end of conversion causes the RFS signal to go low. This falling edge of RFS is used to drive the RFS on a microprocessor—see Serial Interface section for more details. V_{REF} is connected to a voltage source such as the AD780, while V_{DD} is connected to a voltage source of 3 V ± 10% or 5 V ± 10%. Due to the proximity of the $\overline{\text{CONVST}}$ and V_{IN} pins, it is recommended to use a 10 nF decoupling capacitor on V_{IN}. When V_{DD} is first connected the AD7827 powers up in a low current mode, i.e., power-down. A rising edge on the $\overline{\text{CONVST}}$ pin will cause the AD7827 to fully power up. For applications where power consumption is of concern, the automatic power-down at the end of a conversion should be used to improve power performance. See the Power-Down Options section of this data sheet.

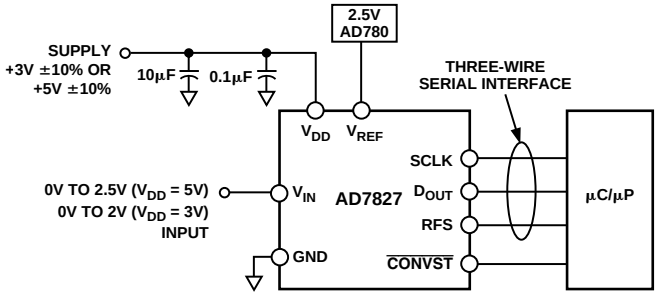


Figure 5. Typical Connection Diagram

ADC TRANSFER FUNCTION

The output coding of the AD7827 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1 LSB, 2 LSBs, etc.). The LSB size is = $V_{REF}/256$ (V_{DD} = 5 V) or the LSB size = (0.8 V_{REF})/256 (V_{DD} = 3 V). The ideal transfer characteristic for the AD7827 is shown in Figure 6 below.

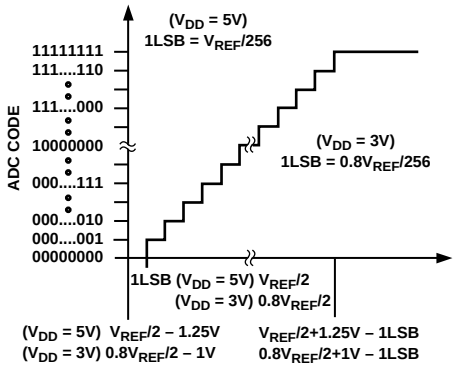


Figure 6. Transfer Characteristic

ANALOG INPUT

The AD7827 has a single input channel with an input range of 0 V to 2.5 V or 0 V to 2.0 V, depending on the supply voltage (V_{DD}). This input range is automatically set up by an on-chip "V_{DD} detector" circuit. 5 V operation of the ADC is detected when V_{DD} exceeds 4.1 V and 3 V operation is detected when V_{DD} falls below 3.8 V. This circuit also possesses a degree of glitch rejection; for example, a glitch from 5.5 V to 2.7 V up to 60 ns wide will not trip the V_{DD} detector.

Note: Although there is a V_{REF} pin from which a voltage reference of 2.5 V may be sourced, or to which an external reference may be applied, this does not provide an option of varying the value of the voltage reference. As stated in the specifications for the AD7827, the input voltage range at this pin is 2.5 V ± 2%.

Analog Input Structure

Figure 7 shows an equivalent circuit of the analog input structure of the AD7827. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 200 mV. This will cause these diodes to become forward biased and start conducting current into the substrate. The maximum current these diodes can conduct without causing irreversible damage to the part is 20 mA. The capacitor C2 in Figure 7 is typically about 4 pF and can mostly be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance of several components including that of the multiplexer and the track-and-hold. This resistor is typically about 310 Ω. The capacitor C1 is the track-and-hold capacitor and has a capacitance of 0.5 pF. Switch 1 is the track-and-hold switch, while Switch 2 is that of the sampling capacitor as shown in Figures 2 and 3.

When in track phase, Switch 1 is closed and Switch 2 is in Position A. When in hold mode, Switch 1 opens while Switch 2 remains in Position A. The track-and-hold remains in hold mode for 120 ns—see Circuit Description, after which it returns to track mode and the ADC enters its conversion phase. At this point Switch 1 opens and Switch 2 moves to Position B. At the end of the conversion Switch 2 moves back to Position A.

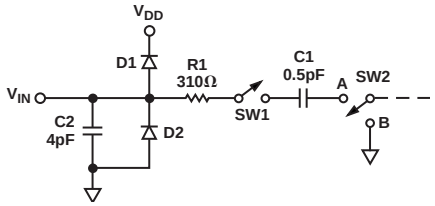


Figure 7. Equivalent Analog Input Circuit

The on-chip track-and-hold can accommodate input frequencies to 10 MHz, making the AD7827 ideal for subsampling applications. When the AD7827 is converting a 10 MHz input signal at a sampling rate of 1 MSPS, the effective number of bits typically remains above seven corresponding to a signal-to-noise ratio of 42 dBs as shown in Figure 8.

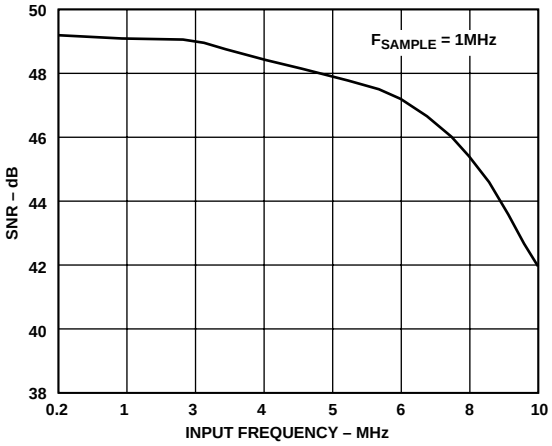


Figure 8. SNR vs. Input Frequency On the AD7827

POWER-UP TIMES

The AD7827 has a 1 µs power-up time when using an external reference and a 25 µs power-up time when using the on-chip reference. When V_{DD} is first connected, the AD7827 is in a low current mode of operation. In order to carry out a conversion the AD7827 must first be powered up. The AD7827 is powered up by a rising edge on the $\overline{\text{CONVST}}$ pin and a conversion is initiated on the falling edge of $\overline{\text{CONVST}}$. Figure 9 shows how to power up the AD7827 when V_{DD} is first connected or after the ADC has been powered down using the $\overline{\text{CONVST}}$ pin when using either the on-chip, or an external, reference. When using an external reference the falling edge of $\overline{\text{CONVST}}$ may occur before the required power-up time has elapsed; however, the conversion will not be initiated on the falling edge of $\overline{\text{CONVST}}$ but rather at the moment when the part has completely powered up, i.e., after 1 µs. If the falling edge of $\overline{\text{CONVST}}$ occurs after the required power-up time has elapsed, it is upon this falling edge that a conversion is initiated. When using the on-chip reference, it is necessary to wait the required power-up time of approximately 25 µs before initiating a conversion, i.e., a falling edge on $\overline{\text{CONVST}}$ may not occur before the required power-up time has elapsed, when V_{DD} is first connected or after the AD7827 has been powered down using the $\overline{\text{CONVST}}$ pin as shown in Figure 9.

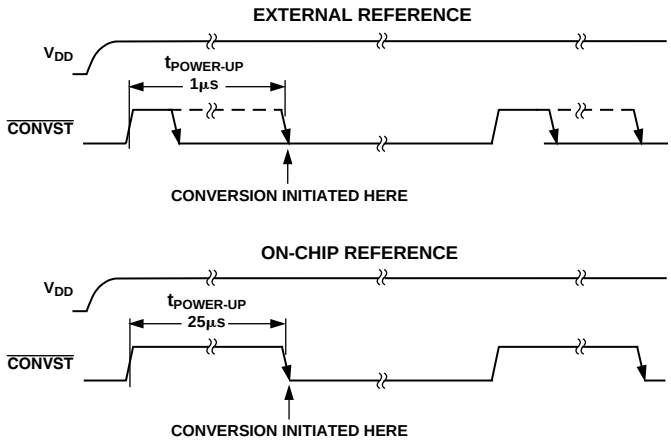


Figure 9. Power-Up Time

POWER VS. THROUGHPUT

Superior power performance can be achieved by using the automatic power-down (Mode 2) at the end of a conversion (see Operating Modes section of this data sheet).

Figure 10 shows how the automatic power-down is implemented using the $\overline{\text{CONVST}}$ signal to achieve the optimum power performance for the AD7827. The duration of the $\overline{\text{CONVST}}$ pulse is set to be equal to or less than the power-up time of the devices (see Operating Modes section). As the throughput rate is reduced, the device remains in its power-down state for longer and the average power consumption over time drops accordingly.

For example, if the AD7827 is operated in a continuous sampling mode, with a throughput rate of 100 kSPS and using an external reference, the power consumption is calculated as follows. The power dissipation during normal operation is 30 mW, V_{DD} = 3 V.

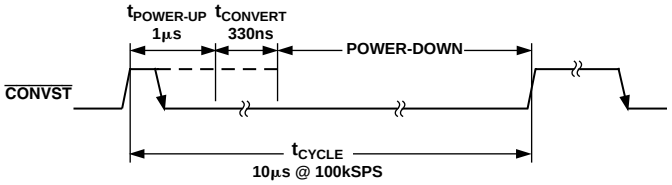


Figure 10. Automatic Power-Down

If the power-up time is 1 µs and the conversion time is 330 ns (@ 25°C), the AD7827 can be said to dissipate 30 mW for 1.33 µs (worst case) during each conversion cycle. If the throughput rate is 100 kSPS, the cycle time is 10 µs and the average power dissipated during each cycle is (1.33/10) × (30 mW) = 3.99 mW.

Figure 11 shows the Power vs. Throughput rate for automatic full power-down.

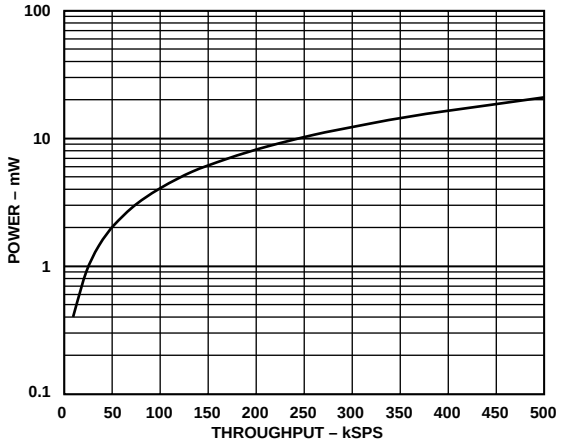


Figure 11. Power vs. Throughput

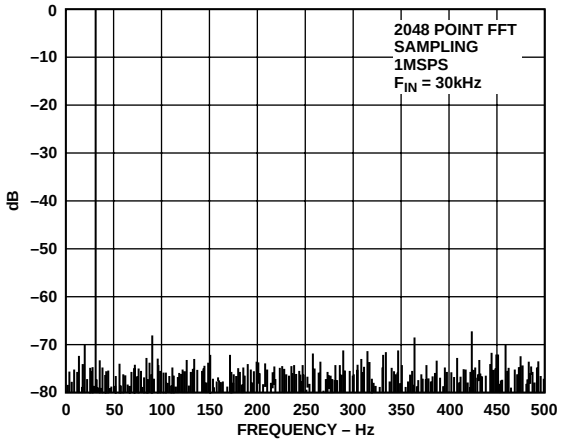


Figure 12. AD7827 SNR

OPERATING MODES

The AD7827 has two possible modes of operation depending on the state of the $\overline{\text{CONVST}}$ pulse at the end of a conversion.

Mode 1 Operation (High Speed Sampling)

When the AD7827 is operated in Mode 1 the device is not powered down between conversions. This mode of operation allows high throughput rates to be achieved. Figure 13 shows how this optimum throughput rate is achieved by bringing $\overline{\text{CONVST}}$ high before the end of the conversion. When operating in this mode, a new conversion should not be initiated until 30 ns after the end of a read operation. This is to allow the track/hold to acquire the analog signal to 0.5 LSB accuracy.

Mode 2 Operation (Automatic Power-Down)

When the AD7827 is operated in Mode 2 (see Figure 14) it automatically powers down 530 ns after the falling edge of $\overline{\text{CONVST}}$. The $\overline{\text{CONVST}}$ signal is brought low to initiate a conversion and is left logic low until 530 ns has elapsed after the falling edge of the $\overline{\text{CONVST}}$ pulse, i.e., before Point A or Point B in Figure 14, depending on the actual value of t_2 (see Timing Characteristics). The state of the $\overline{\text{CONVST}}$ signal is sampled at this point (i.e., 530 ns after $\overline{\text{CONVST}}$ falling edge) and the AD7827 will power down as long as the $\overline{\text{CONVST}}$ is low. The ADC is powered up again on the rising edge of the $\overline{\text{CONVST}}$ signal. The $\overline{\text{CONVST}}$ pulse width does not have to be as long as the power-up time if an external reference is used (see Power-Up Times section). Superior power performance can be achieved in this mode of operation by powering up the AD7827 to only carry out a conversion. The serial interface of the AD7827 is still fully operational while the device is powered down.

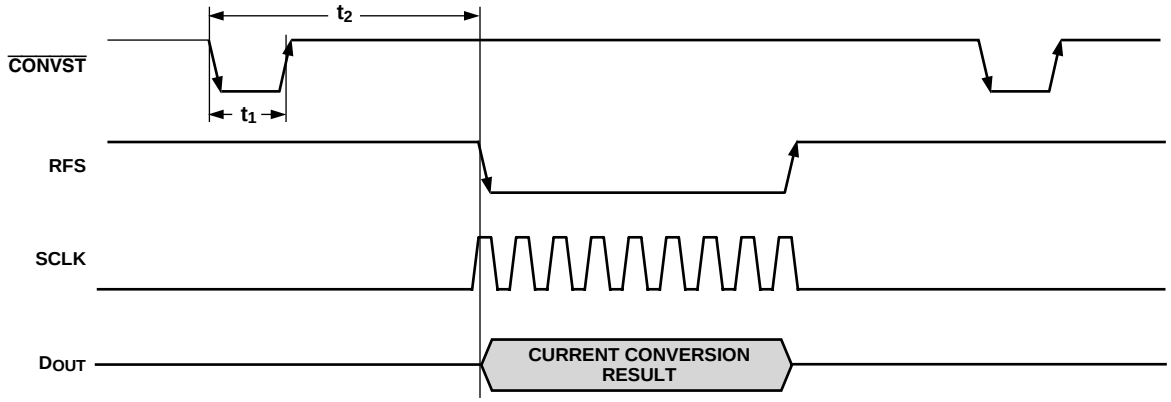


Figure 13. Mode 1 Operation Timing Diagram

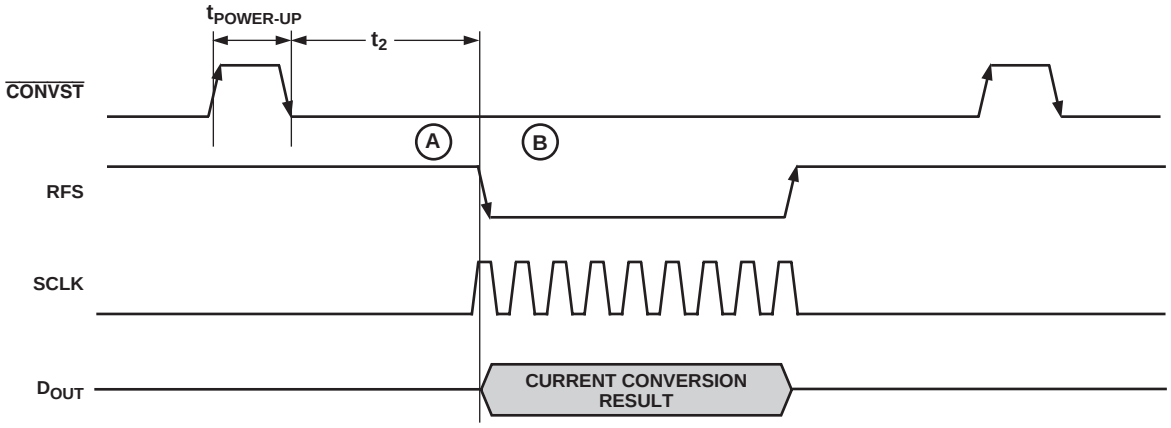


Figure 14. Mode 2 Operation Timing Diagram

AD7827 SERIAL INTERFACE

In order to achieve a high throughput rate, the serial port of the AD7827 has been optimized for high speed serial protocols. Many high speed serial protocols use a continuous serial clock to transfer data, e.g., the serial ports of many popular DSPs like the TMS320C5x, ADSP-21xx and DSP560xx. The serial interface of the AD7827 is optimized for communication with such devices.

The serial interface of the AD7827 uses a three-wire interface to communicate with a Master. The serial clock pin (SCLK) is a logic input and determines the bit transfer rate. The Receive Frame Synchronization pin (RFS) is a logic output and used to synchronize the data with a continuous serial clock. The data output pin (D_{OUT}) is a logic output and serial data is shifted out onto this pin on the rising edge of the serial clock. The first rising edge of the serial clock after the end of a conversion causes the RFS pin to go logic low. (See Figure 15 below.) The D_{OUT} pin leaves its high impedance state and the first MSB is shifted out on the first SCLK rising edge after the end of conversion. The remaining seven data bits are shifted out on subsequent SCLK rising edges. The D_{OUT} pin enters its high impedance state again on the falling edge of the eighth SCLK after RFS goes low. The RFS output goes high again on the rising edge of the ninth SCLK. If the AD7827 does not receive a ninth SCLK, the RFS will be reset logic high by the next falling edge of $\overline{\text{CONVST}}$.

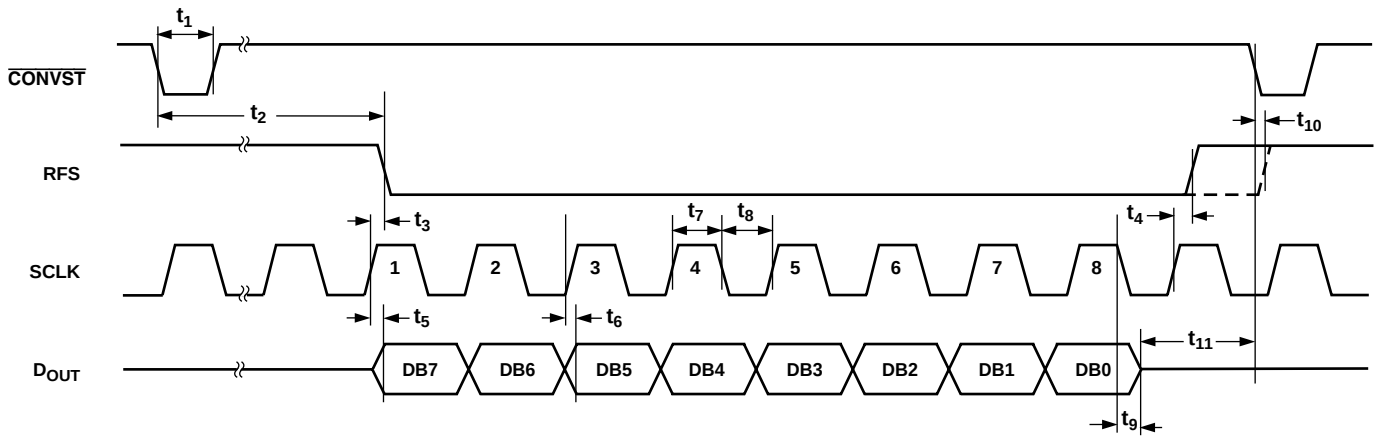


Figure 15. Serial Timing

MICROPROCESSOR INTERFACING

The Serial Interface on the AD7827 allows the part to be connected directly to a range of many different microprocessors and microcontrollers. This section explains how to interface the AD7827 with some of the more common DSP serial interface protocols.

AD7827 to TMS320C5x

The serial interface on the TMS320C5x uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices such as the AD7827. A receive frame synchronization output has been supplied on the AD7827 to allow easy interfacing with no extra gluing logic. The serial port of the TMS320C5x is set up to operate in Burst Mode with internal CLKX (TX serial clock) and FSR (RX frame sync). The Serial Port Control register (SPC) must have the following setup: F0 = 1, FSM = 1, MCM = 1. The connection diagram is shown in Figure 16.

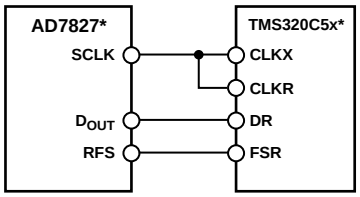


Figure 16. Interfacing to the TMS320C5x

AD7827 to ADSP-21xx

The ADSP-21xx family of DSPs are easily interfaced to the AD7827 without the need for any extra gluing logic. The SPORT is operated in alternate framing mode. The SPORT control register should be set up as follows:

TFSW = RFSW = 1, Alternate Framing
INVRFS = INVTFS = 1, Active Low Frame Signal
DTYPE = 00, Right Justify Data
SLEN = 0111, 8-Bit Data Words
ISCLK = 1, Internal Serial Clock
TFSR = RFSR = 1, Frame Every Word
IRFS = 0, External Framing Signal
ITFS = 1, Internal Framing Signal

The 8-bit data words will be right justified in the 16-bit serial data registers when using this configuration. Figure 17 shows the connection diagram.

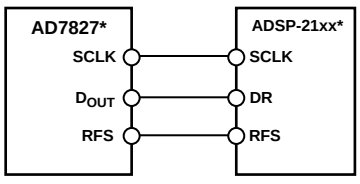


Figure 17. Interfacing to the ADSP-21xx

AD7827 to DSP56xxx

The connection diagram in Figure 18 shows how the AD7827 can be connected to the SSI (Synchronous Serial Interface) of the DSP56xxx family of DSPs from Motorola. The SSI is operated in Synchronous Mode (SYN bit in CRB = 1) with internally generated 1-bit clock period frame sync for both TX and RX (FSL1 and FSL0 bits in CRB = 1 and 0 respectively).

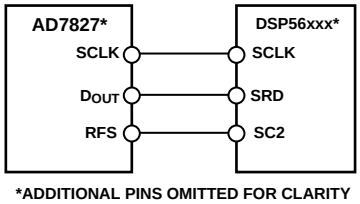


Figure 18. Interfacing to the DSP56xxx

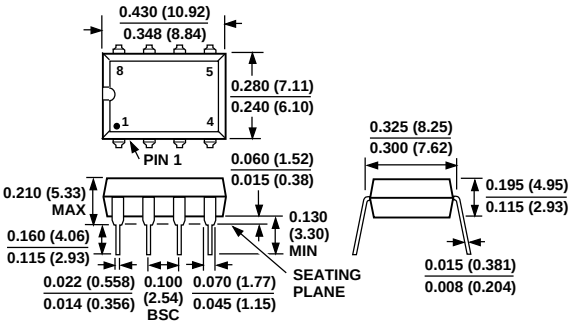
Microcontrollers

The AD7827 may also be interfaced to many microcontrollers, as a continuous serial clock is not essential. However, enough time must be left for the conversion to be complete before applying a burst of serial clocks to read out the data.

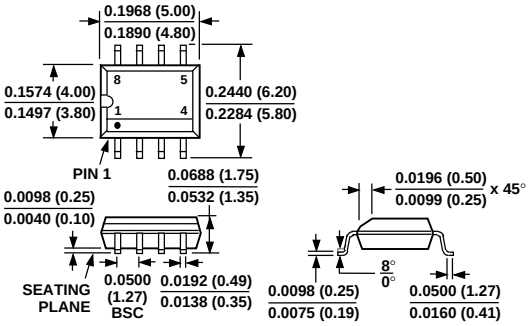
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP
(N-8)



8-Lead Small Outline Package
(SO-8)



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