



THIS SPEC IS OBSOLETE

Spec No: 001-06497

Spec Title: CY62137VN MOBL(R) 2-MBIT (128K X 16)
STATIC RAM

Sunset Owner: Anuj Chakrapani (aju)

Replaced by: NONE

2-Mbit (128K x 16) Static RAM

Features

- **Temperature Ranges**
 - Automotive-A: -40°C to 85°C
 - Automotive-E: -40°C to 125°C
- **High Speed: 70 ns**
- **Wide voltage range: 2.7V–3.6V**
- **Ultra-low active, standby power**
- **Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in Pb-free 44-pin TSOP Type II package**

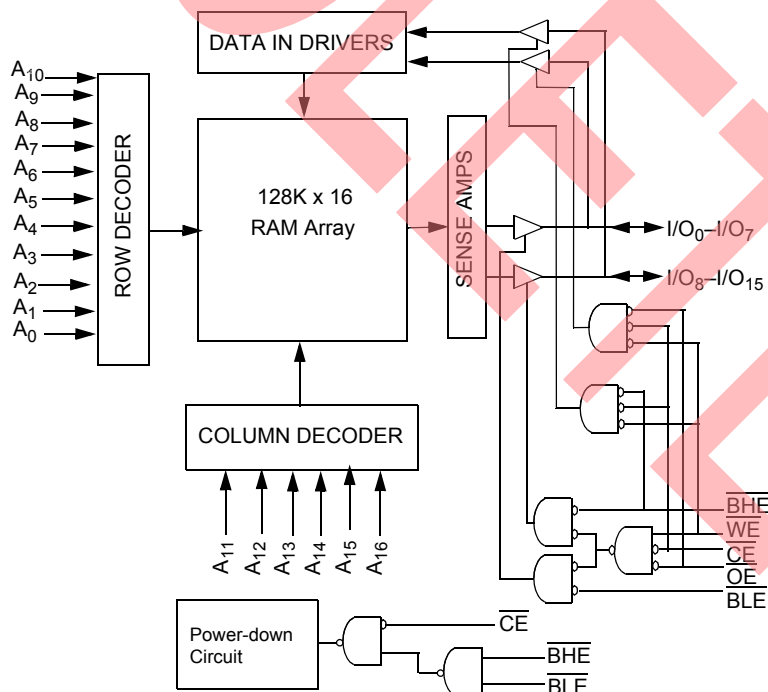
Functional Description

The CY62137VN is a high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that reduces power

consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{\text{CE}}$ HIGH) or when $\overline{\text{CE}}$ is LOW and both BLE and BHE are HIGH. The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{\text{CE}}$ HIGH), outputs are disabled ($\overline{\text{OE}}$ HIGH), BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation ($\overline{\text{CE}}$ LOW, and WE LOW). Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}). Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the truth table at the back of this data sheet for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note [AN1064](#), [SRAM System Guidelines](#).

Logic Block Diagram



Product Portfolio

Product		V _{CC} Range (V)			Speed (ns)	Power Dissipation			
						Operating, I _{CC} (mA)		Standby, I _{SB2} (μA)	
		Min.	Typ. ^[2]	Max.		Typ. ^[2]	Max.	Typ. ^[2]	Max.
CY62137VNLL	Automotive-A	2.7	3.0	3.6	70	7	15	1	15
CY62137VNLL	Automotive-E				70	7	15	1	20

Pin Configurations

TSOP II (Forward)
Top View

A ₄	1	44	A ₅
A ₃	2	43	A ₆
A ₂	3	42	A ₇
A ₁	4	41	OE
A ₀	5	40	BHE
$\overline{\text{CE}}$	6	39	BLE
I/O ₀	7	38	I/O ₁₅
I/O ₁	8	37	I/O ₁₄
I/O ₂	9	36	I/O ₁₃
I/O ₃	10	35	I/O ₁₂
V _{CC}	11	34	V _{SS}
V _{SS}	12	33	V _{CC}
I/O ₄	13	32	I/O ₁₁
I/O ₅	14	31	I/O ₁₀
I/O ₆	15	30	I/O ₉
I/O ₇	16	29	I/O ₈
WE	17	28	NC
A ₁₆	18	27	A ₈
A ₁₅	19	26	A ₉
A ₁₄	20	25	A ₁₀
A ₁₃	21	24	A ₁₁
A ₁₂	22	23	NC

Pin Definitions

Pin Number	Type	Description
1–5, 18–22, 24–27, 42–45	Input	A ₀ –A ₁₆ . Address Inputs
7–10, 13–16, 29–32, 35–38	Input/Output	I/O ₀ –I/O ₁₅ . Data lines. Used as input or output lines depending on operation
23	No Connect	NC. This pin is not connected to the die
17	Input/Control	WE. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted
6	Input/Control	CE. When LOW, selects the chip. When HIGH, deselects the chip
40, 39	Input/Control	Byte Write Select Inputs, active LOW. BHE controls I/O ₁₅ –I/O ₈ , BLE controls I/O ₇ –I/O ₀ .
41	Input/Control	OE. Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins
12, 34	Ground	V _{SS} . Ground for the device
11, 33	Power Supply	V _{CC} . Power supply for the device

Notes:

1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(TYP)}, T_A = 25°C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage to Ground Potential -0.5V to +4.6V

DC Voltage Applied to Outputs
in High-Z State^[3] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[3] -0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Automotive-A	-40°C to +85°C	2.7V to 3.6V
Automotive-E	-40°C to +125°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-70			Unit	
			Min.	Typ. ^[2]	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = 2.7V, I _{OH} = −1.0 mA	2.4			V	
V _{OL}	Output LOW Voltage	V _{CC} = 2.7V, I _{OL} = 2.1 mA			0.4	V	
V _{IH}	Input HIGH Voltage		2.2		V _{CC} + 0.5V	V	
V _{IL}	Input LOW Voltage		−0.5		0.8	V	
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	−1		+1	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	−1		+1	μA	
I _{CC}	V _{CC} Operating Supply Current	I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC} , CMOS Levels	V _{CC} = 3.6V	Auto-A/ Auto-E	7	15	mA
		I _{OUT} = 0 mA, f = 1 MHz, CMOS Levels		Auto-A/ Auto-E	1	2	
I _{SB1}	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} − 0.3V or V _{IN} ≤ 0.3V, f = f _{MAX}	V _{CC} = 3.6V	Auto-A/ Auto-E		100	μA
I _{SB2}	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ V _{IN} ≥ V _{CC} − 0.3V or V _{IN} ≤ 0.3V, f = 0	V _{CC} = 3.6V	Auto-A	1	15	μA
				Auto-E	1	20	

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ C, f = 1\text{ MHz}$, $V_{CC} = V_{CC(typ)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance^[4]

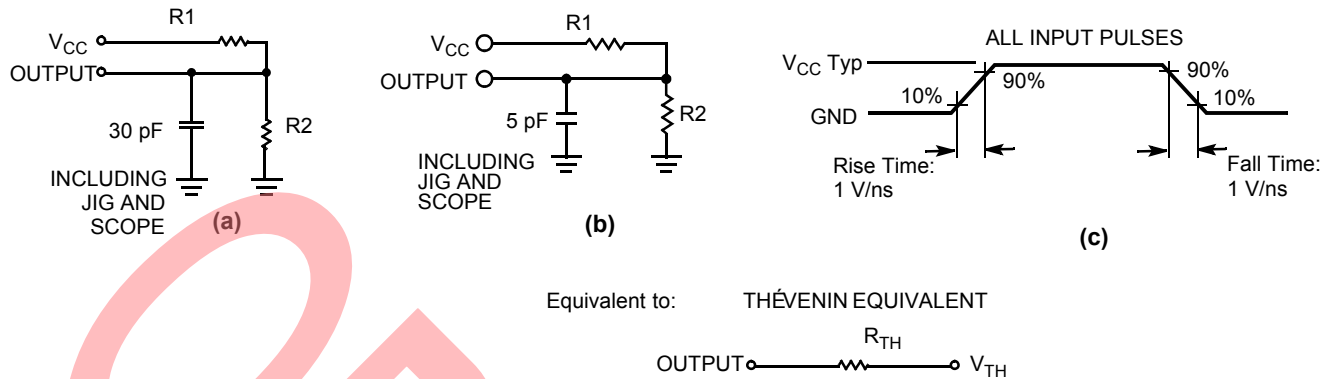
Parameter	Description	Test Conditions	TSOPII	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 2-layer printed circuit board	60	$^\circ C/W$
Θ_{JC}	Thermal Resistance (Junction to Case)		22	$^\circ C/W$

Notes:

3. $V_{IL(min.)} = -2.0V$ for pulse durations less than 20 ns.

4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

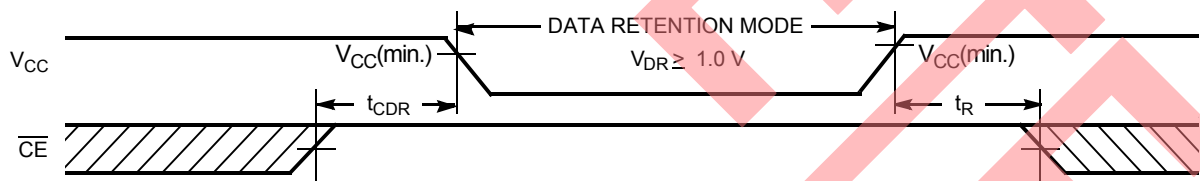


Parameters	Value	Unit
R1	1105	Ohms
R2	1550	Ohms
R_{TH}	645	Ohms
V_{TH}	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0			V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.0V, \overline{CE} \geq V_{CC} - 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V;$ No input may exceed $V_{CC} + 0.3V$	Auto-A	0.5	7.5	μA
			Auto-E		10	
$t_{CDR}^{[4]}$	Chip Deselect to Data Retention Time		0			ns
t_R	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform



Switching Characteristics Over the Operating Range ^[5]

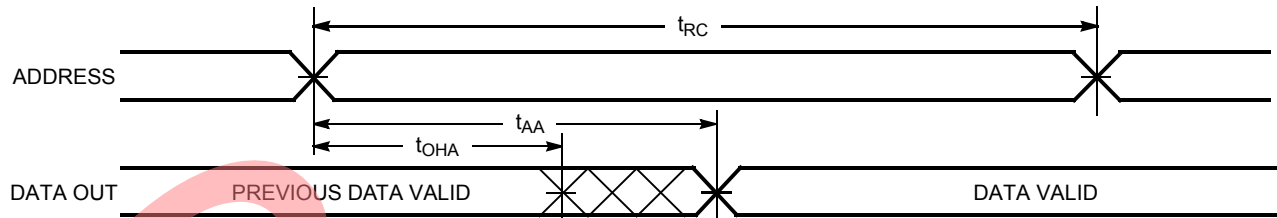
Parameter	Description	70 ns		Unit
		Min.	Max.	
Read Cycle				
t _{RC}	Read Cycle Time	70		ns
t _{AA}	Address to Data Valid		70	ns
t _{OHA}	Data Hold from Address Change	10		ns
t _{ACE}	\overline{CE} LOW to Data Valid		70	ns
t _{DOE}	\overline{OE} LOW to Data Valid		35	ns
t _{LZOE}	\overline{OE} LOW to Low-Z ^[6]	5		ns
t _{HZOE}	\overline{OE} HIGH to High-Z ^[6, 7]		25	ns
t _{LZCE}	\overline{CE} LOW to Low-Z ^[6]	10		ns
t _{HZCE}	\overline{CE} HIGH to High-Z ^[6, 7]		25	ns
t _{PU}	\overline{CE} LOW to Power-up	0		ns
t _{PD}	\overline{CE} HIGH to Power-down		70	ns
t _{DBE}	\overline{BHE} / \overline{BLE} LOW to Data Valid		70	ns
t _{LZBE} ⁽⁸⁾	\overline{BHE} / \overline{BLE} LOW to Low-Z	5		ns
t _{HZBE}	\overline{BHE} / \overline{BLE} HIGH to High-Z		25	ns
Write Cycle ^[9, 10]				
t _{WC}	Write Cycle Time	70		ns
t _{SCE}	\overline{CE} LOW to Write End	60		ns
t _{AW}	Address Set-up to Write End	60		ns
t _{HA}	Address Hold from Write End	0		ns
t _{SA}	Address Set-up to Write Start	0		ns
t _{PWE}	\overline{WE} Pulse Width	50		ns
t _{SD}	Data Set-up to Write End	30		ns
t _{HD}	Data Hold from Write End	0		ns
t _{HZWE}	\overline{WE} LOW to High-Z ^[6, 7]		25	ns
t _{LZWE}	\overline{WE} HIGH to Low-Z ^[6]	10		ns
t _{BW}	\overline{BHE} / \overline{BLE} LOW to End of Write	60		ns

Notes:

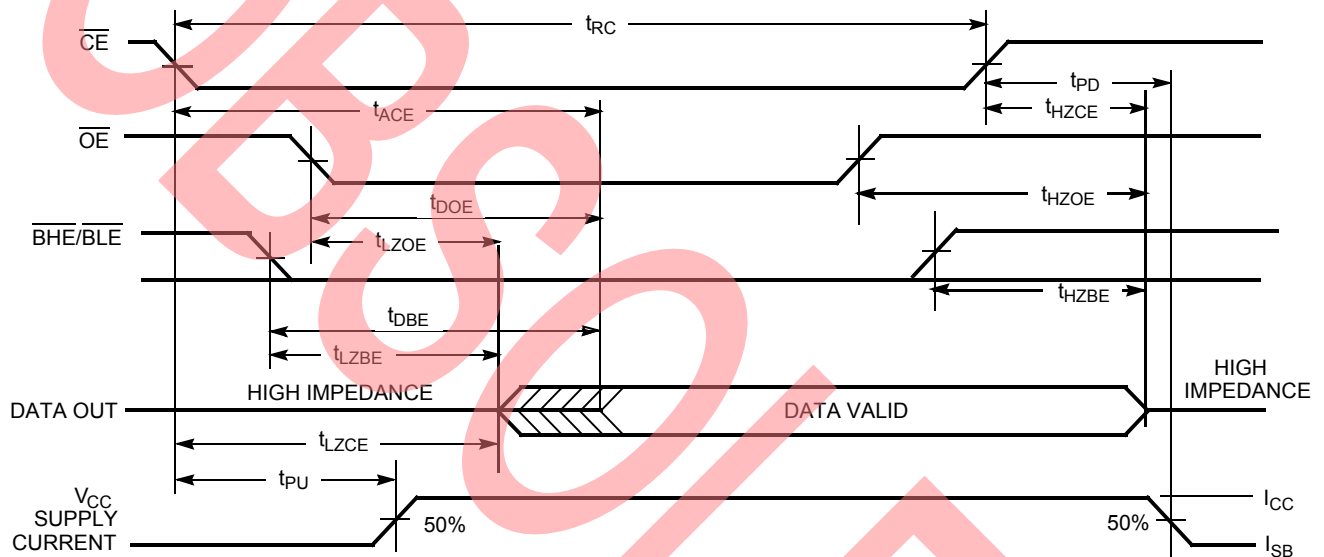
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to V_{CC} typ., and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- If both byte enables are toggled together this value is 10 ns.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Read Cycle No. 1^[11, 12]



Read Cycle No. 2^[12, 13]

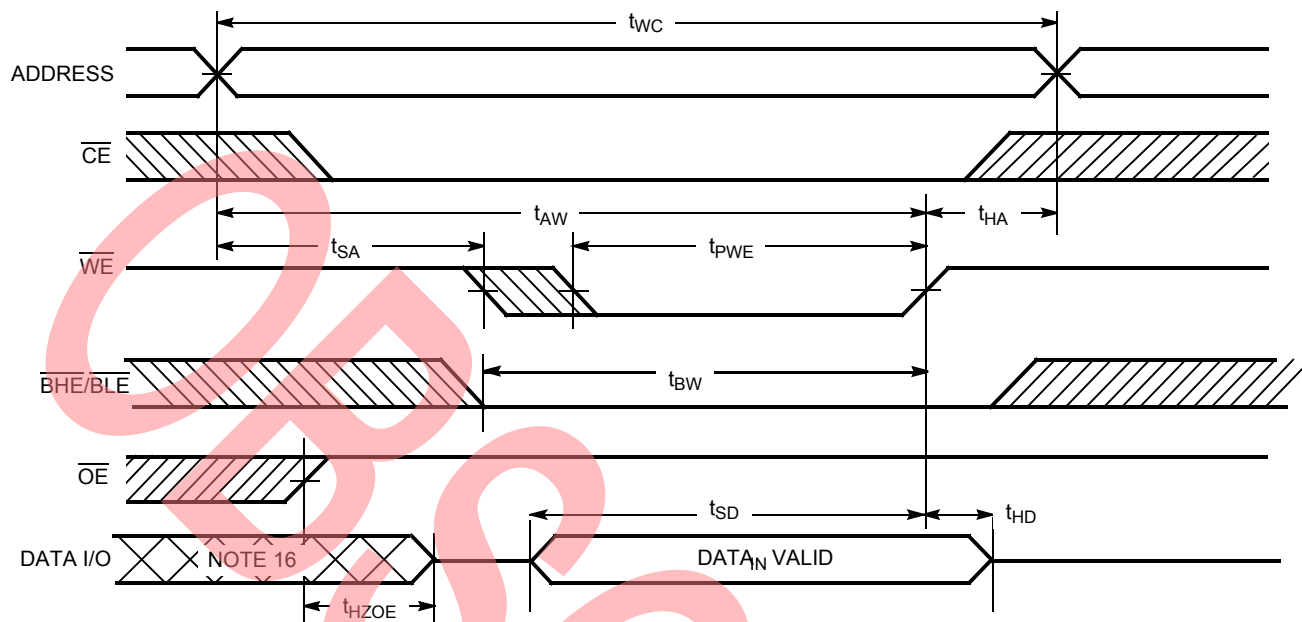


Notes:

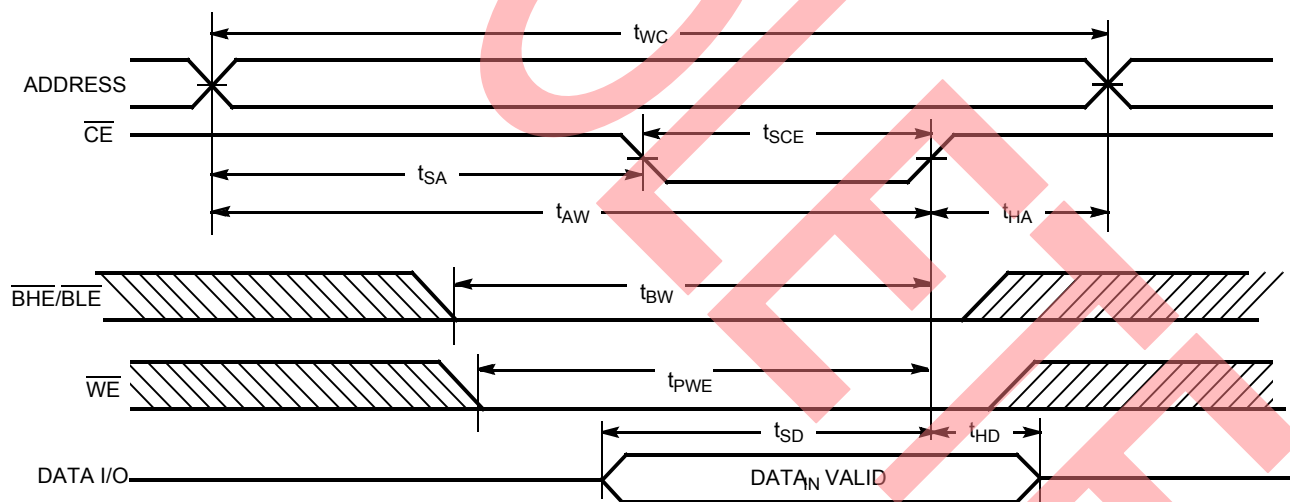
11. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
12. \overline{WE} is HIGH for read cycle.
13. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled)^[9, 14, 15]



Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)^[9, 14, 15]

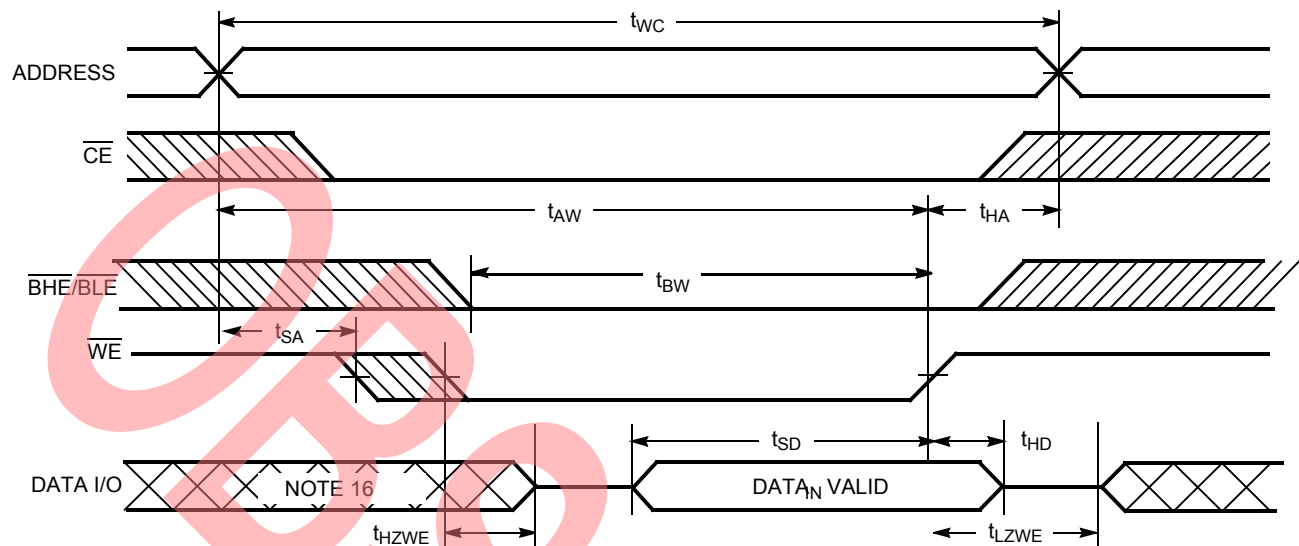


Notes:

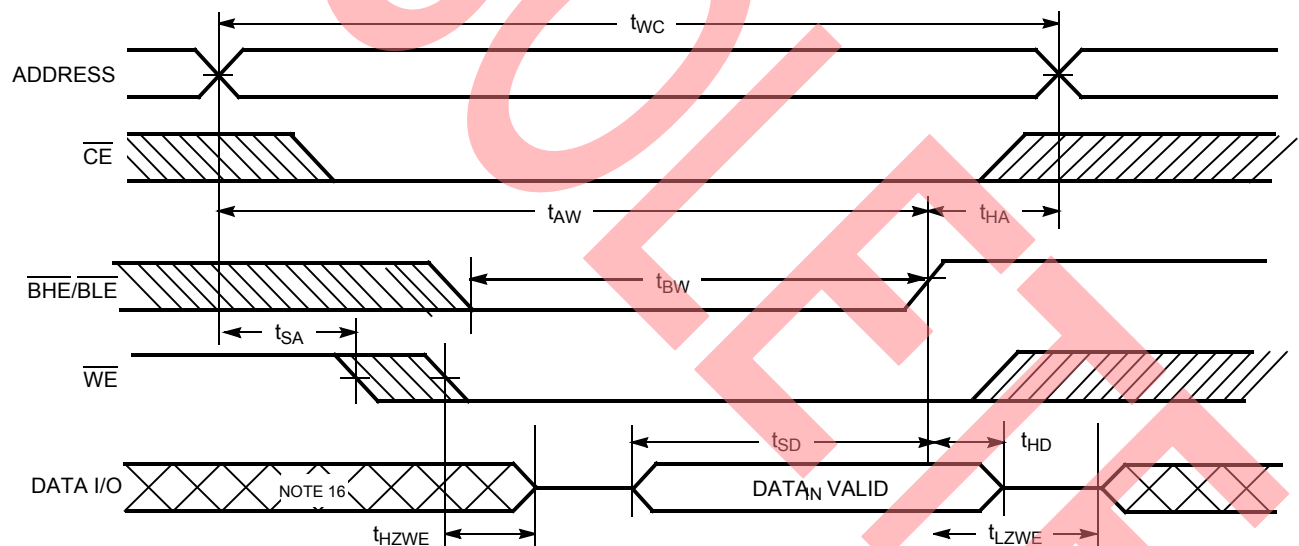
14. Data I/O is high-impedance if $\overline{\text{OE}} = V_{\text{IH}}$.
15. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.
16. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

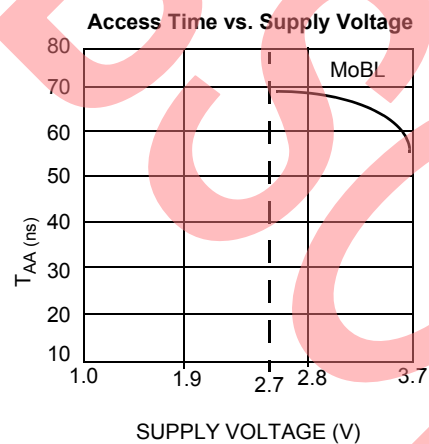
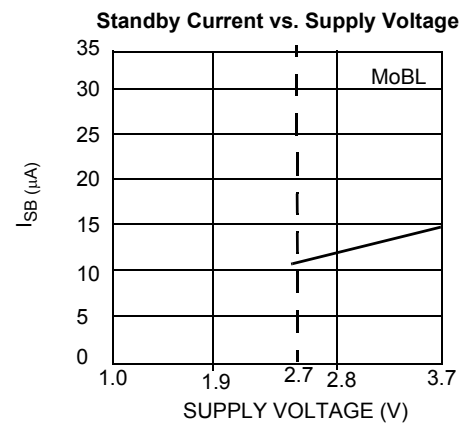
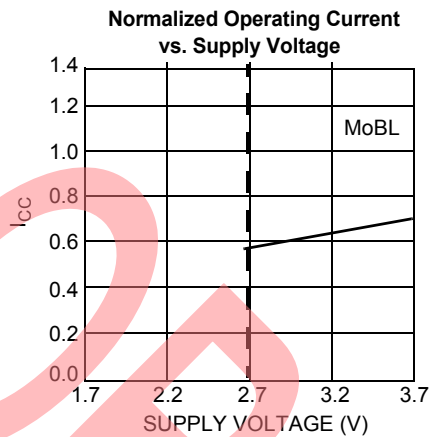
Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[10, 15]



Write Cycle No. 4 ($\overline{\text{BHE/BLE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[16]



Typical DC and AC Characteristics



Truth Table

\overline{CE}	\overline{WE}	\overline{OE}	\overline{BHE}	\overline{BLE}	I/O ₈ –I/O ₁₅	I/O ₀ –I/O ₇	Mode	Power
H	X	X	X	X	High-Z	High-Z	Deselect/Power-down	Standby (I_{SB})
X	X	X	H	H	High-Z	High-Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	L	L	Data Out	Data Out	Read	Active (I_{CC})
L	H	L	H	L	High-Z	Data Out	Read	Active (I_{CC})
L	H	L	L	H	Data Out	High-Z	Read	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In	Data In	Write	Active (I_{CC})
L	L	X	H	L	High-Z	Data In	Write	Active (I_{CC})
L	L	X	L	H	Data In	High-Z	Write	Active (I_{CC})

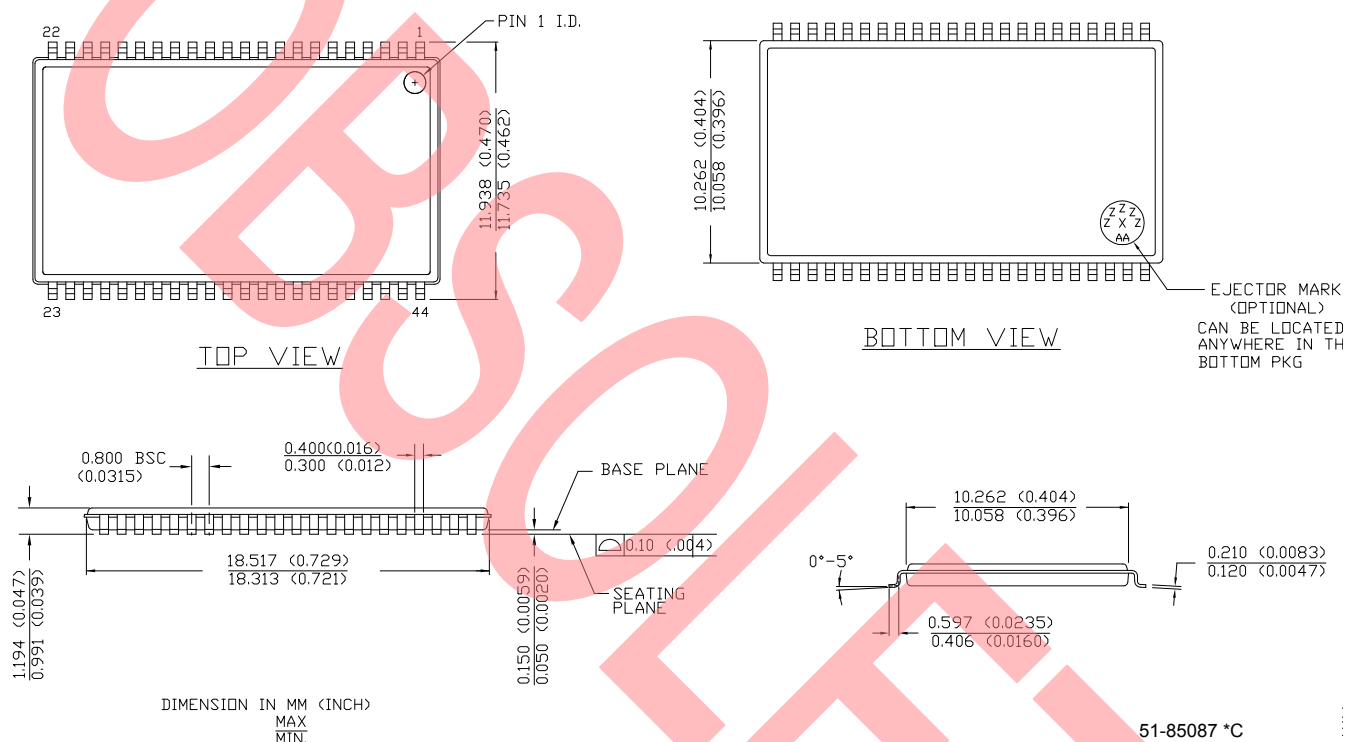
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY62137VNLL-70ZSXA	51-85087	44-pin TSOP II (Pb-free)	Automotive-A
	CY62137VNLL-70ZSXE		44-pin TSOP II (Pb-free)	Automotive-E

Please contact your local Cypress sales representative for availability of these parts

Package Diagram (continued)

Figure 1. 44-pin TSOP II (51-85087)



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Document History Page

Document Title: CY62137VN MoBL® 2-Mbit (128K x 16) Static RAM Document Number: 001-06497				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	426503	See ECN	NXR	New Data Sheet
*A	488954	See ECN	NXR	Added Automotive product Updated Ordering Information table
*B	2897932	03/23/2010	VKN	Removed Industrial grade Removed 55ns speed bin Updated Ordering Information table Updated TSOP-II package outline diagram
*C	3094203	11/24/2010	RAME	The specified parts in the ordering information table are being pruned. Obsolete datasheet.