High-Current, High- & Low-Side, Gate-Drive IC

FAN7392

ON Semiconductor®

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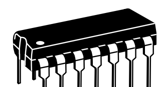
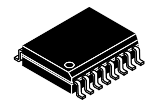
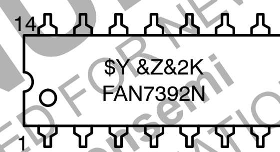


PDIP−14
14−PDIP
CASE 646−06

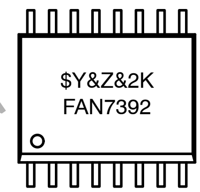


SOIC−16
16−SOP
CASE 751BH−01

MARKING DIAGRAM



FAN7392N



FAN7392MX

FAN7392N FAN7392	= Device Code
&Z	= Assembly Plant Code
&2	= 2−Digit Date Code
&K	= 2−Digits Lot Run Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

Description

The FAN7392 is a monolithic high− and low−side gate drive IC, that can drive high−speed MOSFETs and IGBTs that operate up to +600 V. It has a buffered output stage with all NMOS transistors designed for high pulse current driving capability and minimum cross−conduction. ON Semiconductor's high−voltage process and common−mode noise canceling techniques provide stable operation of the high−side driver under high dv/dt noise circumstances. An advanced level−shift circuit offers high−side gate driver operation up to V_S = −9.8 V (typical) for V_{BS} = 15 V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The UVLO circuit prevents malfunction when V_{CC} and V_{BS} are lower than the specified threshold voltage. The high−current and low−output voltage drop feature makes this device suitable for half− and full−bridge inverters, like switching−mode power supply and high−power DC−DC converter applications.

Features

- Floating Channel for Bootstrap Operation to +600 V
- 3 A/3 A Sourcing/Sinking Current Driving Capability
- Common−Mode dv/dt Noise Canceling Circuit
- 3.3 V Logic Compatible
- Separate Logic Supply (V_{DD}) Range from 3.3 V to 20 V
- Under−Voltage Lockout for V_{CC} and V_{BS}
- Cycle−by−Cycle Edge−Triggered Shutdown Logic
- Matched Propagation Delay for Both Channels
- Outputs In−phase with Input Signals
- Available in 14−DIP and 16−SOP (Wide) Packages
- This is a Pb−Free Device

Applications

- High−Speed Power MOSFET and IGBT Gate Driver
- Server Power Supply
- Uninterrupted Power Supply (UPS)
- Telecom System Power Supply
- Distributed Power Supply
- Motor Drive Inverter

May, 2024 − Rev. 3
Publication Order Number:
FAN7392/D

TYPICAL APPLICATION DIAGRAMS

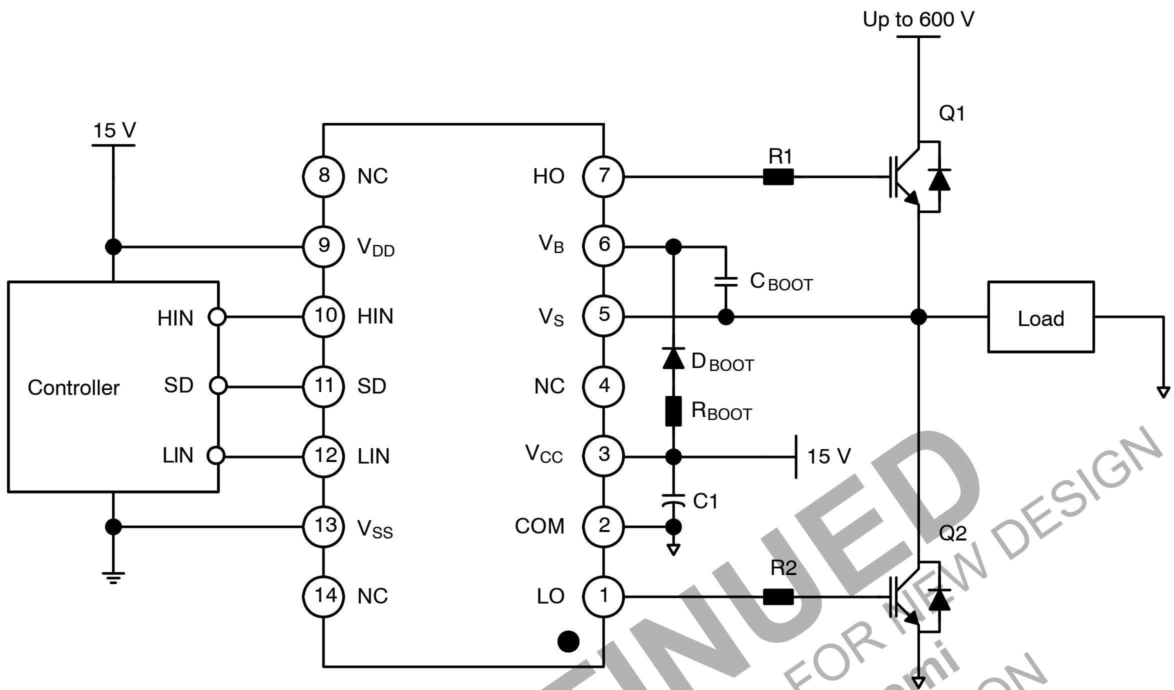


Figure 1. Typical Application Circuit (Referenced 14−DIP)

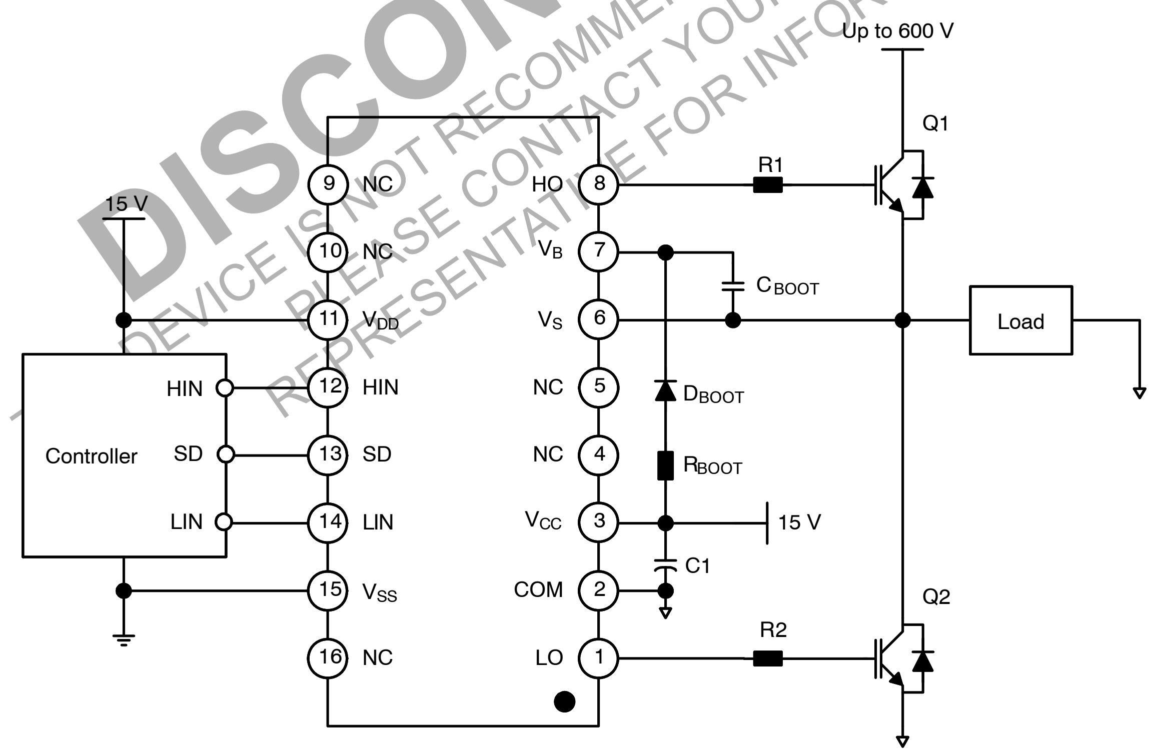


Figure 2. Application Circuit for Half−Bridge (Referenced 16−SOP)

INTERNAL BLOCK DIAGRAM

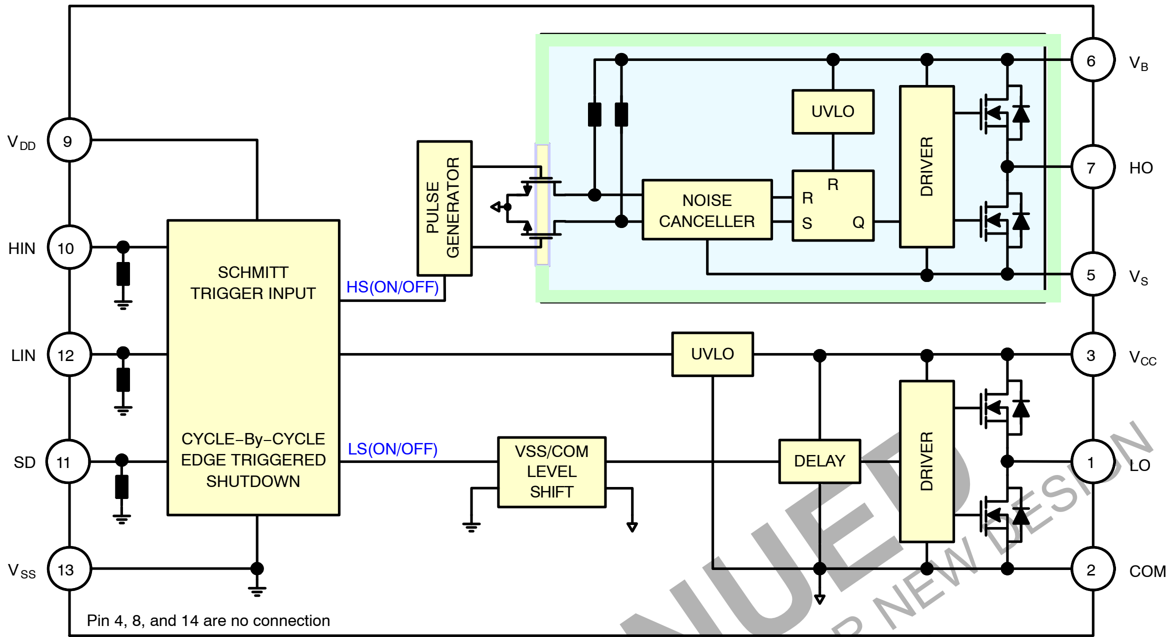


Figure 3. Functional Block Diagram (Referenced 14–Pin)

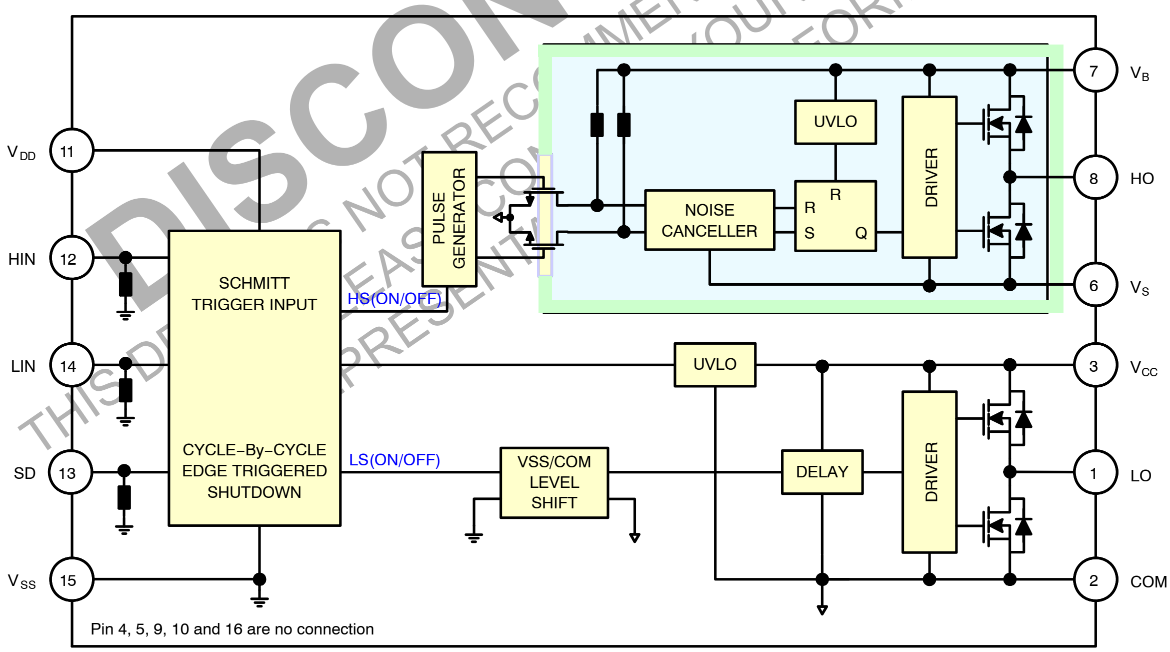
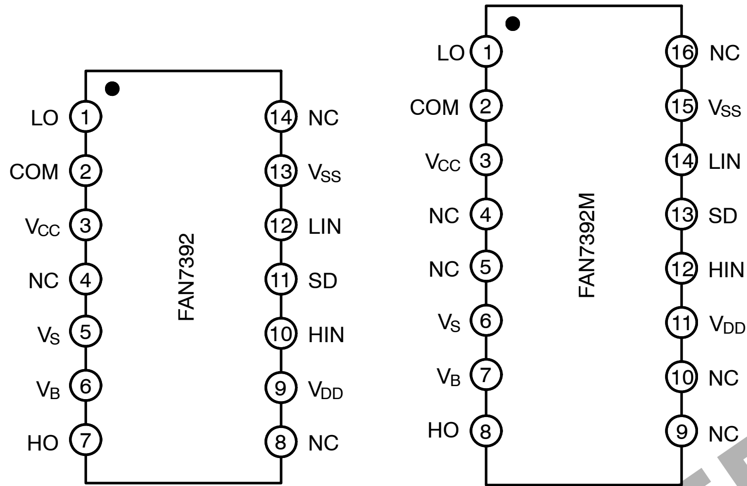


Figure 4. Functional Block Diagram (Referenced 16–SOP)

PIN CONFIGURATION



(a) 14−DIP (b) 16−SOP (Wide Body)

Figure 5. Pin Configurations (Top View)

PIN DEFINITIONS

14−Pin	16−Pin	Name	Description
1	1	LO	Low−Side Driver Output
2	2	COM	Low−Side Return
3	3	V_{CC}	Low−Side Supply Voltage
5	6	V_S	High−Voltage Floating Supply Return
6	7	V_B	High−Side Floating Supply
7	8	HO	High−Side Driver Output
9	11	V_{DD}	Logic Supply Voltage
10	12	HIN	Logic Input for High−Side Gate Driver Output
11	13	SD	Logic Input for Shutdown Function
12	14	LIN	Logic Input for Low−Side Gate Driver Output
13	15	V_{SS}	Logic Ground
4, 8, 14	4, 5, 9, 10, 16	NC	No Connect

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Symbol	Characteristics		Min	Max	Unit
V_B	High−Side Floating Supply Voltage		−0.3	625.0	V
V_S	High−Side Floating Offset Voltage		V_B − 25.0	V_B + 0.3	V
V_{HO}	High−Side Floating Output Voltage		V_S − 0.3	V_B + 0.3	V
V_{CC}	Low−Side Supply Voltage		−0.3	25.0	V
V_{LO}	Low−Side Floating Output Voltage		−0.3	V_{CC} + 0.3	V
V_{DD}	Logic Supply Voltage		−0.3	V_{SS} + 25.0	V
V_{SS}	Logic Supply Offset Voltage		V_{CC} − 25.0	V_{CC} + 0.3	V
V_{IN}	Logic Input Voltage (HIN, LIN and SD)		V_{SS} − 0.3	V_{DD} + 0.3	V
dV_S/dt	Allowable Offset Voltage Slew Rate		–	±50	V/ns
P_D	Power Dissipation (Note 1, 2, 3)	14−PDIP	–	1.6	W
		16−SOP	–	1.3	
θ_{JA}	Thermal Resistance	14−PDIP	–	75	°C/W
		16−SOP	–	95	
T_J	Maximum Junction Temperature		–	+150	°C
T_{STG}	Storage Temperature		−55	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR−4 glass epoxy material).
2. Refer to the following standards:
   JESD51−2: Integral circuits thermal test method environmental conditions − natural convection; and
   JESD51−3: Low effective thermal conductivity test board for leaded surface−mount packages.
3. Do not exceed power dissipation (P_D) under any circumstances.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_B	High−Side Floating Supply Voltage	V_S + 10	V_S + 20	V
V_S	High−Side Floating Supply Offset Voltage	6 − V_{CC}	600	V
V_{HO}	High−Side Output Voltage	V_S	V_B	V
V_{CC}	Low−Side Supply Voltage	10	20	V
V_{LO}	Low−Side Output Voltage	0	V_{CC}	V
V_{DD}	Logic Supply Voltage	V_{SS} + 3	V_{SS} + 20	V
V_{SS}	Logic Supply Offset Voltage	−5	5	V
V_{IN}	Logic Input Voltage	V_{SS}	V_{DD}	V
T_A	Operating Ambient Temperature	−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15.0 V, V_{SS} = COM = 0 V and T_A=25°C, unless otherwise specified. The V_{IH}, V_{IL}, and I_{IN} parameters are referenced to V_{SS} and are applicable to the respective input leads: HIN, LIN, and SD. The V_O and I_O parameters are referenced to V_S and COM and are applicable to the respective output leads: HO and LO.)

Symbol	Characteristics	Test Condition	Min	Typ	Max	Unit
LOW–SIDE POWER SUPPLY SECTION						
I_{QCC}	Quiescent V_{CC} Supply Current	V_{IN} = 0 V or V_{DD}	–	40	80	μA
I_{QDD}	Quiescent V_{DD} Supply Current	V_{IN} = 0 V or V_{DD}	–	–	10	μA
I_{PCC}	Operating V_{CC} Supply Current	f_{IN} = 20 kHz, rms, V_{IN} = 15 V_{PP}	–	430	–	μA
I_{PDD}	Operating V_{DD} Supply Current	f_{IN} = 20 kHz, rms, V_{IN} = 15 V_{PP}	–	300	–	μA
I_{SD}	Shutdown Supply Current	S_D=V_{DD}	–	120	–	μA
V_{CCUV+}	V_{CC} Supply Under–Voltage Positive–Going Threshold Voltage	V_{IN} = 0 V, V_{CC} = Sweep	7.7	8.8	9.9	V
V_{CCUV-}	V_{CC} Supply Under–Voltage Negative–Going Threshold Voltage	V_{IN} = 0 V, V_{CC} = Sweep	7.3	8.4	9.5	V
V_{CCUVH}	V_{CC} Supply Under–Voltage Lockout Hysteresis Voltage	V_{IN} = 0 V, V_{CC} = Sweep	–	0.4	–	V
BOOTSTRAPPED SUPPLY SECTION						
I_{QBS}	Quiescent V_{BS} Supply Current	V_{IN} = 0 V or V_{DD}	–	60	130	μA
I_{PBS}	Operating V_{BS} Supply Current	f_{IN} = 20 kHz, rms value	–	500	–	μA
V_{BSUV+}	V_{BS} Supply Under–Voltage Positive–Going Threshold Voltage	V_{IN} = 0 V, V_{BS} = Sweep	7.7	8.8	9.9	V
V_{BSUV-}	V_{BS} Supply Under–Voltage Negative–Going Threshold Voltage	V_{IN} = 0 V, V_{BS} = Sweep	7.3	8.4	9.5	V
V_{BSUVH}	V_{BS} Supply Under–Voltage Lockout Hysteresis Voltage	V_{IN} = 0 V, V_{BS} = Sweep	–	0.4	–	V
I_{LK}	Offset Supply Leakage Current	V_B = V_S = 600 V	–	–	50	μA
INPUT LOCIC SECTION (HIN, LIN, AND SD)						
V_{IH}	Logic "1" Input Threshold Voltage	V_{DD} = 3 V	2.4	–	–	V
		V_{DD} = 15 V	9.5	–	–	V
V_{IL}	Logic "0" Input Threshold Voltage	V_{DD} = 3 V	–	–	0.8	V
		V_{DD} = 15 V	–	–	4.5	V
I_{IN+}	Logic Input High Bias Current	V_{IN} = V_{DD}	–	20	40	μA
I_{IN-}	Logic Input Low Bias Current	V_{IN} = 0 V	–	–	3	μA
R_{IN}	Logic Input Pull–Down Resistance		375	750	–	kΩ
GATE DRIVER OUTPUT SECTION						
V_{OH}	High–Level Output Voltage (V_{BIAS} – V_O)	No Load (I_O = 0 A)	–	–	1.5	V
V_{OL}	Low–Level Output Voltage	No Load (I_O = 0 A)	–	–	200	mV
I_{O+}	Output High, Short–Circuit Pulsed Current (Note 4)	V_O = 0 V, PW ≤ 10 μs	2.5	3.0	–	A
I_{O-}	Output Low, Short–Circuit Pulsed Current (Note 4)	V_O = 15 V, PW ≤ 10 μs	2.5	3.0	–	A
V_{SS}/COM	V_{SS}–COM/COM–V_{SS} Voltage Endurability		–5.0	–	5.0	V
$-V_S$	Allowable Negative V_S Pin Voltage for HIN Signal Propagation to HO		–	–9.8	–7.0	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. This parameter guaranteed by design.

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15.0 V, V_{SS} = COM = 0V, C_{LOAD} = 1000 pF, T_A = 25°C, unless otherwise specified.)

Symbol	Characteristics	Test Condition	Min	Typ	Max	Unit
t_{on}	Turn−On Propagation Delay Time	V_S = 0 V	–	130	180	ns
t_{off}	Turn−Off Propagation Delay Time	V_S = 0 V	–	150	200	ns
t_{sd}	Shutdown Propagation Delay Time (Note 5)		–	130	180	
t_r	Turn−On Rise Time		–	25	50	
t_f	Turn−Off Fall Time		–	20	45	
MT	Delay Matching, HO & LO Turn−On/Off		–	–	35	

5. This parameter guaranteed by design.

TYPICAL CHARACTERISTICS

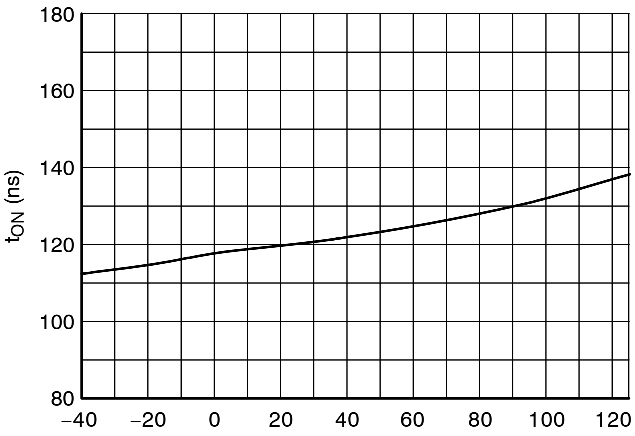


Figure 6. Turn−On Propagation Delay vs. Temperature

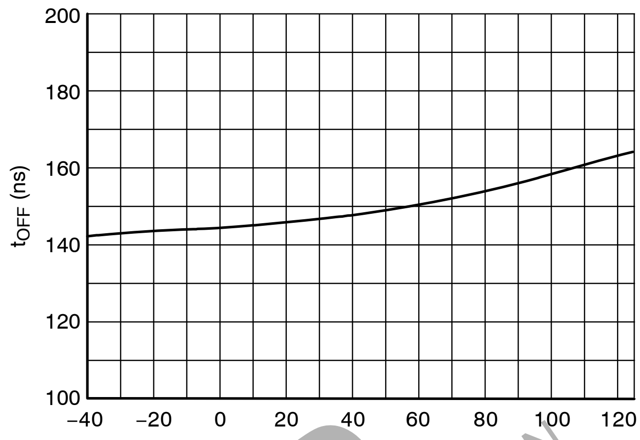


Figure 7. Turn−Off Propagation Delay vs. Temperature

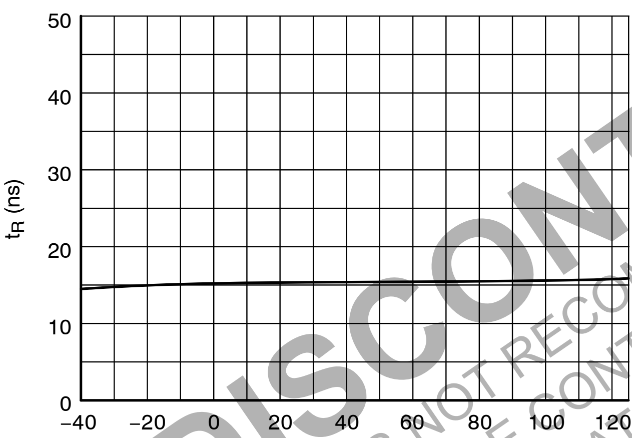


Figure 8. Turn−On Rise Time vs. Temperature

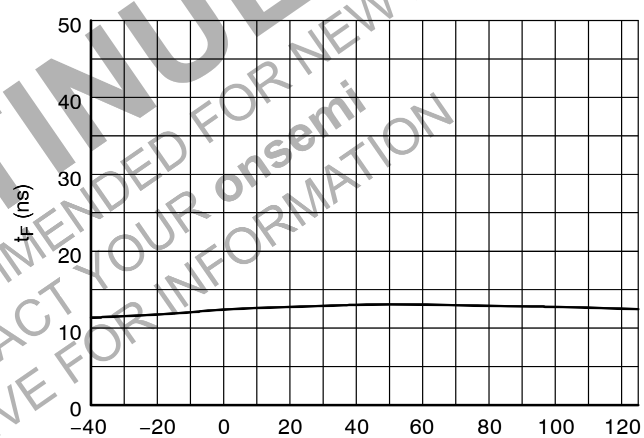


Figure 9. Turn−Off Fall Time vs. Temperature

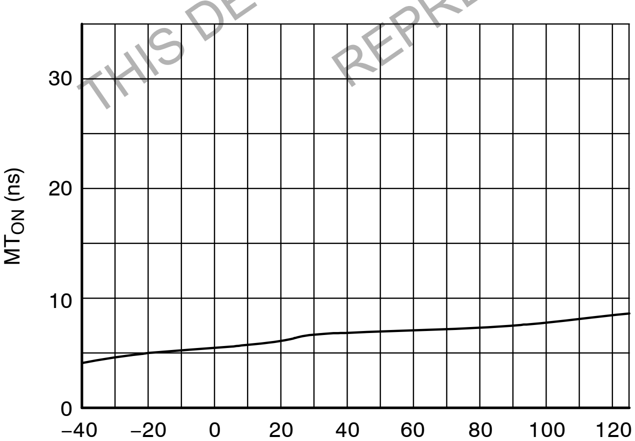


Figure 10. Turn−On Delay Matching vs. Temperature

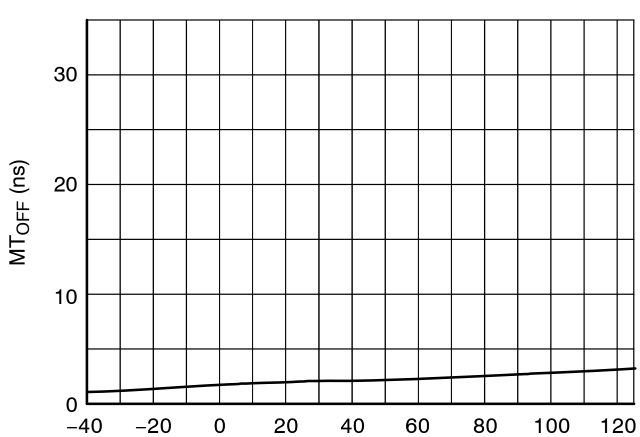


Figure 11. Turn−Off Delay Matching vs. Temperature

TYPICAL CHARACTERISTICS (continued)

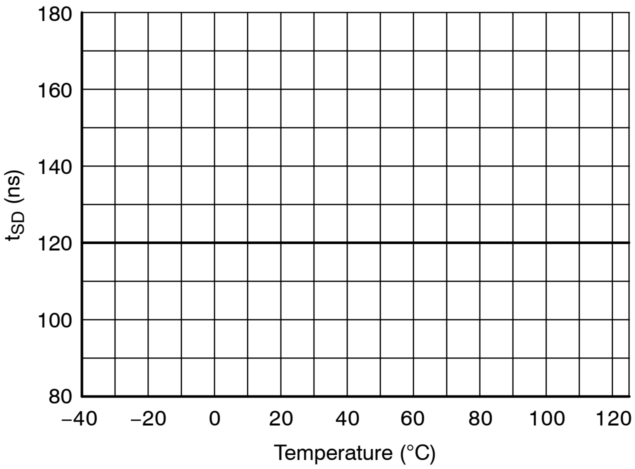


Figure 12. Shutdown Propagation Delay vs. Temperature

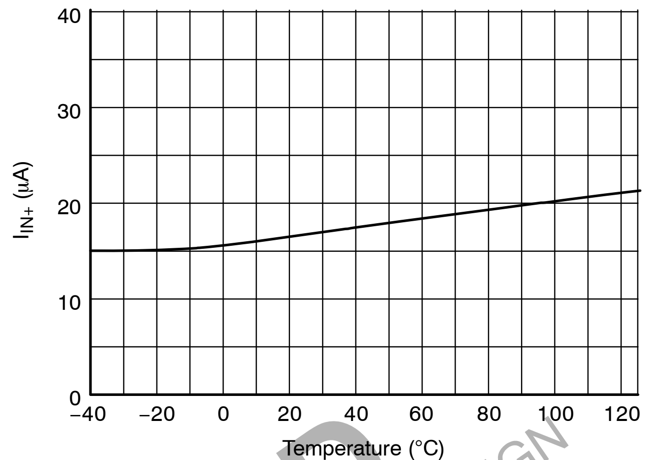


Figure 13. Logic Input High Bias Current vs. Temperature

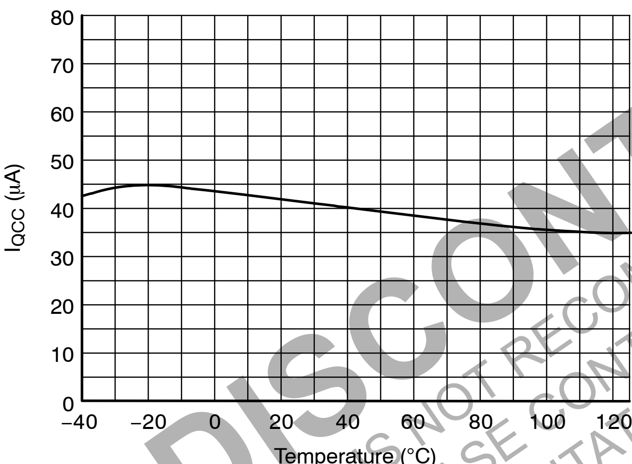


Figure 14. Quiescent V_{CC} Supply Current vs. Temperature

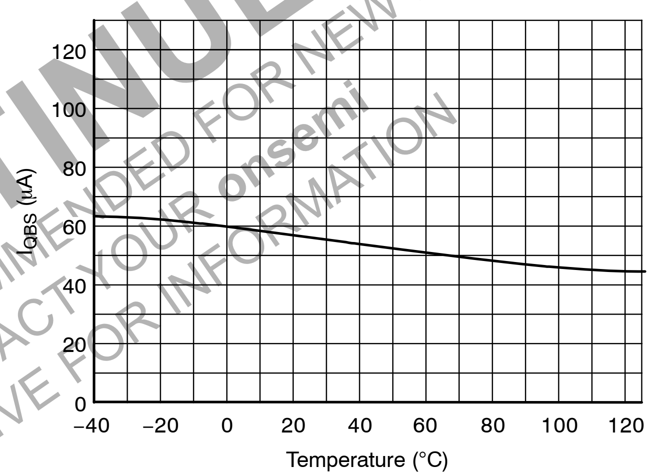


Figure 15. Quiescent V_{BS} Supply Current vs. Temperature

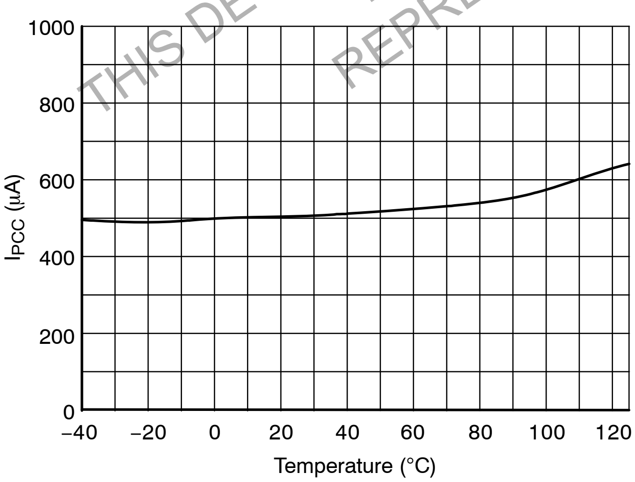


Figure 16. Operating V_{CC} Supply Current vs. Temperature

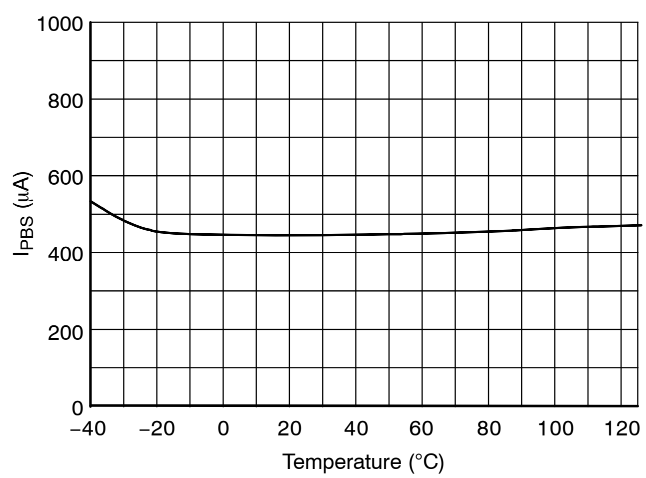


Figure 17. Operating V_{BS} Supply Current vs. Temperature

TYPICAL CHARACTERISTICS (continued)

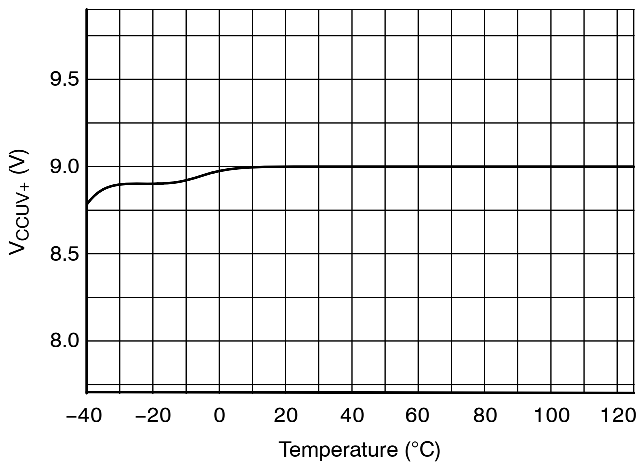


Figure 18. V_{CC} UVLO+ vs. Temperature

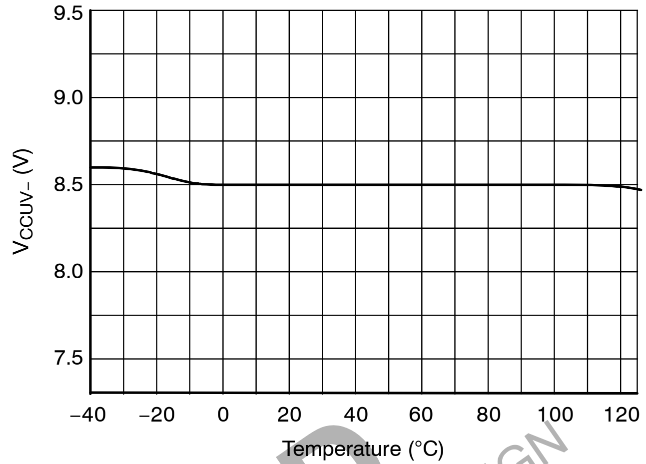


Figure 19. V_{CC} UVLO− vs. Temperature

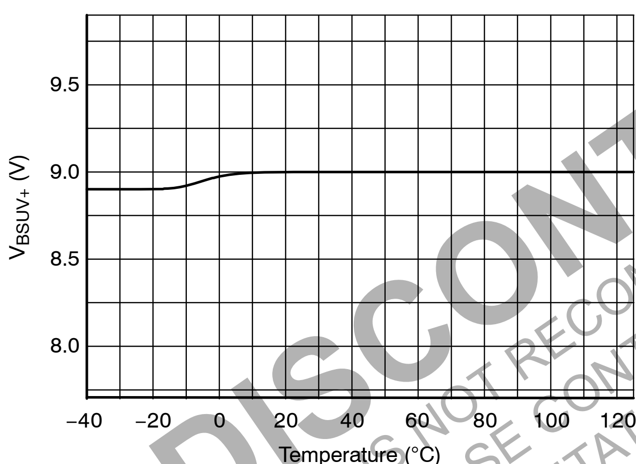


Figure 20. V_{BS} UVLO+ vs. Temperature

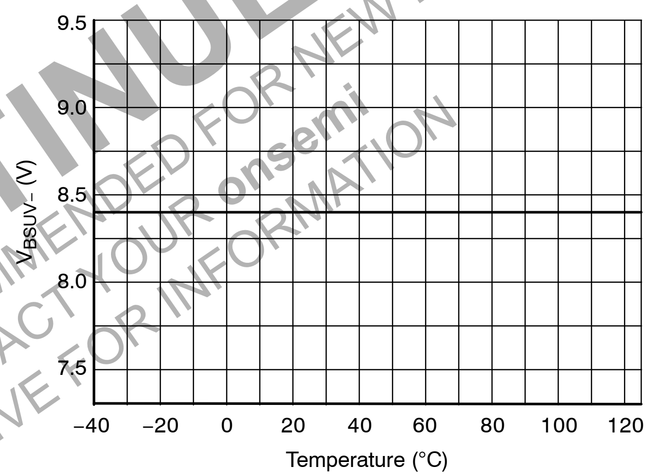


Figure 21. V_{BS} UVLO− vs. Temperature

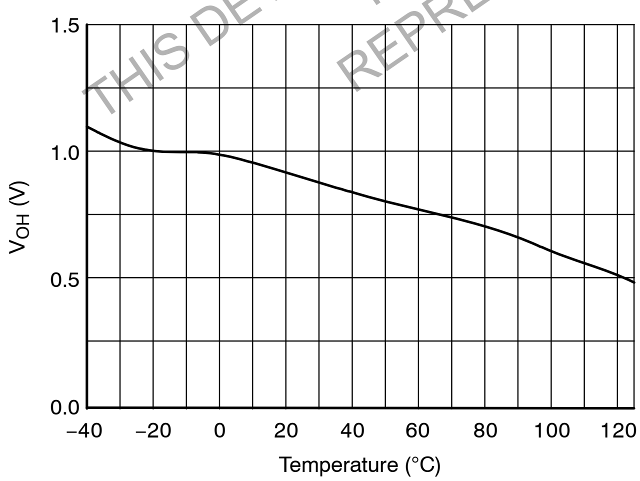


Figure 22. High−Level Output Voltage vs. Temperature

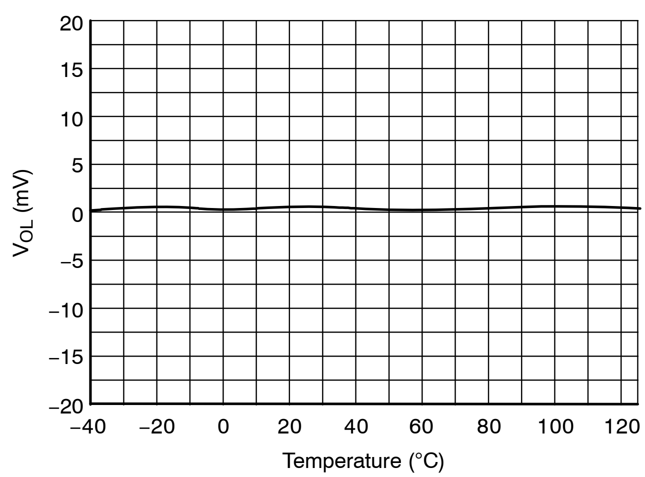


Figure 23. Low−Level Output Voltage vs. Temperature

TYPICAL CHARACTERISTICS (continued)

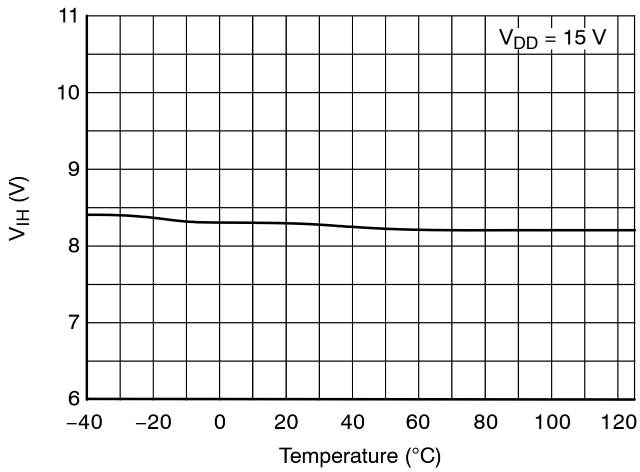


Figure 24. Logic High Input Voltage vs. Temperature

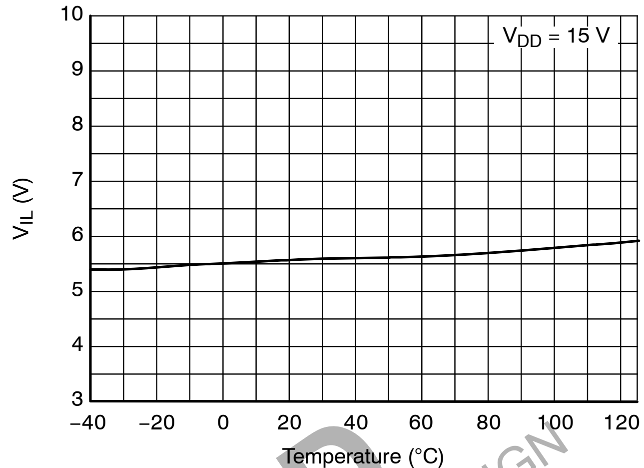


Figure 25. Logic Low Input Voltage vs. Temperature

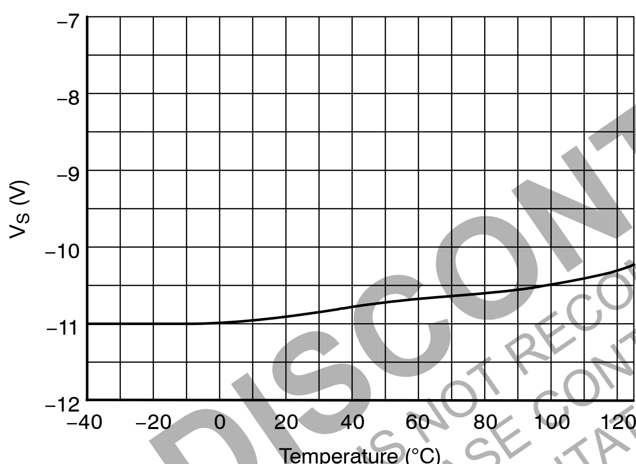


Figure 26. Allowable Negative V_S Voltage vs. Temperature

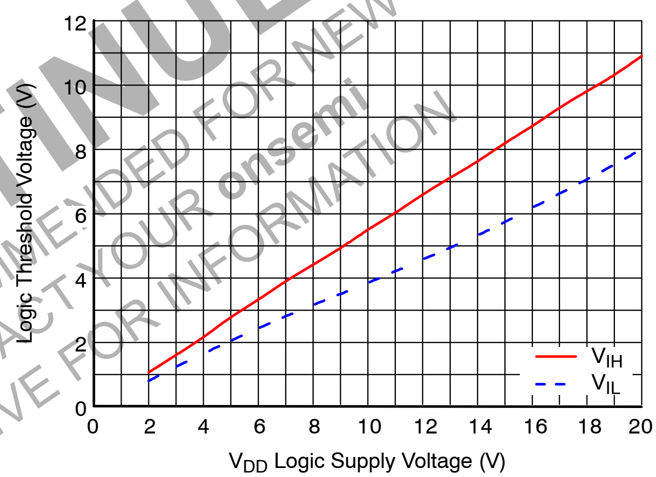


Figure 27. Input Logic (HIN & LIN) Threshold Voltage vs. V_{DD} Supply Voltage

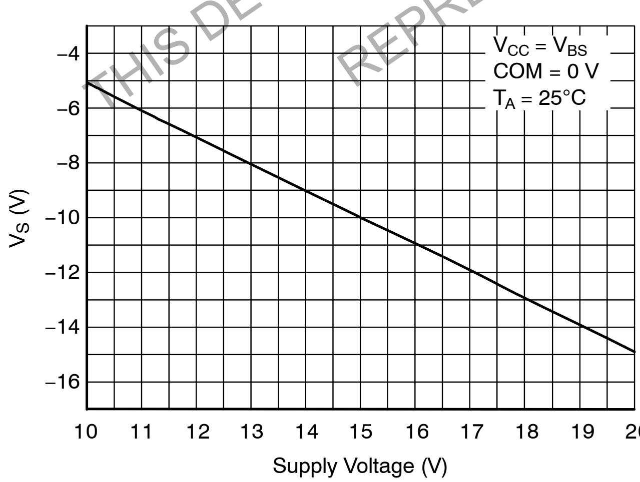


Figure 28. Allowable Negative Vs Voltage for HIN Signal Propagation to High Side vs. Supply Voltage

SWITCHING TIME DEFINITIONS

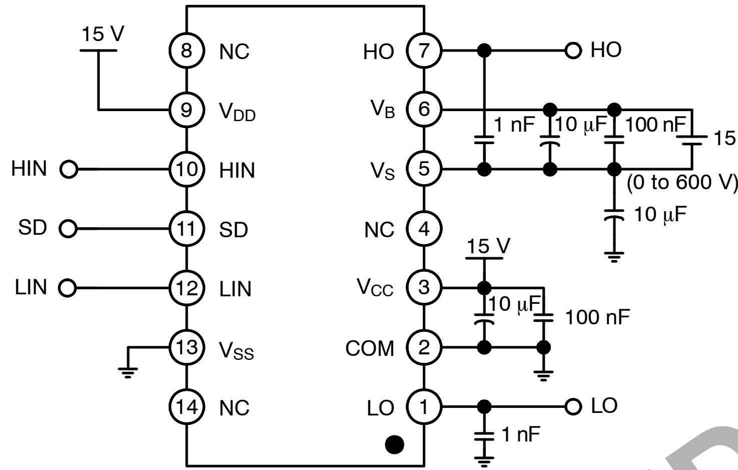


Figure 29. Switching Time Test Circuit (Referenced 14−DIP)

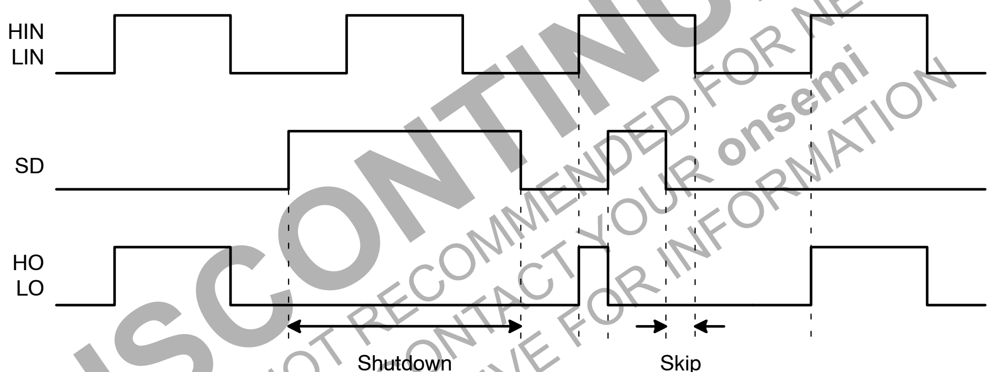


Figure 30. Input/Output Timing Diagram

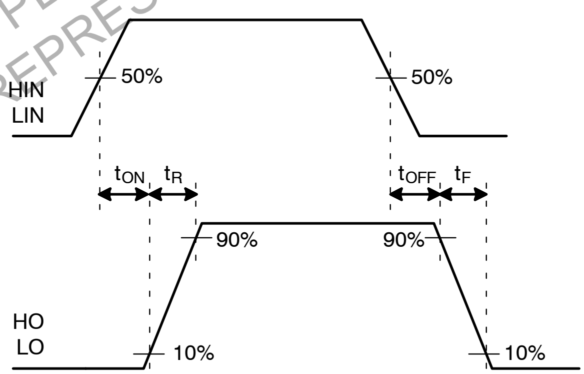


Figure 31. Switching Time Waveform Definitions

SWITCHING TIME DEFINITIONS (continued)

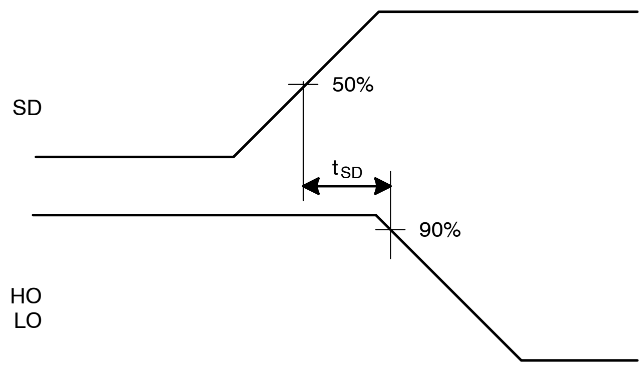


Figure 32. Shutdown Waveform Definition

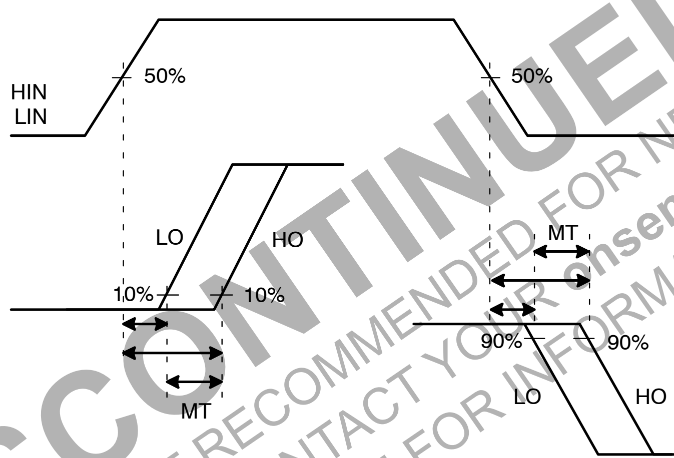


Figure 33. Delay Matching Waveform Definitions

APPLICATION INFORMATION

Negative V_S Transient

The bootstrap circuit has the advantage of being simple and low cost, but has some limitations. The biggest difficulty with this circuit is the negative voltage present at the emitter of the high−side switching device when high−side switch is turned−off in half−bridge application.

If the high−side switch, Q1, turns−off while the load current is flowing to an inductive load, a current commutation occurs from high−side switch, Q1, to the diode, D2, in parallel with the low−side switch of the same inverter leg. Then the negative voltage present at the emitter of the high−side switching device, just before the freewheeling diode, D2, starts clamping, causes load current to suddenly flow to the low−side freewheeling diode, D2, as shown in Figure 34.

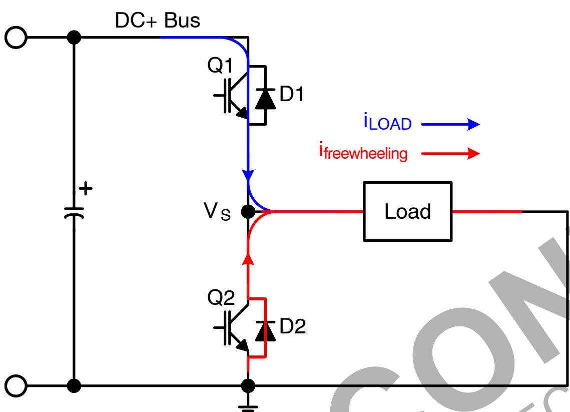


Figure 34. Half−Bridge Application Circuits

This negative voltage can be trouble for the gate driver's output stage, there is the possibility to develop an over−voltage condition of the bootstrap capacitor, input signal missing and latch−up problems because it directly affects the source V_S pin of the gate driver, as shown in Figure 35. This undershoot voltage is called "negative V_S transient".

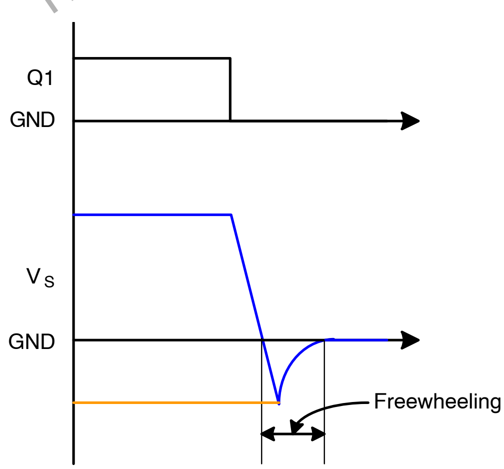


Figure 35. V_S Waveforms During Q1 Turn−Off

Figure 36 and Figure 37 show the commutation of the load current between high−side switch, Q1, and low−side freewheelling diode, D3, in same inverter leg. The parasitic inductances in the inverter circuit from the die wire bonding to the PCB tracks are jumped together in L_C and L_E for each IGBT. When the high−side switch, Q1, and low−side switch, Q4, are turned on, the V_{S1} node is below DC+ voltage by the voltage drops associated with the power switch and the parasitic inductances of the circuit due to load current is flows from Q1 and Q4, as shown in Figure 36. When the high−side switch, Q1, is turned off and Q4, remained turned on, the load current to flows the low−side freewheeling diode, D3, due to the inductive load connected to VS1 as shown in Figure 37. The current flows from ground (which is connected to the COM pin of the gate driver) to the load and the negative voltage present at the emitter of the high−side switching device.

In this case, the COM pin of the gate driver is at a higher potential than the V_S pin due to the voltage drops associated with freewheeling diode, D3, and parasitic elements, L_{C3} and L_{E3}.

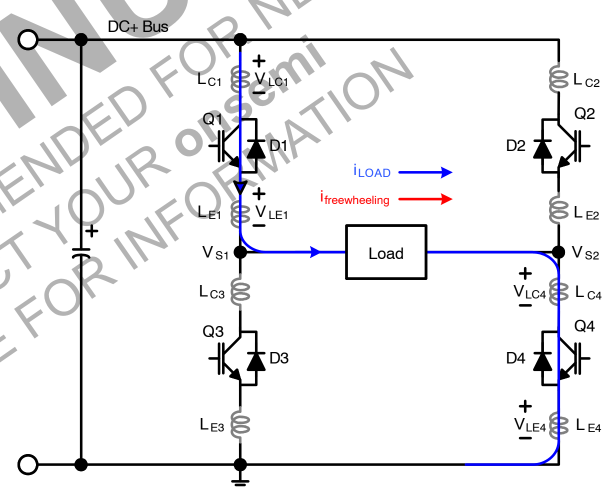


Figure 36. Q1 and Q4 Turn−On

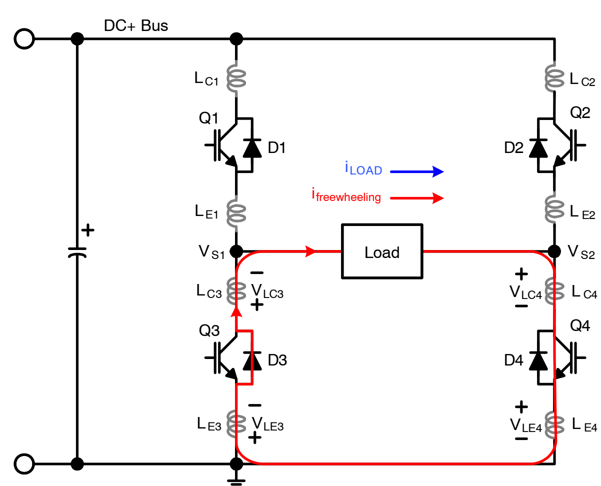


Figure 37. Q1 Turn−Off and D3 Conducting

The FAN7392 has a negative V_S transient performance curve, as shown in Figure 38.

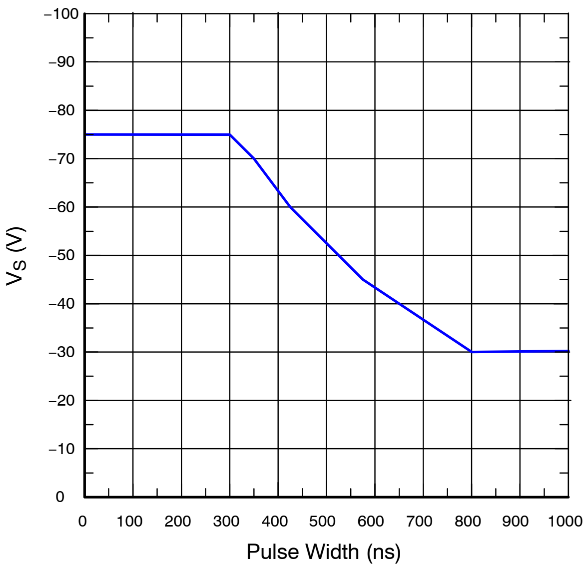


Figure 38. Negative V_S Transient Characteristic

Even though the FAN7392 has been shown able to handle these negative V_S tranient conditions, it is strongly recommended that the circuit designer limit the negative V_S transient as much as possible by careful PCB layout to minimized the value of parasitic elements and component use. The amplitude of negative V_S voltage is proportional to the parasitic inductances and the turn−off speed, di/dt, of the switching device.

GENERAL GUIDELINES

Printed Circuit Board Layout

The relayout recommended for minimized parasitic elements is as follows:

- Direct tracks between switches with no loops or deviation.
- Avoid interconnect links. These can add significant inductance.
- Reduce the effect of lead−inductance by lowering package height above the PCB.
- Consider co−locating both power switches to reduce track length.
- To minimize noise coupling, the ground plane should not be placed under or near the high−voltage floating side.
- To reduce the EM coupling and improve the power switch turn−on/off performance, the gate drive loops must be reduced as much as possible.

Placement of Components

The recommended placement and selection of component as follows:

- Place a bypass capacitor between the V_{DD} and V_{SS} pins. A ceramic 1 μF capacitor is suitable for most applications. This component should be placed as close as possible to the pins to reduce parasitic elements.
- The bypass capacitor from V_{CC} to COM supports both the low−side driver and bootstrap capacitor recharge. A value at least ten times higher than the bootstrap capacitor is recommended.
- The bootstrap resistor, R_{BOOT}, must be considered in sizing the bootstrap resistance and the current developed during initial bootstrap charge. If the resistor is needed in series with the bootstrap diode, verify that V_B does not fall below COM (ground). Recommended use is typically 5~10 Ω that increase the V_{BS} time constant. If the voltage drop of of bootstrap resistor and diode is too high or the circuit topology does not allow a sufficient charging time, a fast recovery or ultra−fast recovery diode can be used.
- The bootstrap capacitor, C_{BOOT}, uses a low−ESR capacitor, such as ceramic capacitor.

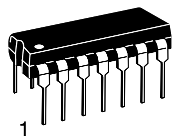
It is strongly recommended that the placement of components is as follows:

- Place components tied to the floating voltage pins (V_B and V_S) near the respective high−voltage portions of the device and the FAN7392. NC (not connected) pins in this package maximize the distance between the high−voltage and low−voltage pins (*see Figure 5*).
- Place and route for bypass capacitors and gate resistors as close as possible to gate drive IC.
- Locate the bootstrap diode, D_{BOOT}, as close as possible to bootstrap capacitor, C_{BOOT}.
- The bootstrap diode must use a lower forward voltage drop and minimal switching time as soon as possible for fast recovery or ultra−fast diode.

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
FAN7392N	−40°C~125°C	PDIP−14 14−PDIP (Pb−Free)	1500 Units / Tube
FAN7392MX		SOIC−16 16−SOP (Pb−Free)	1000 / Tape & Reel

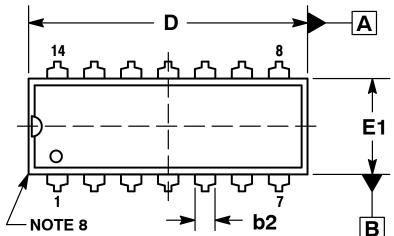
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



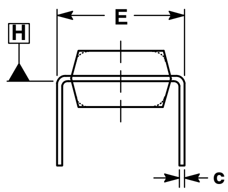
SCALE 1:1

PDIP−14
CASE 646−06
ISSUE S

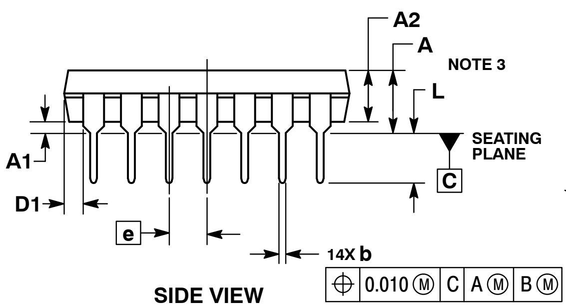
DATE 22 APR 2015



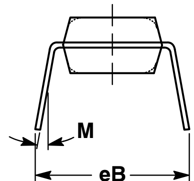
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW

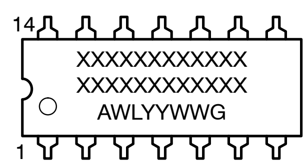


END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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PDIP−14
CASE 646−06
ISSUE S

DATE 22 APR 2015

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. NO CONNECTION
5. GATE
6. SOURCE
7. DRAIN
8. DRAIN
9. SOURCE
10. GATE
11. NO CONNECTION
12. GATE
13. SOURCE
14. DRAIN

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. NO CONNECTION
5. SOURCE
6. DRAIN
7. GATE
8. GATE
9. DRAIN
10. SOURCE
11. NO CONNECTION
12. SOURCE
13. DRAIN
14. GATE

STYLE 6:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 7:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 8:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 9:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

STYLE 10:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 12:
PIN 1. COMMON CATHODE
2. COMMON ANODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. COMMON ANODE
7. COMMON CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. ANODE/CATHODE
14. ANODE/CATHODE

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SOIC−16, 300 mils
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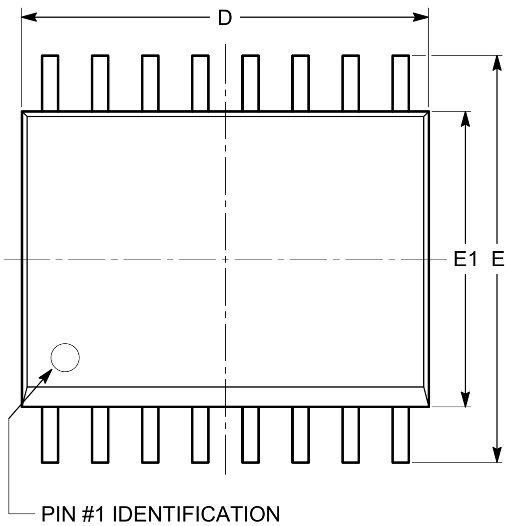
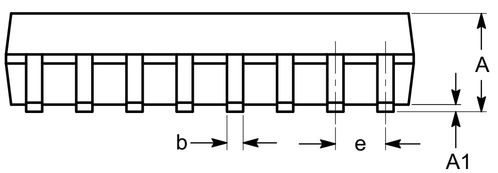
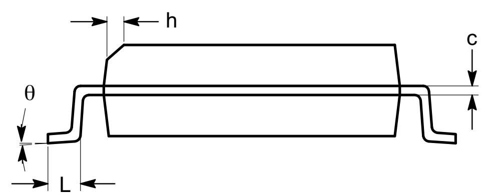


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.36	2.49	2.64
A1	0.10		0.30
b	0.33	0.41	0.51
c	0.18	0.23	0.28
D	10.08	10.31	10.49
E	10.01	10.31	10.64
E1	7.39	7.49	7.59
e		1.27 BSC	
h	0.25		0.75
L	0.38	0.81	1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-013.

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