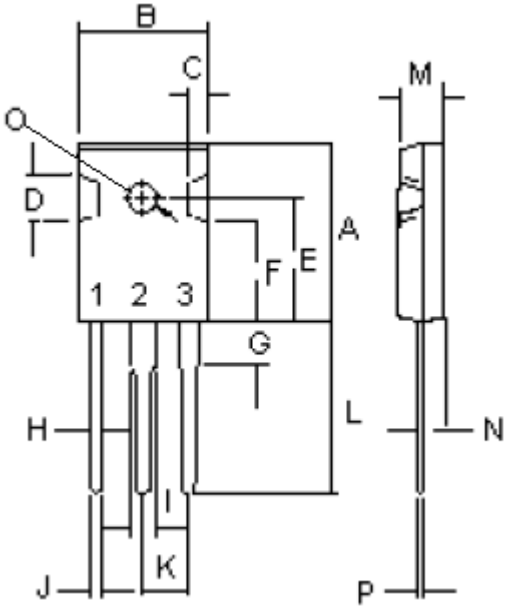
TIP147

Darlington Transistors

Features:

- Designed for general-purpose amplifier and low speed switching applications
- Collector - emitter sustaining voltage : $V_{CEO(sus)}$ = 100 V (Minimum)
- Collector-Emitter saturation voltage : $V_{CE\ (sat)}$ = 2 V (Maximum) at I_C = 5 A
- Monolithic construction with built-in base-emitter shunt resistor

TO-247 (3P)



Dimensions	Minimum	Maximum
A	20.63	22.38
B	15.38	16.2
C	1.9	2.7
D	5.1	6.1
E	14.81	15.22
F	11.72	12.84
G	4.2	4.5
H	1.82	2.46
I	2.92	3.23
J	0.89	1.53
K	5.26	5.66
L	18.5	21.5
M	4.68	5.36
N	2.4	2.8
O	3.25	3.65
P	0.55	0.7

Dimensions : Millimetres

PNP
TIP147

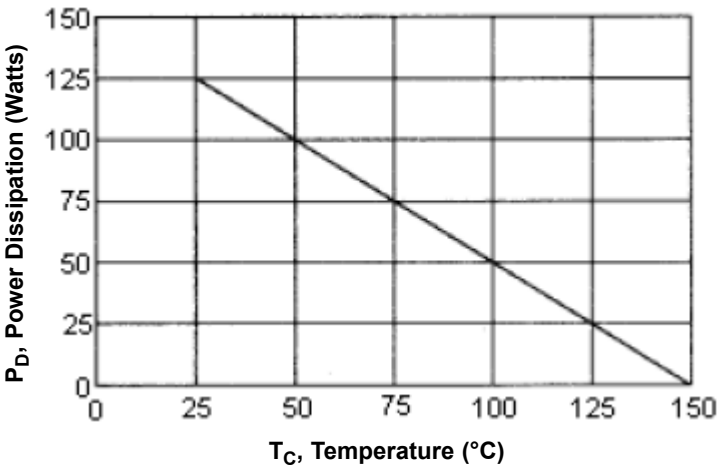
10 Amperes
Darlington
Complementary Silicon
Power Transistors
60 - 100 Volts
125 Watts

Maximum Ratings

Characteristic	Symbol	TIP147	Unit
Collector - emitter voltage	V_{CEO}	100	V
Collector - base voltage	V_{CBO}	100	
Emitter - base voltage	V_{EBO}	5	
Collector current - continuous - peak	I_C I_{CM}	10 15	A
Base current	I_B	0.5	
Total power dissipation at Tc = 25°C derate above 25°C	P_D	125 1	W W/°C
Operating and storage junction temperature range	T_J, T_{STG}	-65 to +150	°C

Thermal Characteristics

Characteristic	Symbol	Maximum	Unit
Thermal resistance junction to case	Rθjc	1	°C/W

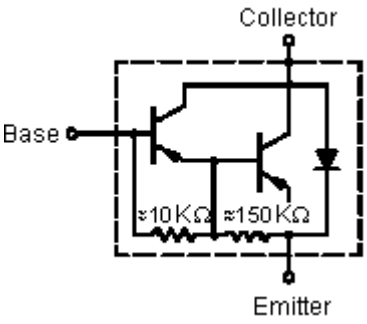


Electrical Characteristics (T_C = 25°C Unless Otherwise Specified)

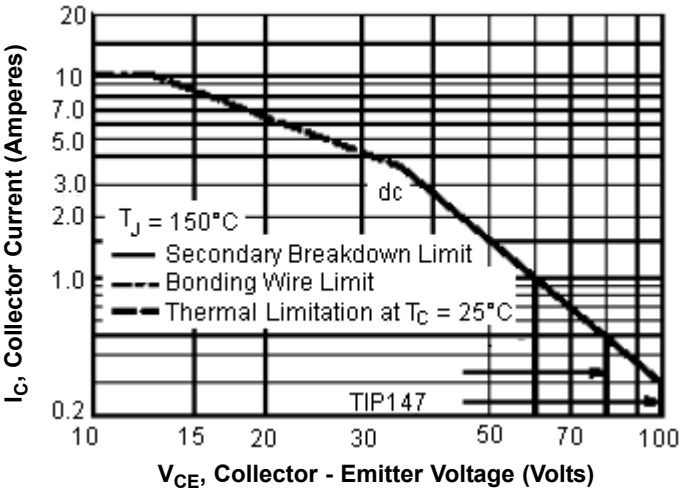
Characteristic		Symbol	Minimum	Maximum	Unit
OFF Characteristics					
Collector - emitter sustaining voltage (1) (I_C = 30 mA, I_B = 0)		$V_{CEO\ (SUS)}$	100	-	V
Collector cut off current (V_{CE} = 50 V, IB = 0)		I_{CEO}	-	2	mA
Collector cut off current (V_{CB} = 100 V, I_E = 0)		I_{CBO}	-	1	
Emitter cut off current (V_{EB} = 5 V, I_C = 0)		I_{EBO}	-	2	
ON Characteristics (1)					
DC current gain (I_C = 5 A, V_{CE} = 4 V) (I_C = 10 A, V_{CE} = 4 V)		h_{FE}	1,000 500	-	-
Collector - emitter saturation voltage (I_C = 5 A, I_B = 10 mA) (I_C = 10 A, I_B = 40 mA)		$V_{CE\ (sat)}$	-	2 3	V
Base - emitter saturation voltage (I_C = 10 A, I_B = 40 mA)		$V_{BE\ (sat)}$	-	3.5	
Base - emitter on voltage (I_C = 10 A, V_{CE} = 4 V)		$V_{BE\ (on)}$	-	3	
Switching Characteristics					
Delay Time	V_{CC} = 30 V, I_C = 5 A I_{B1} = -I_{B2} = 20 mA t_p = 20 µs, Duty cycle ≤ 2%	td	0.15 (Typical)	-	µs
Rise Time		tr	0.55 (Typical)	-	
Storage Time		ts	2.5 (Typical)	-	
Fall Time		tf		-	

(1) Pulse Test : Pulse width = 300 µs, duty cycle ≤ 2%

Internal Schematic Diagram



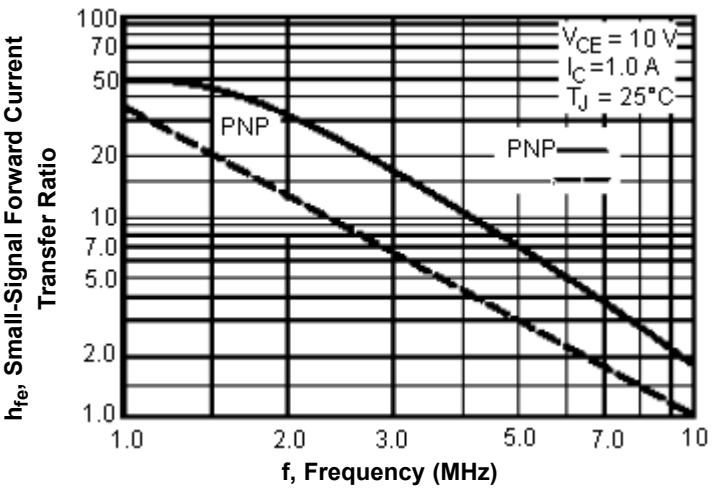
Active Region Safe Operating Area (SOA)



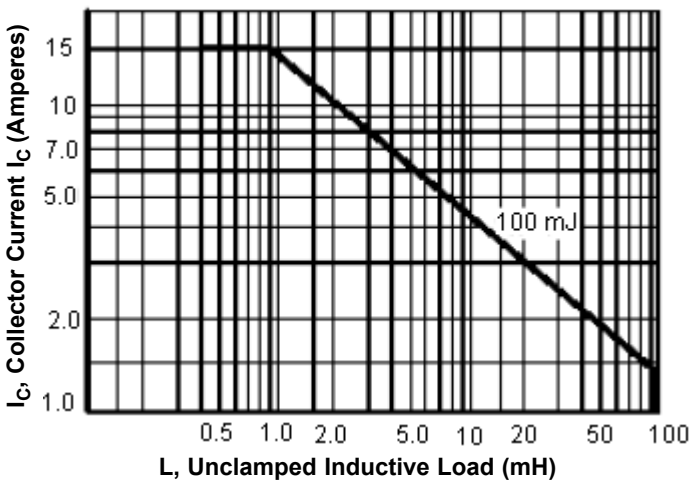
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate

The data of SOA curve is base on $T_{J\ (PK)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitation will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Small-Signal Common-Emitter Forward Current Transfer Ratio



Unclamped Inductive Load



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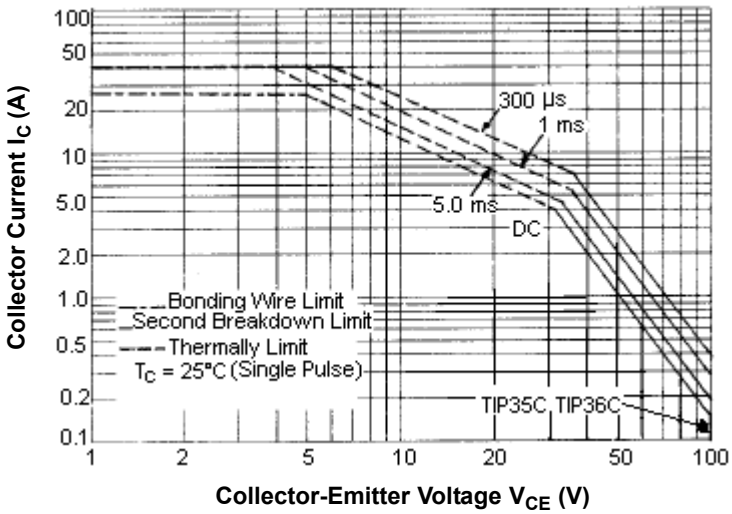
Safe Operating Area



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
The data of Figure - 6 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level . Second breakdown pulse limits are valid for duty cycle to 10% but must be derated when $T_C \geq 25°C$, second breakdown limitations do not derate the same as thermal limitation.

Specification Table

Description	$I_{C(av)}$ Maximum (A)	V_{CEO} Maximum (V)	h_{FE} Minimum at I_C = 15 A	P_{tot} at 25°C (W)	Package	Type	Part Number
Complementary Power Transistor	25	100	15	125	TO-247	NPN	TIP35C
Complementary Power Transistor	25	100	15	125	TO-247	PNP	TIP36C