



# CSD16323Q3 N-Channel NexFET™ Power MOSFET

## 1 Features

- Optimized for 5-V Gate Drive
- Ultra-Low  $Q_g$  and  $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3-mm × 3.3-mm Plastic Package

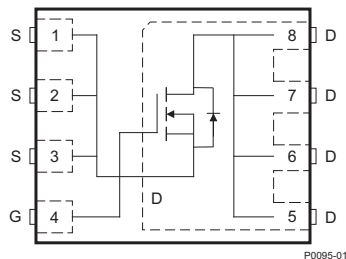
## 2 Applications

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Control or Synchronous FET Applications

## 3 Description

This 25-V, 3.8-m $\Omega$ , 3.3 × 3.3-mm SON NexFET™ power MOSFET has been designed to minimize losses in power conversion and optimized for 5-V gate drive applications.

Top View



P0095-01

### Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	25		V
$Q_g$	Gate Charge Total (4.5 V)	6.2		nC
$Q_{gd}$	Gate Charge Gate-to-Drain	1.1		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 3\text{ V}$	5.4	m $\Omega$
		$V_{GS} = 4.5\text{ V}$	4.4	
		$V_{GS} = 8\text{ V}$	3.8	
$V_{th}$	Threshold Voltage	1.1		V

### Device Information<sup>(1)</sup>

DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD16323Q3	13-Inch Reel	2500	SON	Tape and Reel
CSD16323Q3T	7-Inch Reel	250	3.30-mm × 3.30-mm Plastic Package	

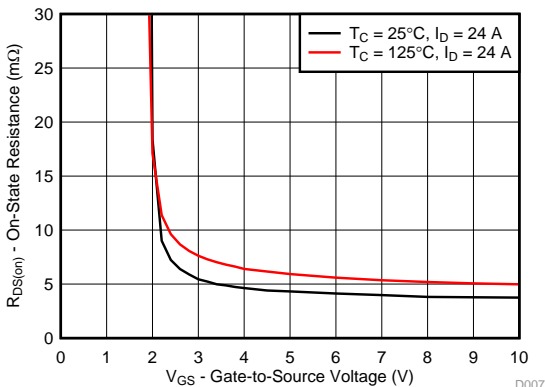
(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ (unless otherwise stated)		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	25	V
$V_{GS}$	Gate-to-Source Voltage	+10 / -8	V
$I_D$	Continuous Drain Current (Package Limit)	60	A
	Continuous Drain Current (Silicon Limited), $T_C = 25^\circ\text{C}$	105	
	Continuous Drain Current <sup>(1)</sup>	20	
$I_{DM}$	Pulsed Drain Current <sup>(2)</sup>	240	A
$P_D$	Power Dissipation <sup>(1)</sup>	2.8	W
	Power Dissipation, $T_C = 25^\circ\text{C}$	74	
$T_J$ , $T_{stg}$	Operating Junction, Storage Temperature	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, Single Pulse $I_D = 50\text{ A}$ , $L = 0.1\text{ mH}$ , $R_G = 25\text{ }\Omega$	125	mJ

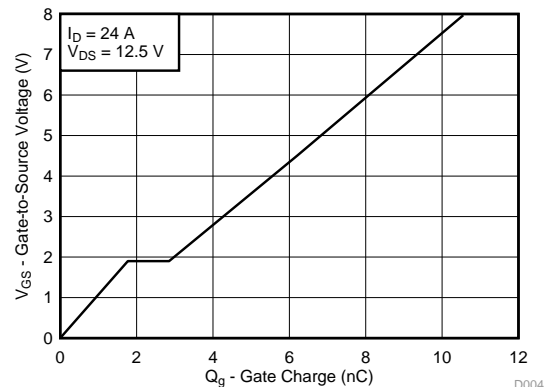
(1)  $R_{\theta JA} = 45^\circ\text{C/W}$  on 1-in<sup>2</sup>, 2-oz Cu pad on 0.06-in thick FR4 PCB.

(2) Max  $R_{\theta JC} = 1.7^\circ\text{C/W}$ , pulse duration  $\leq 100\text{ }\mu\text{s}$ , duty cycle  $\leq 1\%$ .

 $R_{DS(on)}$  vs  $V_{GS}$ 

D007

Gate Charge



D004



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2011) to Revision C	Page
• Changed <i>Description</i> text .....	<b>1</b>
• Added silicon limited continuous drain current to <i>Absolute Maximum Ratings</i> table .....	<b>1</b>
• Changed Note 2 in <i>Absolute Maximum Ratings</i> table.....	<b>1</b>
• Changed values in the <i>Thermal Information</i> table to align with standards .....	<b>3</b>
• Changed <a href="#">Figure 1</a> to reflect a transient $R_{\theta JC}$ curve .....	<b>4</b>
• Changed <a href="#">Figure 10</a> to reflect measured data.....	<b>5</b>
• Added <i>Device and Documentation Support</i> section.....	<b>7</b>
• Changed <i>MECHANICAL DATA</i> section to <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>8</b>

Changes from Revision A (April 2010) to Revision B	Page
• Replaced the THERMAL CHARACTERISTICS table with the new Thermal Information Table.....	<b>4</b>
• Replaced <a href="#">Figure 10</a> - Maximum Safe Operating Area .....	<b>5</b>

Changes from Original (August 2009) to Revision A	Page
• Changed $R_{DS(on)}$ - $V_{GS} = 3\text{ V}$ , $I_D = 24\text{ A}$ MAX value From: 6.5 To: 7.2 .....	<b>3</b>

## 5 Specifications

### 5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV <sub>DSS</sub>	Drain-to-source voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	25			V
I <sub>DSS</sub>	Drain-to-source leakage current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 20 V			1	μA
I <sub>GSS</sub>	Gate-to-source leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = +10/-8 V			100	nA
V <sub>GS(th)</sub>	Gate-to-source threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	0.9	1.1	1.4	V
R <sub>DS(on)</sub>	Drain-to-source on-resistance	V <sub>GS</sub> = 3 V, I <sub>D</sub> = 24 A		5.4	7.2	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 24 A		4.4	5.5	
		V <sub>GS</sub> = 8 V, I <sub>D</sub> = 24 A		3.8	4.5	
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 12.5 V, I <sub>D</sub> = 24 A		108		S
DYNAMIC CHARACTERISTICS						
C <sub>ISS</sub>	Input capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 12.5 V, f = 1 MHz		1020	1300	pF
C <sub>OSS</sub>	Output capacitance			740	960	pF
C <sub>RSS</sub>	Reverse transfer capacitance			50	65	pF
R <sub>g</sub>	Series gate resistance	V <sub>DS</sub> = 12.5 V, I <sub>D</sub> = 24 A		1.4	2.8	Ω
Q <sub>g</sub>	Gate charge total (4.5 V)			6.2	8.4	nC
Q <sub>gd</sub>	Gate charge gate-to-drain			1.1		nC
Q <sub>gs</sub>	Gate charge gate-to-source			1.8		nC
Q <sub>g(th)</sub>	Gate charge at V <sub>th</sub>			1		nC
Q <sub>OSS</sub>	Output charge	V <sub>DS</sub> = 12.5 V, V <sub>GS</sub> = 0 V		14		nC
t <sub>d(on)</sub>	Turnon delay time	V <sub>DS</sub> = 12.5 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 24 A R <sub>G</sub> = 2 Ω		5.3		ns
t <sub>r</sub>	Rise time			15		ns
t <sub>d(off)</sub>	Turnoff delay time			13		ns
t <sub>f</sub>	Fall time			6.3		ns
DIODE CHARACTERISTICS						
V <sub>SD</sub>	Diode forward voltage	I <sub>S</sub> = 24 A, V <sub>GS</sub> = 0 V		0.85	1	V
Q <sub>rr</sub>	Reverse recovery charge	V <sub>DD</sub> = 12.5 V, I <sub>F</sub> = 24 A, di/dt = 300 A/μs		21		nC
t <sub>rr</sub>	Reverse recovery time	V <sub>DD</sub> = 12.5 V, I <sub>F</sub> = 24 A, di/dt = 300 A/μs		16		ns

### 5.2 Thermal Information

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

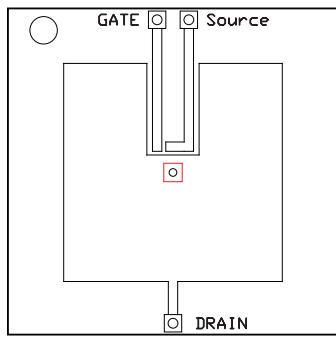
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance <sup>(1)</sup>			1.7	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)(2)</sup>			55	$^\circ\text{C}/\text{W}$

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.

# CSD16323Q3

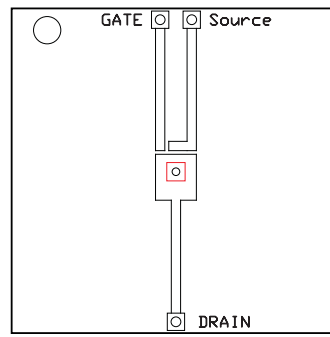
SLPS224C – AUGUST 2009 – REVISED NOVEMBER 2016

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M0161-01

Max  $R_{\theta JA} = 55^{\circ}\text{C/W}$   
when mounted on 1 in<sup>2</sup>  
of 2-oz Cu.

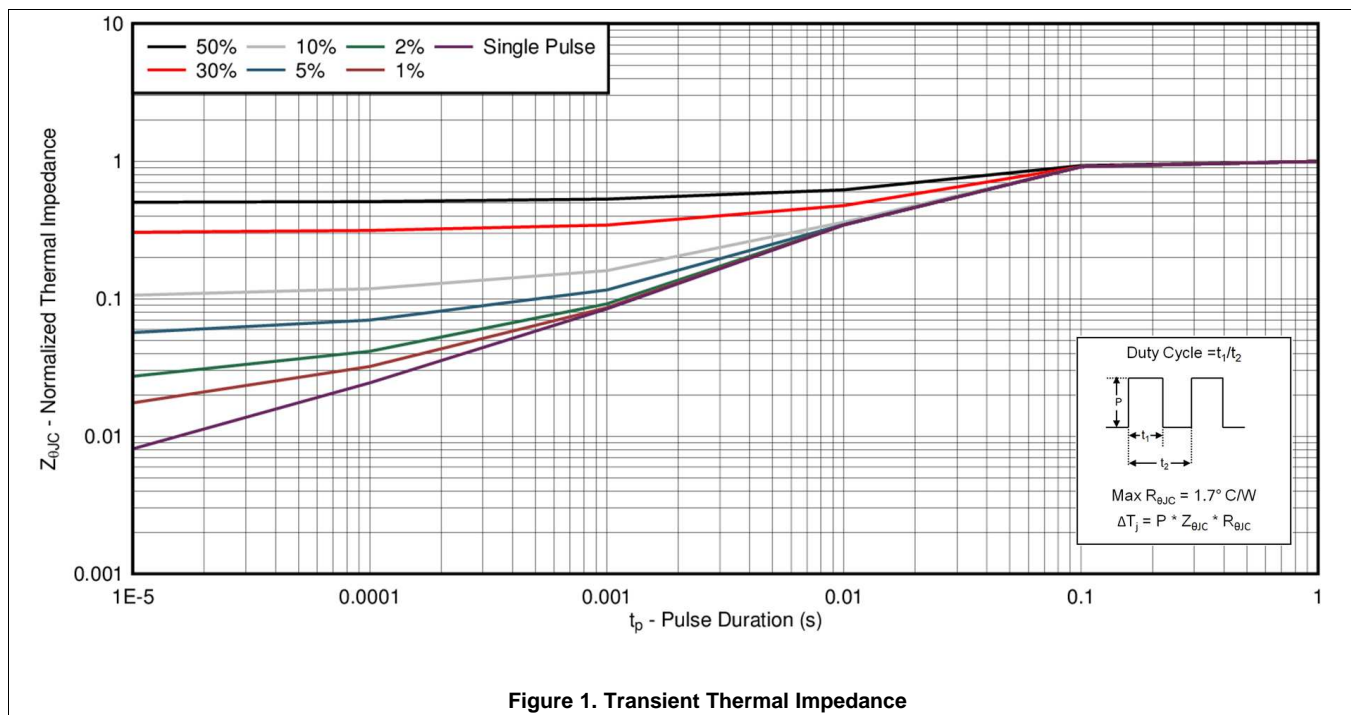


M0161-02

Max  $R_{\theta JA} = 160^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of  
2-oz Cu.

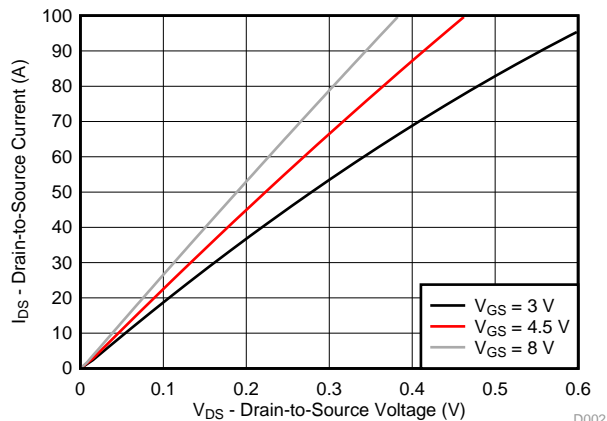
## 5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$  (unless otherwise stated)

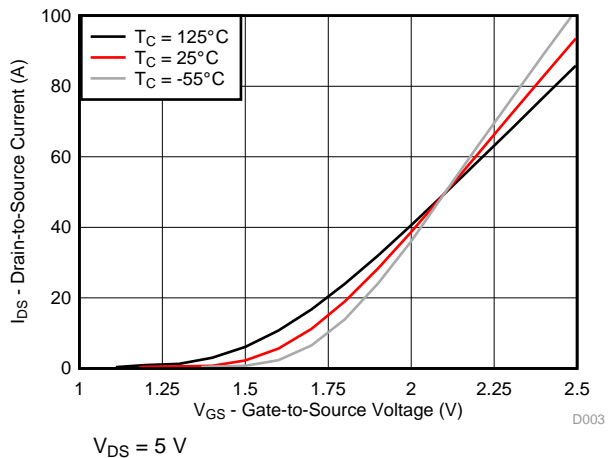


## Typical MOSFET Characteristics (continued)

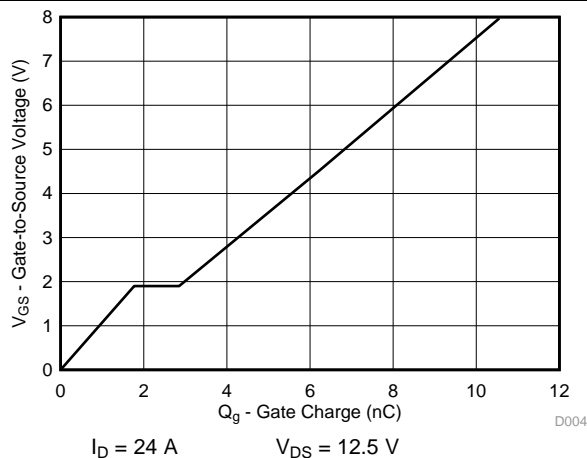
$T_A = 25^\circ\text{C}$  (unless otherwise stated)



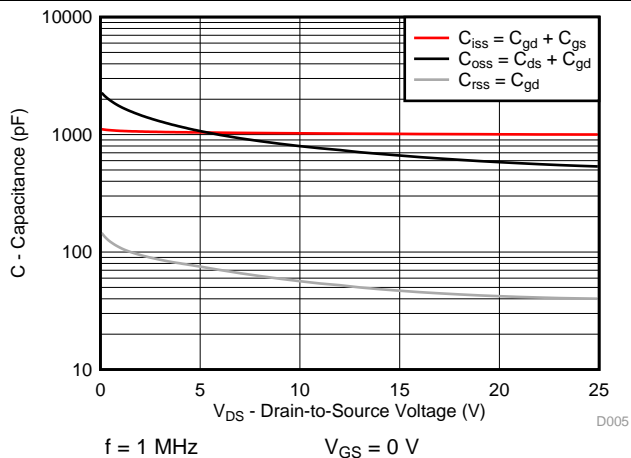
**Figure 2. Saturation Characteristics**



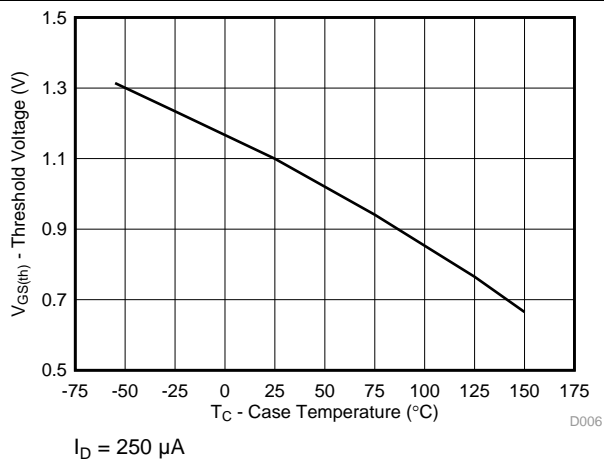
**Figure 3. Transfer Characteristics**



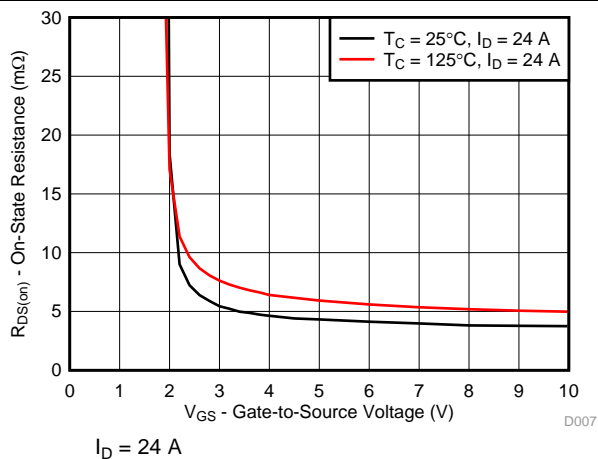
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Threshold Voltage vs Temperature**



**Figure 7. On Resistance vs Gate Voltage**

## Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

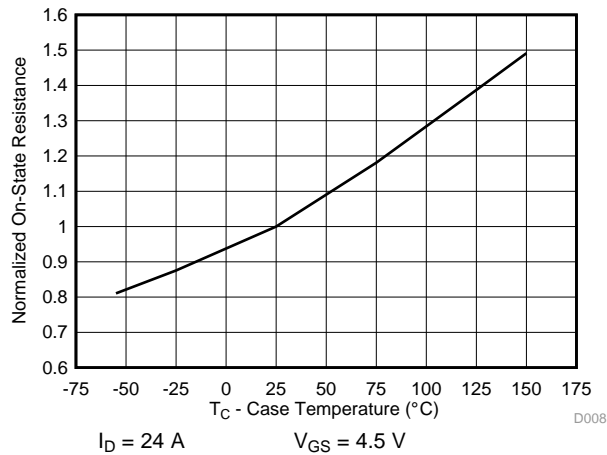


Figure 8. Normalized On Resistance vs Temperature

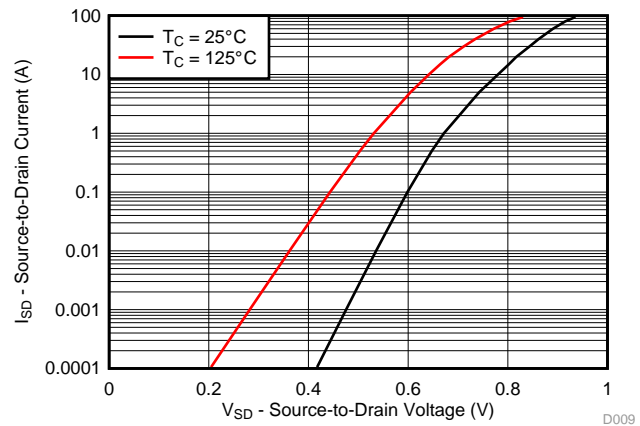


Figure 9. Typical Diode Forward Voltage

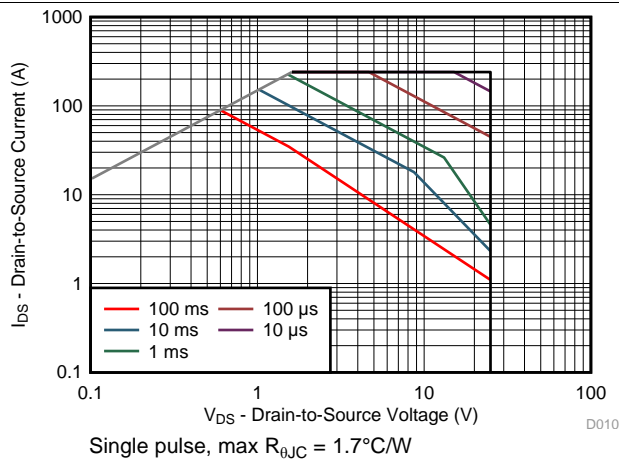


Figure 10. Maximum Safe Operating Area

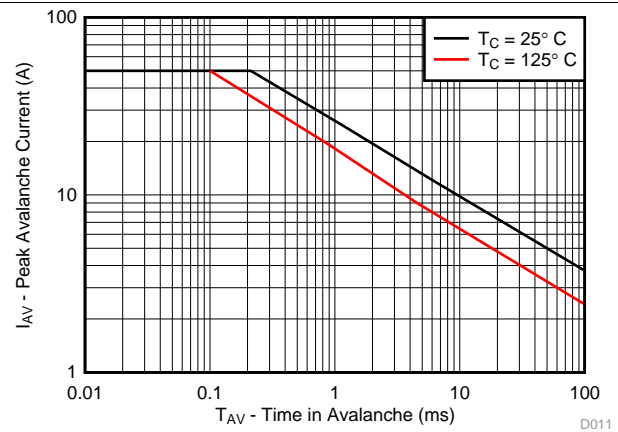


Figure 11. Single Pulse Unclamped Inductive Switching

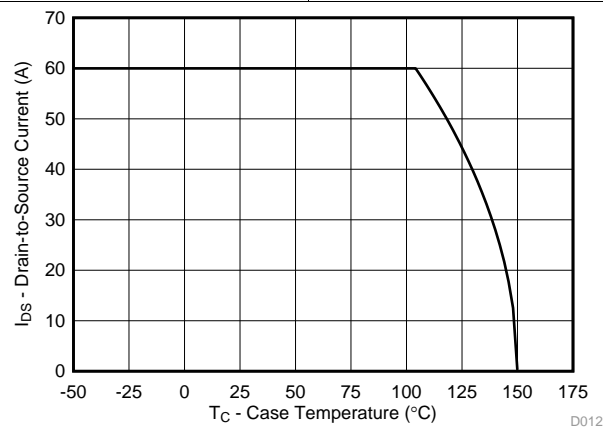


Figure 12. Maximum Drain Current vs Temperature

## 6 Device and Documentation Support

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.5 Glossary

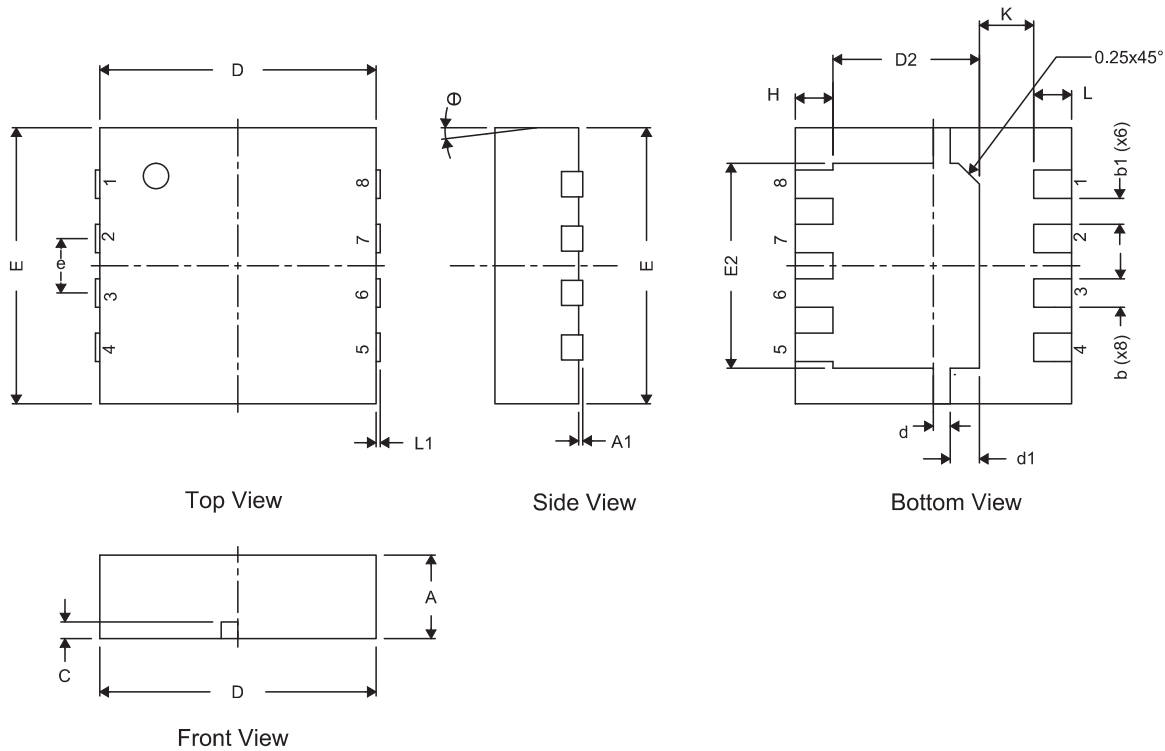
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

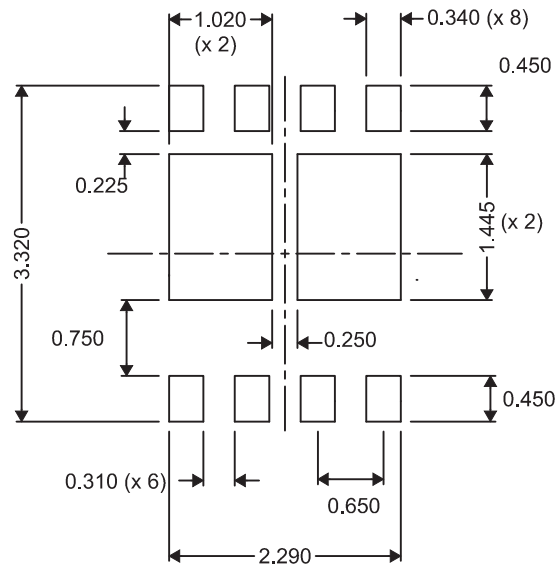
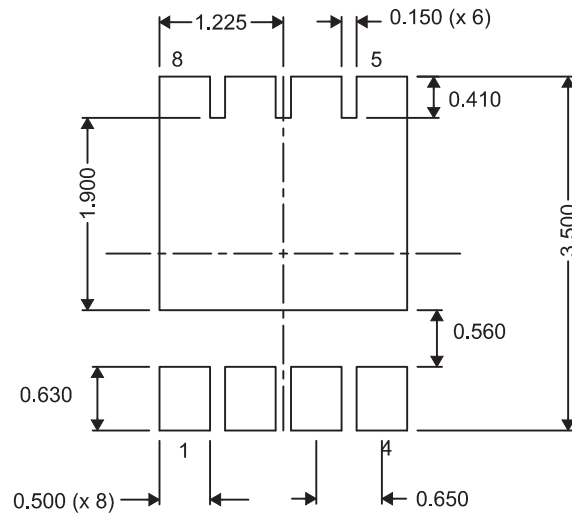
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Q3 Package Dimensions

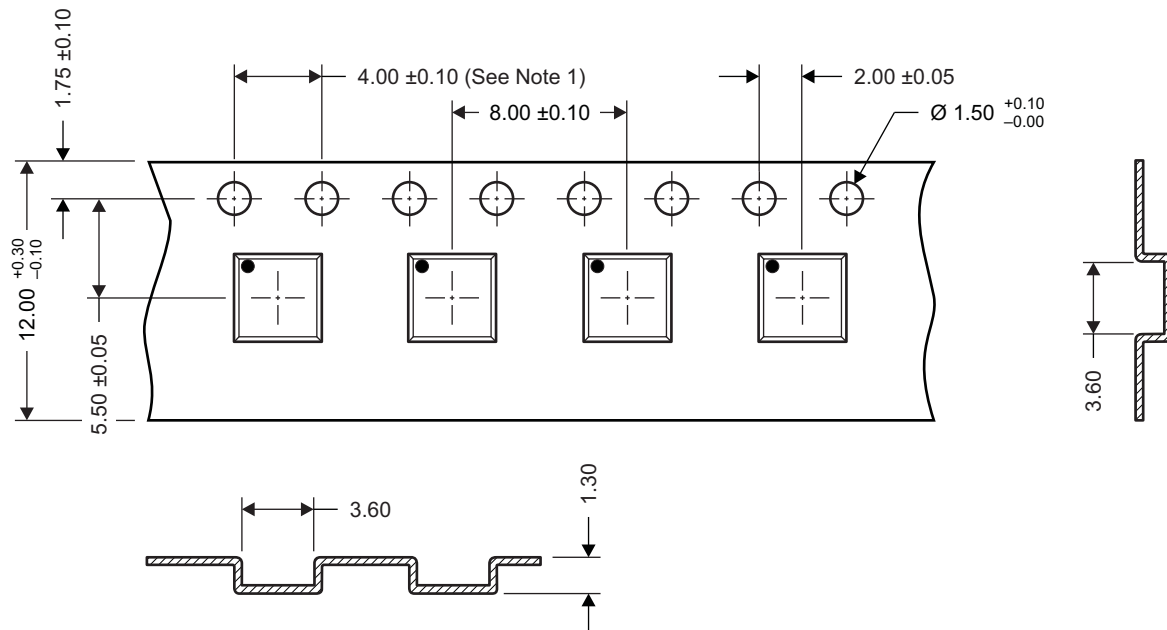


DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1	0.310 NOM			0.012 NOM		
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026 TYP		
H	0.35	0.450	0.550	0.014	0.018	0.022
K	0.650 TYP			0.026 TYP		
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
$\theta$	0	—	0	0	—	0





## 7.4 Q3 Tape and Reel Information



M0144-01

### Notes:

1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$ .
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm.
3. Material: black static dissipative polystyrene.
4. All dimensions are in mm (unless otherwise specified).
5. Thickness:  $0.30 \pm 0.05$  mm.
6. MSL1 260°C (IR and Convection) PbF-Reflow Compatible.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16323Q3	ACTIVE	VSON-CLIP	DQG	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-55 to 150	CSD16323	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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