UCC2912
UCC3912
PROGRAMMABLE HOT SWAP POWER MANAGER

SLUS241D − MARCH 1994 - REVISED NOVEMBER 2003

- **Integrated 0.15-Ω Power MOSFET**
- **3-V to 8-V Operation**
- **Digital Programmable Current Limit from 0 A to 3 A**
- **Electronic Circuit Breaker Function**
- **1μA I_{CC} When Disabled**
- **Programmable On-Time**
- **Programmable Start Delay**
- **Fixed 3% Duty Cycle**
- **Unidirectional Switch**
- **Thermal Shutdown**
- **Fault-Output Indicator**
- **Maximum-Output Current Can Be Set to 1 A Above the Programmed Fault Level or to a Full 4 A**
- **Power SOIC, Low-Thermal Resistance Packaging**

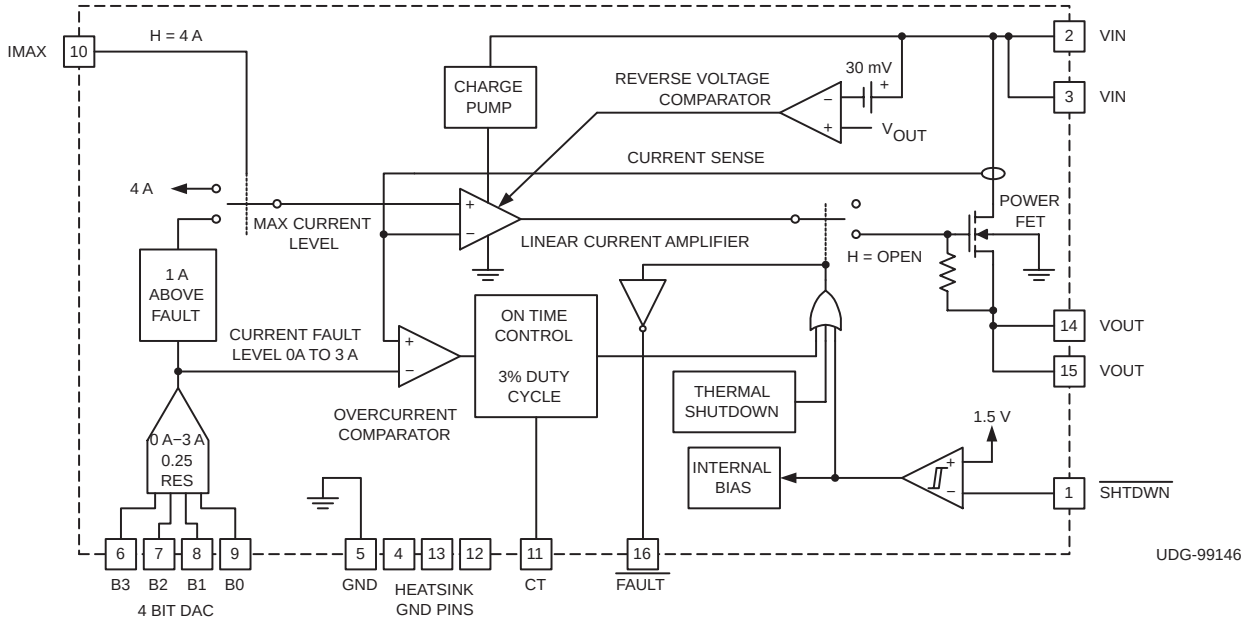
description

The UCC3912 family of hot swap power managers provides complete power management, hot swap capability, and circuit breaker functions. The only component required to operate the device, other than supply bypassing, is the fault timing capacitor, C_T. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output-sourcing current, maximum fault time, and startup delay. In the event of a constant fault, the internal fixed 3% duty cycle ratio limits average output power.

The internal 4-bit DAC allows programming of the fault level current from 0 A to 3 A with 0.25-A resolution. The IMAX control pin sets the maximum sourcing current to 1 A above the fault level when driven low, and to a full 4 A when driven high for applications which require fast output capacitor charging.

When the output current is below the fault level, the output MOSFET is switched on with a nominal on resistance of 0.15 Ω. When the output current exceeds the fault level, but is less than the maximum sourcing level, the output remains switched on, but the fault timer starts charging C_T. Once C_T charges to a preset threshold, the switch is turned off, and remains off for 30 times the programmed fault time. When the output current reaches the maximum sourcing level, the MOSFET transitions from a switch to a constant current source. (continued)

block diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description (continued)

The UCC3912 family is designed for unidirectional current flow, emulating an ideal diode in series with the power switch. This feature is particularly attractive in applications where many devices are powering a common bus, such as with SCSI Termpwr.

The UCC3912 family can be put into sleep mode drawing only 1-μA of supply current. The $\overline{\text{SHTDWN}}$ pin has a preset threshold hysteresis which allows the user the ability to set a time delay upon startup to achieve sequencing of power. Other features include an open drain $\overline{\text{FAULT}}$ output indicator, thermal shutdown, under voltage lockout, and a low thermal resistance small outline package.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†‡

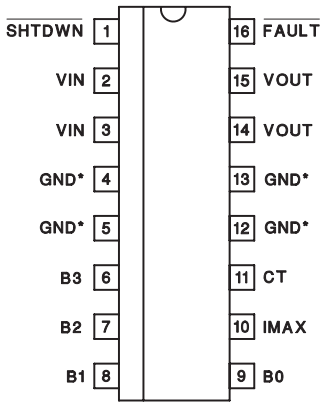
VIN	8 V
$\overline{\text{FAULT}}$ sink current	50 mA
$\overline{\text{FAULT}}$ voltage	-0.3 to V_{IN}
Output current	Self Limiting
Input voltage (B0, B1, B2, B3, IMAX, $\overline{\text{SHTDWN}}$)	-0.3 to V_{IN}
Storage temperature range, T_{stg}	-65°C to 150°C
Operating junction temperature range, T_J	-55°C to 150°C
Lead temperature (soldering, 10 sec.)	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Interface Products Data book (TI Literature Number SLUD002) for thermal limitations and considerations of packages.

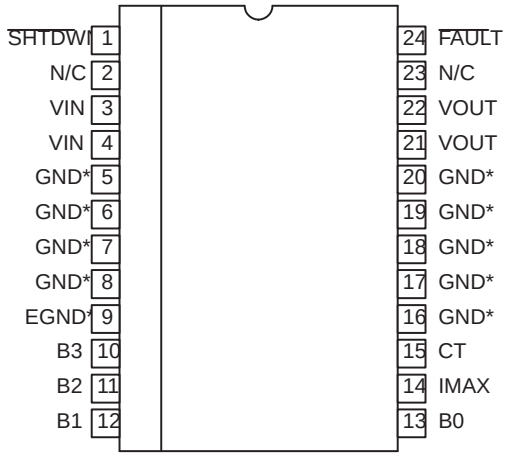
package information

DIL-16, SOIC-16
N, DP Package
(TOP VIEW)



*Pin 5 serves as lowest impedance to the electrical ground; Pins 4, 12, and 13 serve as heat sink/ground. These pins should be connected to large etch areas to help dissipate heat. For N package, pins 4, 12, and 13 are N/C.

TSSOP-24,
PWP Package
(TOP VIEW)



*Pin 9 serves as lowest impedance to the electrical ground; other GND pins serve as heat sink/ground. These pins should be connected to large etch areas to help dissipate heat.

electrical characteristics, these specifications apply for T_A = −40°C to 85°C for the UCC2912; T_A = 0°C to 70°C for the UCC3912, VIN = 5 V, IMAX = 0.4 V, $\overline{SHTDWN}$ = 2.4 V (unless otherwise stated)

supply section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage input range		3.0		8.0	V
Supply current			1.0	2.0	mA
Sleep mode current	$\overline{SHTDWN}$ = 0.2 V		0.5	5.0	µA

NOTE 1: All voltages are with respect to ground. Current is positive into and negative out of the specified terminal.

output section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage drop	I_{OUT} = 1 A		0.15	0.22	V
	I_{OUT} = 2 A		0.3	0.45	V
	I_{OUT} = 3 A		0.45	0.68	V
	I_{OUT} = 1A, VIN = 3 V		0.17	0.27	V
	I_{OUT} = 2 A, VIN = 3 V		0.35	0.56	V
	I_{OUT} = 3 A, VIN = 3 V		0.5	0.8	V
Reverse leakage current	$V_{IN} < V_{OUT}$, $\overline{SHTDWN}$ = 0.2 V, V_{OUT} = 5 V		5	20	µA
Initial startup time	See Note 2		100		µs
Short circuit response	See Note 2		100		ns
Thermal shutdown	See Note 2		170		°C
Thermal hysteresis	See Note 2		10		°C

NOTE 1: All voltages are with respect to ground. Current is positive into and negative out of the specified terminal.
NOTE 2: Ensured by design. Not production tested.

DAC section

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output leakage		Code = 0000−0011			0	20	µA
Trip current		Code = 0100		0.1	0.25	0.45	A
		Code = 0101		0.25	0.50	0.75	A
		Code = 0110		0.5	0.75	1.0	A
		Code = 0111		0.75	1.00	1.25	A
		Code = 1000		1.0	1.25	1.5	A
		Code = 1001		1.25	1.50	1.75	A
		Code = 1010		1.5	1.75	2.0	A
		Code = 1011		1.7	2.00	2.3	A
		Code = 1100		1.9	2.25	2.58	A
		Code = 1101		2.1	2.50	2.9	A
		Code = 1110		2.3	2.75	3.2	A
		Code = 1111		2.5	3.0	3.5	A
Maximum output current		Code = 0000 to 0011				0.02	mA
Maximum output current over trip (current source mode)	UCC2912	Code = 0100 to 1111,	I_{MAX} = 0 V	0.5	1.0	2.0	A
	UCC3912	Code = 0100 to 1111,	I_{MAX} = 0 V	0.5	1.0	1.8	A
Maximum output current (current source mode)		Code = 0100 to 1111,	I_{MAX} = 2.4 V	3.0	4.0	5.2	A

NOTE 1: All voltages are with respect to ground. Current is positive into and negative out of the specified terminal.

electrical characteristics, these specifications apply for T_A = −40°C to 85°C for the UCC2912; T_A = 0°C to 70°C for the UCC3912, VIN = 5 V, IMAX = 0.4 V, $\overline{SHTDWN}$ = 2.4 V (unless otherwise stated)

timer section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
CT charge current		V_{CT} = 1.0 V	−45.0	-36.0	−22.0	µA
CT discharge current	UCC2912	V_{CT} = 1.0 V	0.72	1.20	1.57	µA
	UCC3912	V_{CT} = 1.0 V	0.72	1.20	1.50	µA
Output duty cycle		V_{OUT} = 0 V	2.0	3.0	6.0	%
CT fault threshold			1.3	1.5	1.7	V
CT reset threshold			0.4	0.5	0.6	V

NOTE 1: All voltages are with respect to ground. Current is positive into and negative out of the specified terminal.

shutdown section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown threshold		1.1	1.5	1.9	V
Shutdown hysteresis			100		mV
Input current	$\overline{SHTDWN}$ = 1 V		100	500	nA

fault output section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output leakage current				500	nA
Low level output voltage	I_{OUT} = 10 mA		0.4	0.8	V

TTL input dc characteristics section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TTL input voltage high	(can be connected to V_{IN})	2.0			V
TTL input voltage low				0.8	V
TTL input high current	V_{IH} = 2.4 V		3	10	µA
TTL input low current	V_{IL} = 0.4 V			1	µA

NOTE 1: All voltages are with respect to ground. Current is positive into and negative out of the specified terminal.

pin description

B0−B3: These pins provide digital input to the DAC which sets the fault current threshold. They can be used to provide a digital soft-start, adaptive current limiting.

CT: A capacitor connected to ground sets the maximum fault time. The maximum fault time must be more than the time to charge the external capacitance in one cycle. The maximum fault time is defined as FAULT = $27.8 \times 10^3 \times$ CT. Once the fault time is reached the output will shutdown for a time given by: $T_{SD} = 833 \times 10^3 \times$ CT, this equates to a 3% duty cycle.

$\overline{FAULT}$: Open drain output which pulls low upon any condition which causes the output to open: fault, thermal shutdown, or shutdown.

IMAX: When this pin is set to logic low the maximum sourcing current will always be 1 A above the programmed fault level. When set to logic high, the maximum sourcing current will be a constant 4 A for applications which require fast charging of load capacitance.

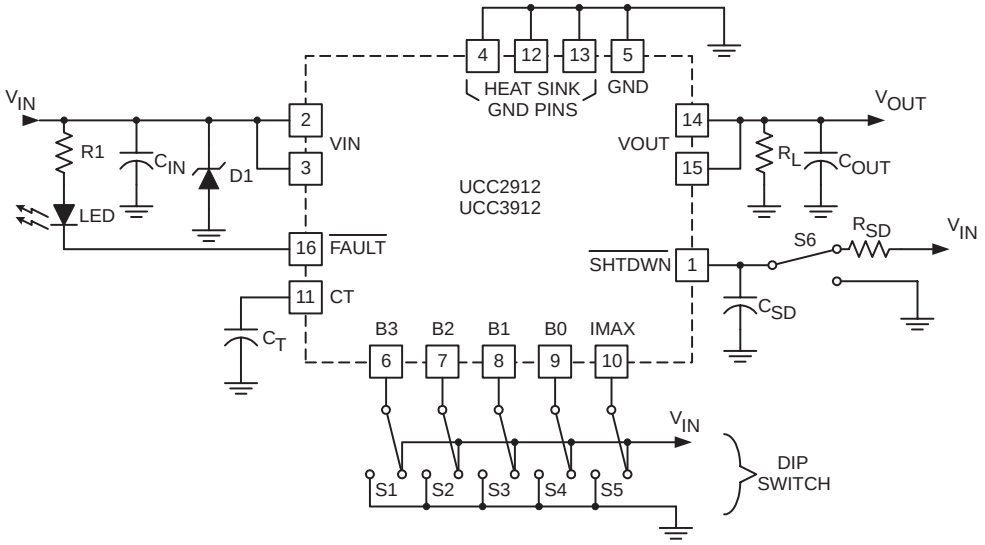
pin description (continued)

$\overline{\text{SHTDWN}}$: When this pin is brought to a logic low, the IC is put into a sleep mode drawing typically less than 1 μA of I_{CC}. The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit.

VIN: Input voltage to the UCC3912. The recommended voltage range is 3 V to 8 V. Both VIN pins should be connected together and to the power source.

VOUT: Output voltage from the UCC3912. When switched the output voltage will be approximately $V_{IN} - (0.15\ \Omega \times I_{OUT})$. Both VOUT pins should be connected together and to the load.

APPLICATION INFORMATION



NOTE: For demonstration board schematic see Design Note DN-58 (TI Literature Number SLUA187).

UDG-99171

Figure 1. Evaluation Circuit

protecting the UCC3912 from voltage transients

The parasitic inductance associated with the power distribution can cause a voltage spike at V_{IN} if the load current is suddenly interrupted by the UCC3912. It is important to limit the peak of this spike to less than 8 V to prevent damage to the UCC3912. This voltage spike can be minimized by:

- Reducing the power distribution inductance (e.g., twist the positive and negative leads of the power supply feeding V_{IN}, locate the power supply close to the UCC3912, use a PCB ground plane,...etc.).
- Decoupling V_{IN} with a capacitor, C_{IN} (refer to Figure 1), located close to pins 2 and 3. This capacitor is typically less than 1 μF to limit the inrush current.
- Clamping the voltage at V_{IN} below 8 V with a zener diode, D1 (refer to Figure 1), located close to pins 2 and 3.

APPLICATION INFORMATION

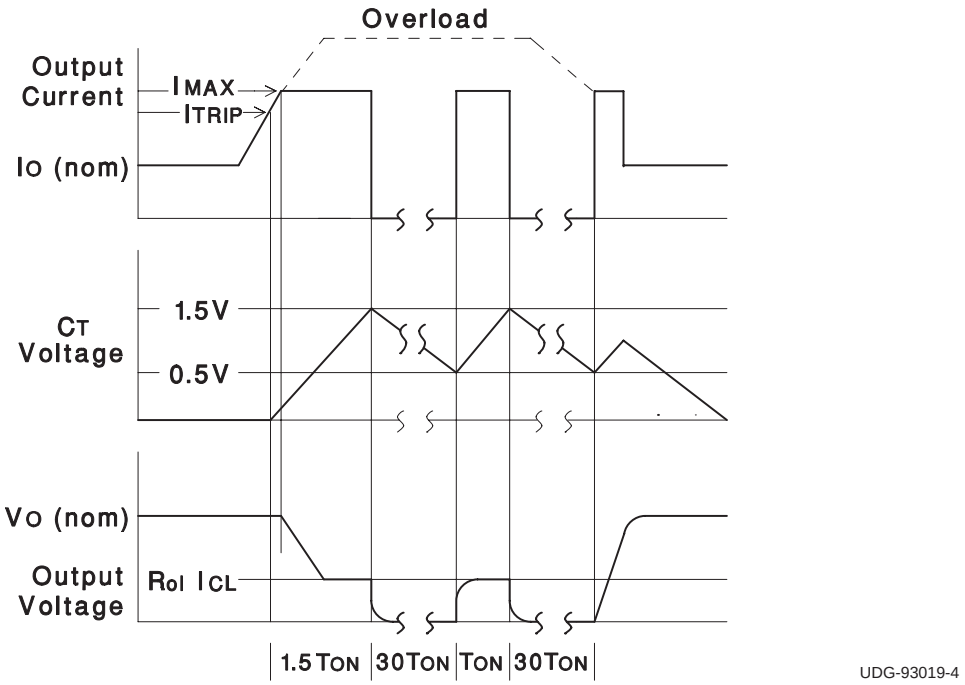


Figure 2. Load Current, Timing-Capacitor Voltage, and Output Voltage of the UCC3912 Under Fault Conditions.

estimating maximum load capacitance

For hot-swap applications, the rate at which the total output capacitance can be charged depends on the maximum output current available and the nature of the load. For a constant-current current-limited controller, the output will come up if the load asks for less than the maximum available short-circuit current.

To ensure recovery of a duty-cycle from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time (fault time). The design value of ON or fault time can be adjusted by changing the timing capacitor C_T.

For worst-case constant-current load of value just less than the trip limit; $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \approx \left(I_{MAX} - I_{LOAD}\right) \times \left(\frac{28 \times 10^3 \times CT}{V_{OUT}}\right)$$

where V_{OUT} is the output voltage.

APPLICATION INFORMATION

For a resistive load of value RL, the value of $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \approx \left(\frac{28 \times 10^3 \times CT}{RL \times \ell n \left(\frac{1}{1 - \left(\frac{V_{OUT}}{I_{MAX} \times RL} \right)} \right)} \right)$$

The overcurrent comparator senses both the DAC output and a representation of the output current. When the output current exceeds the programmed level the timing capacitor C_T charges with 36 μA of current. If the fault occurs for the time it takes for C_T to charge up to 1.5 V, the fault latch is set and the output switch is opened. The output remains opened until C_T discharges to 0.5 V with a 1.2-μA current source. Once the 0.5 V is reached the output is enabled and will either appear as a switch, if the fault is removed, or a current source if the fault remains. If the over current condition is still present, then C_T will begin charging, starting the cycle over, resulting in approximately a 3% on time.

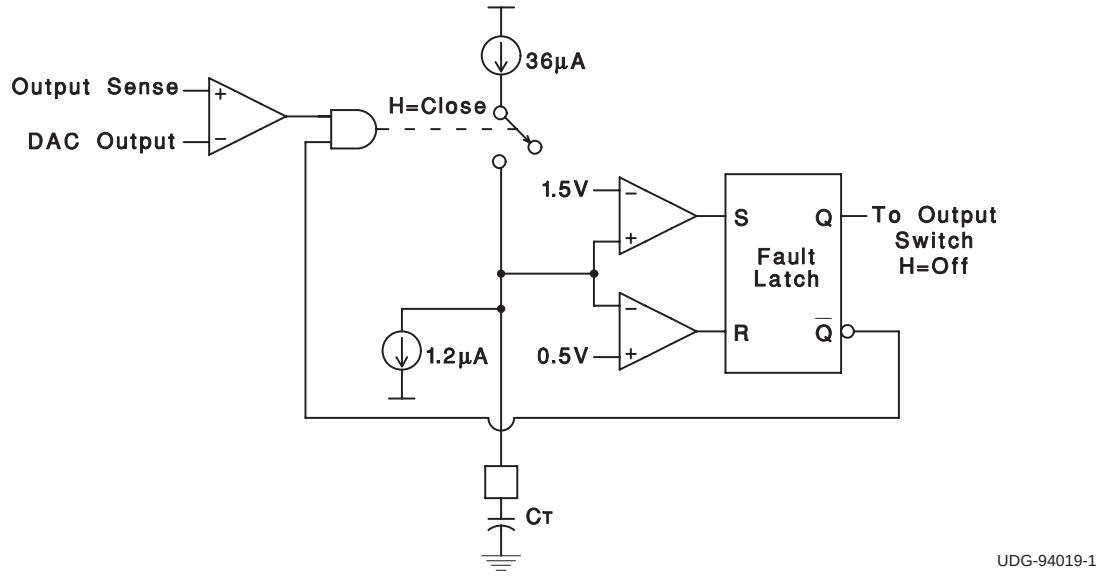


Figure 3. UCC3912 On-Time Circuitry

APPLICATION INFORMATION

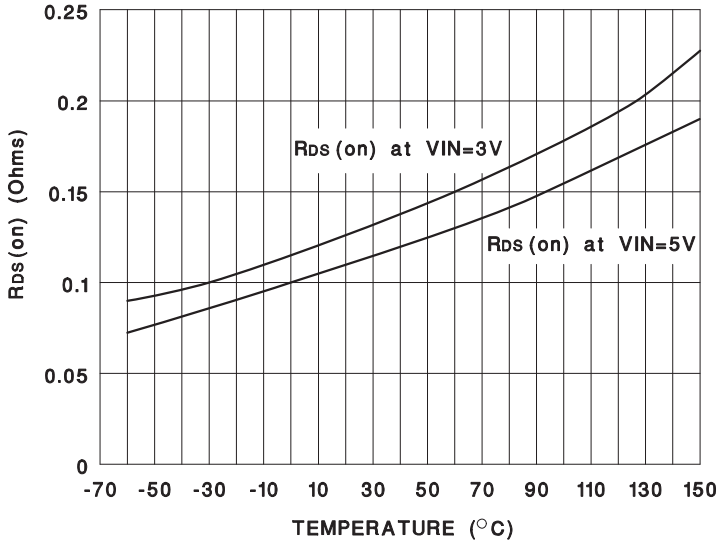


Figure 4. $R_{DS(on)}$ vs. Temperature at 2-A Load Current.

safety recommendations

Although the UCC3912 family is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3912 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3912 will prevent the fuse from blowing virtually for all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC2912DP	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2912DP
UCC2912DP.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2912DP
UCC2912PWP	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2912PWP
UCC2912PWP.A	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2912PWP
UCC3912DP	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3912DP
UCC3912DP.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3912DP
UCC3912PWP	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3912PWP
UCC3912PWP.A	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3912PWP
UCC3912PWPG4	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3912PWP
UCC3912PWPTR	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3912PWP
UCC3912PWPTR.A	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3912PWP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

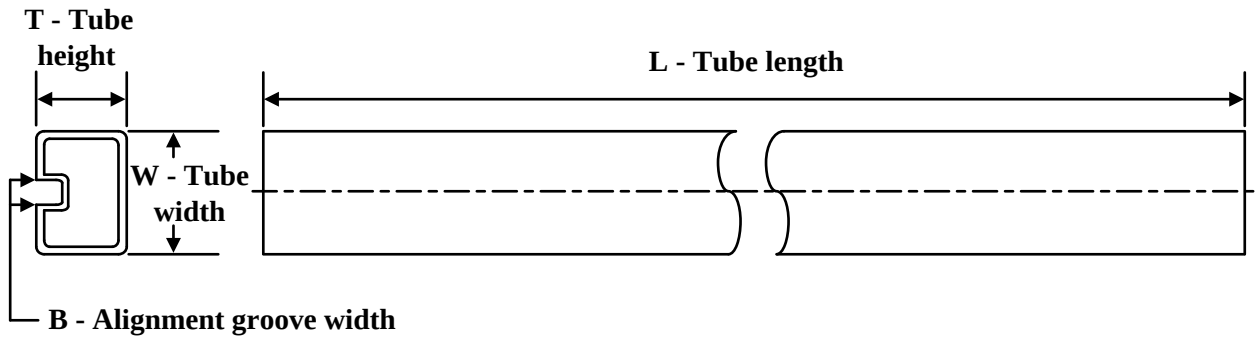
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

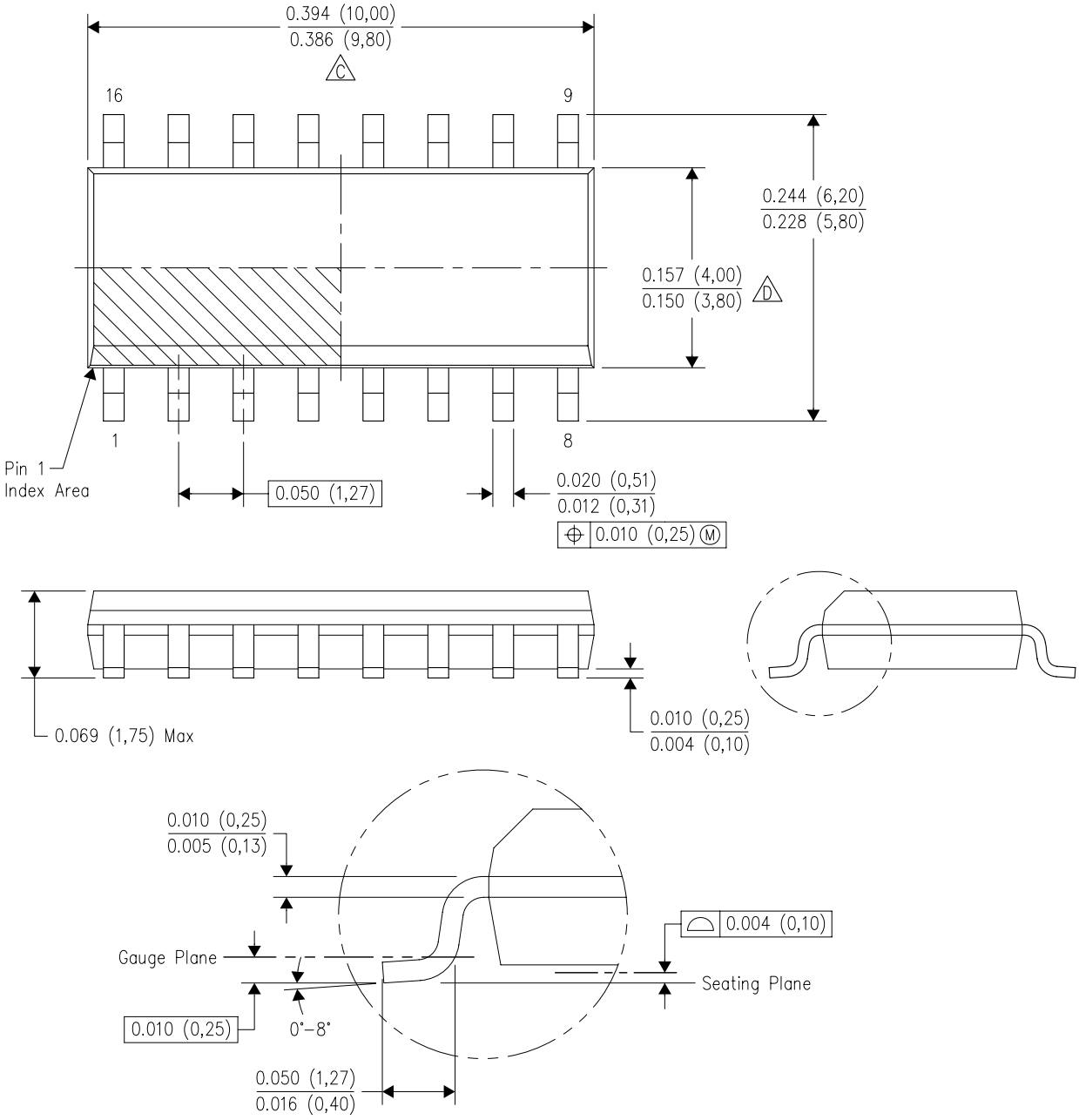
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC2912DP	D	SOIC	16	40	506.6	8	3940	4.32
UCC2912DP.A	D	SOIC	16	40	506.6	8	3940	4.32
UCC2912PWP	PW	TSSOP	24	60	530	10.2	3600	3.5
UCC2912PWP.A	PW	TSSOP	24	60	530	10.2	3600	3.5
UCC3912DP	D	SOIC	16	40	506.6	8	3940	4.32
UCC3912DP.A	D	SOIC	16	40	506.6	8	3940	4.32
UCC3912PWP	PW	TSSOP	24	60	530	10.2	3600	3.5
UCC3912PWP.A	PW	TSSOP	24	60	530	10.2	3600	3.5
UCC3912PWPG4	PW	TSSOP	24	60	530	10.2	3600	3.5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



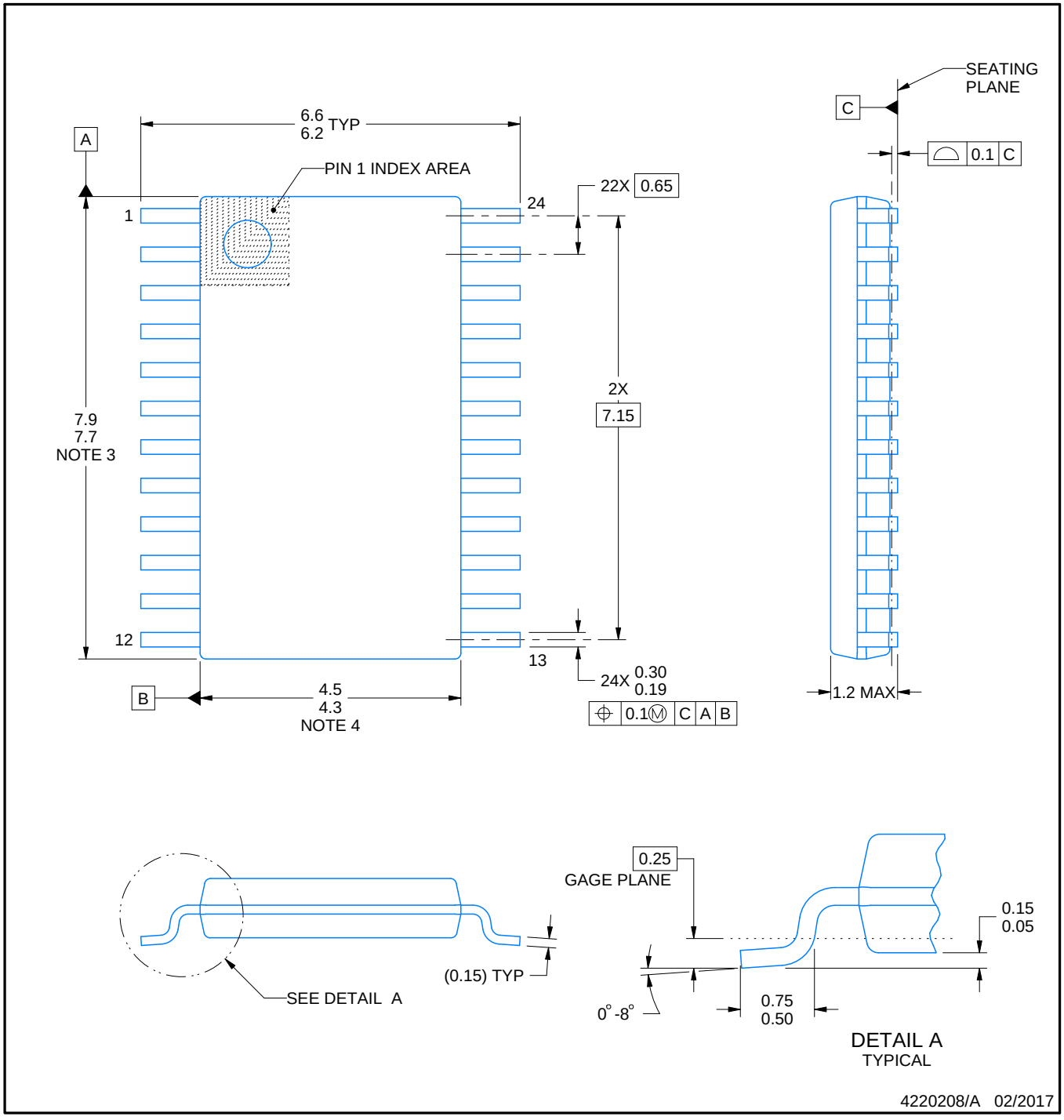
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0024A

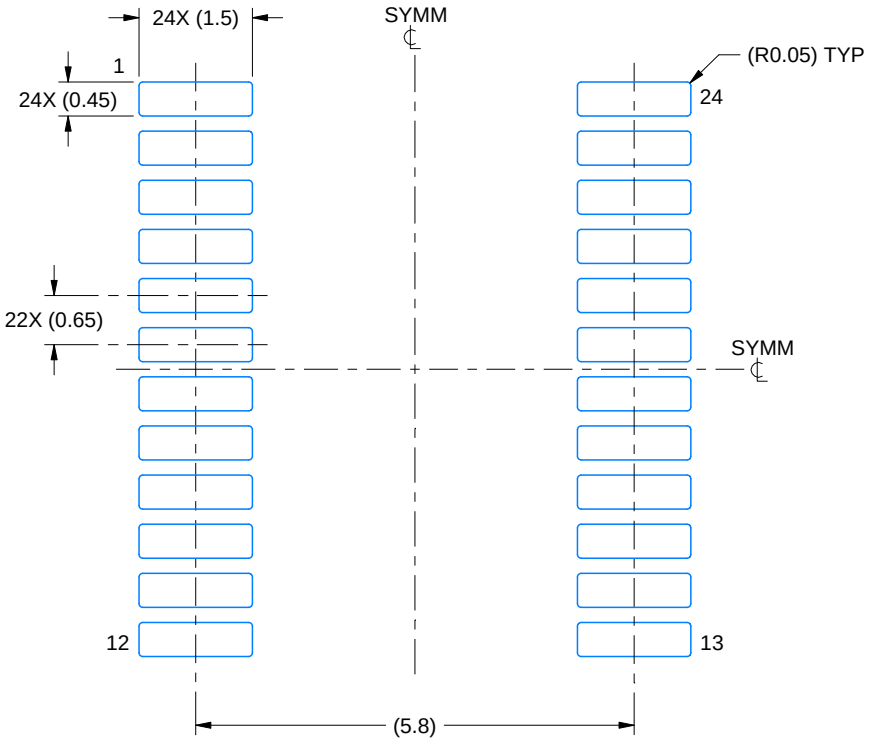
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

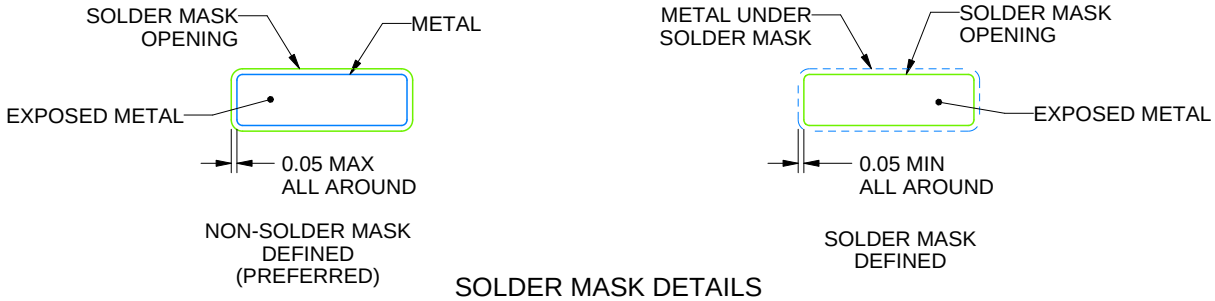


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

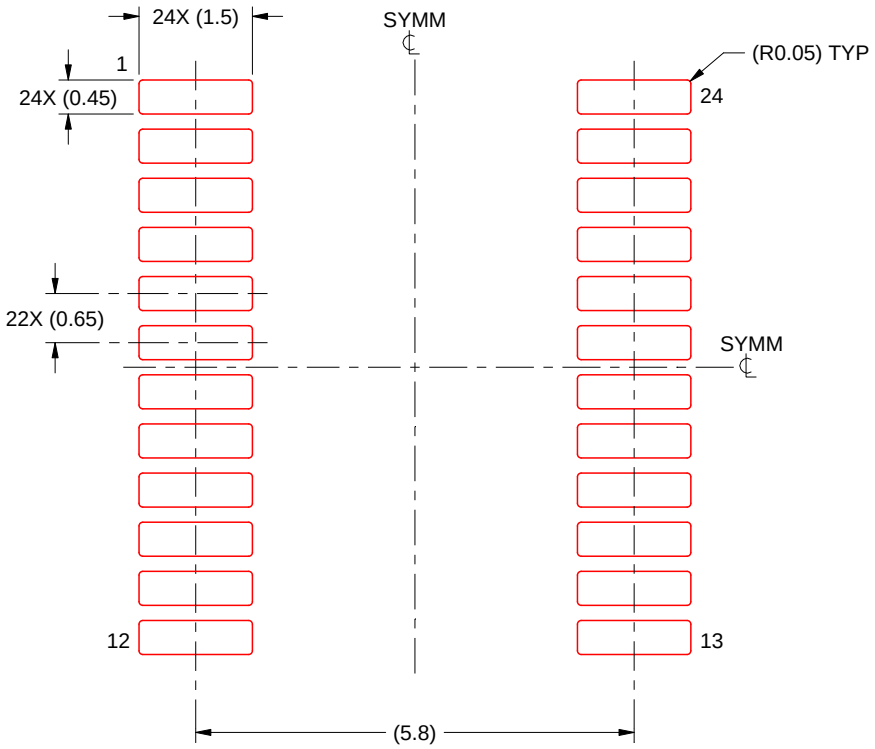


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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