12-/14-/16-Bit, Octal Channel, Ultra-Low Glitch, Voltage Output DIGITAL-TO-ANALOG CONVERTERS with 2.5V, 2ppm/°C Internal Reference

FEATURES

- **Relative Accuracy:**
  - **DAC7568 (12-Bit): 0.5 LSB INL**
  - **DAC8168 (14-Bit): 2 LSB INL**
  - **DAC8568 (16-Bit): 8 LSB INL**
- **Glitch Energy: 0.15nV-s**
- **Internal Reference:**
  - **2.5V Reference Voltage (disabled by default)**
  - **0.004% Initial Accuracy (typ)**
  - **2ppm/°C Temperature Drift (typ)**
  - **5ppm/°C Temperature Drift (max)**
  - **20mA Sink/Source Capability**
- **Power-On Reset to Zero-Scale or Mid-Scale**
- **Ultra-Low Power Operation: 0.15mA/Channel at 5V**
- **Wide Power-Supply Range: +2.7V to +5.5V**
- **Monotonic Over Entire Temperature Range**
- **Settling Time: 10μs to ±0.024% Full-Scale Range (FSR)**
- **Low-Power Serial Interface with Schmitt-Triggered Inputs: Up to 50MHz**
- **On-Chip Output Buffer Amplifier with Rail-to-Rail Operation**
- **Temperature Range: –40°C to +125°C**

APPLICATIONS

- **Portable Instrumentation**
- **Closed-Loop Servo-Control/Process Control**
- **Data Acquisition Systems**
- **Programmable Attenuation, Digital Gain, and Offset Adjustment**
- **Programmable Voltage and Current Sources**

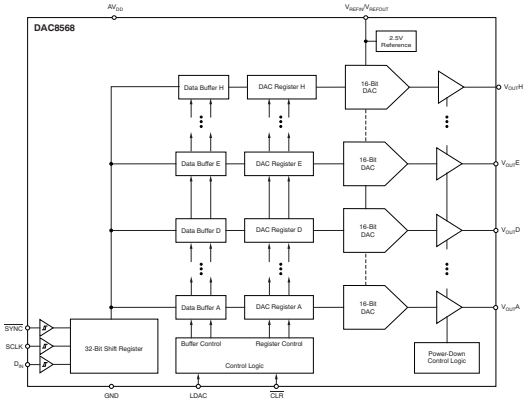
RELATED DEVICES	12-BIT	14-BIT	16-BIT
Pin- and Function-Compatible	DAC7568	DAC8168	DAC8568

DESCRIPTION

The DAC7568, DAC8168, and DAC8568 are low-power, voltage-output, eight-channel, 12-, 14-, and 16-bit digital-to-analog converters (DACs), respectively. These devices include a 2.5V, 2ppm/°C internal reference (disabled by default), giving a full-scale output voltage range of 2.5V or 5V. The internal reference has an initial accuracy of 0.004% and can source up to 20mA at the $V_{REF}IN/V_{REF}OUT$ pin. The device is monotonic, provides very good linearity, and minimizes undesired code-to-code transient voltages (glitch). The DAC7568, DAC8168, and DAC8568 use a versatile 3-wire serial interface that operates at clock rates up to 50MHz. The interface is compatible with standard SPI™, QSPI™, Microwire™, and digital signal processor (DSP) interfaces.

The DAC7568, DAC8168, and DAC8568 incorporate a power-on-reset circuit that ensures the DAC output powers up at either zero-scale or mid-scale until a valid code is written to the device. These devices contain a power-down feature, accessed over the serial interface, that reduces the current consumption of the device to typically 2μA at 5V. Power consumption is typically 3mW at 3V, reducing to 1μW in power-down mode. The low power consumption, internal reference, and small footprint make this device ideal for portable, battery-operated equipment.

The DAC7568, DAC8168, and DAC8568 are drop-in and functionally compatible with each other. The devices are available in TSSOP-16 and TSSOP-14 packages.



PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SPI, QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor.
All other trademarks are the property of their respective owners.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)	MAXIMUM REFERENCE DRIFT (ppm/°C)	OUTPUT VOLTAGE FULL-SCALE RANGE	RESET TO	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DAC8568A	±12	±1	25	2.5V	Zero	TSSOP-16	PW	–40°C to +125°C	DA8568A
DAC8568B	±12	±1	25	2.5V	Mid-Scale	TSSOP-16	PW	–40°C to +125°C	DA8568B
DAC8568C	±12	±1	5	5V	Zero	TSSOP-16	PW	–40°C to +125°C	DA8568C
DAC8568D	±12	±1	5	5V	Mid-Scale	TSSOP-16	PW	–40°C to +125°C	DA8568D
DAC8168A	±4	±1	25	2.5V	Zero	TSSOP-14	PW	–40°C to +125°C	DA8168A
DAC8168C	±4	±1	5	5V	Zero	TSSOP-16	PW	–40°C to +125°C	DA8168C
DAC7568A	±1	±1	25	2.5V	Zero	TSSOP-14	PW	–40°C to +125°C	DA7568A
DAC7568C	±1	±1	5	5V	Zero	TSSOP-16	PW	–40°C to +125°C	DA7568C

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	DAC7568/DAC8168/DAC8568	UNIT
AV_{DD} to GND	–0.3 to +6	V
Digital input voltage to GND	–0.3 to $+V_{DD}$ + 0.3	V
V_{OUT} to GND	–0.3 to $+V_{DD}$ + 0.3	V
V_{REF} to GND	–0.3 to $+V_{DD}$ + 0.3	V
Operating temperature range	–40 to +125	°C
Storage temperature range	–65 to +150	°C
Junction temperature range (T_J max)	+150	°C
Power dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$	W
Thermal impedance, θ_{JA}	+118	°C/W
Thermal impedance, θ_{JC}	+29	°C/W

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

At AV_{DD} = 2.7V to 5.5V and –40°C to +105°C range, unless otherwise noted.

PARAMETER		TEST CONDITIONS	DAC7568/DAC8168/DAC8568 MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)						
DAC8568	Resolution		16			Bits
	Relative accuracy	Measured by the line passing through codes 485 and 64714		±8	±12	LSB
	Differential nonlinearity	16-bit monotonic		±0.5	±1	LSB
DAC8168	Resolution		14			Bits
	Relative accuracy	Measured by the line passing through codes 120 and 16200		±2	±4	LSB
	Differential nonlinearity	14-bit monotonic		±0.25	±0.5	LSB
DAC7568	Resolution		12			Bits
	Relative accuracy	Measured by the line passing through codes 30 and 4050		±0.5	±1	LSB
	Differential nonlinearity	12-bit monotonic		±0.15	±0.3	LSB
Offset error		Extrapolated from two-point line(2), unloaded		0.5	10	mV
Offset error drift				3		µV/°C
Full-scale error		DAC register loaded with all '1's		±0.2	±0.5	% of FSR
Zero-code error		DAC register loaded with all '0's		0.5	10	mV
Zero-code error drift				5		µV/°C
Gain error		Extrapolated from two-point line(2), unloaded		±0.05	±0.15	% of FSR
Gain temperature coefficient		AV_{DD} = 5V		1		ppm of FSR/°C
		AV_{DD} = 2.7V		3		
PSRR		Output unloaded		1		mV/V
OUTPUT CHARACTERISTICS(3)						
Output voltage range		V_{DD} ≥ 2.7V; grades A and B: maximum output voltage 2.5V when using internal reference	0		V_{DD}	V
		V_{DD} ≥ 5V; grades C and D: maximum output voltage 5V when using internal reference				
Output voltage settling time		To ±0.024% FSR, 0020h to 3FD0h, R_L = 2kΩ, 0pF < C_L < 200pF; 1/4 scale to 3/4 scale		6	10	µs
		R_L = 2MΩ, C_L = 470pF		12		
Slew rate				0.5		V/µs
Capacitive load stability		R_L = ∞		470		pF
		R_L = 2kΩ		1000		
Code change glitch impulse		1LSB change around major carry		0.15		nV-s
Digital feedthrough		SCLK toggling, $\overline{SYNC}$ high		0.15		nV-s
Channel-to-channel dc crosstalk		Full-scale swing on adjacent channel		0.25		LSB
Channel-to-channel ac crosstalk		1kHz full-scale sine wave, outputs unloaded		–100		dB
DC output impedance		At mid-code input		1		Ω
Short-circuit current				50		mA
Power-up time		Coming out of power-down mode, AV_{DD} = 5V		2.5		µs
		Coming out of power-down mode, AV_{DD} = 3V		5		

(1) Linearity calculated using a reduced code range of 30 to 4050; output unloaded.
(2) 16-bit: 485 and 64714; 14-bit: 120 and 16200; 12-bit: 30 and 4050
(3) Specified by design or characterization; not production tested.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

At AV_{DD} = 2.7V to 5.5V and –40°C to +105°C range, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DAC7568/DAC8168/DAC8568 MIN	TYP	MAX	UNIT
AC PERFORMANCE(4)					
SNR	T_A = +25°C, BW = 20kHz, V_{DD} = 5V, f_{OUT} = 1kHz. First 19 harmonics removed for SNR calculation.		88		dB
THD			–77		dB
SFDR			77		dB
SINAD			76		dB
DAC output noise density	T_A = +25°C, at mid-code input, f_{OUT} = 1kHz		120		nV/√Hz
DAC output noise	T_A = +25°C, at mid-code input, 0.1Hz to 10Hz		6		μV_{PP}
REFERENCE					
Internal reference current consumption	AV_{DD} = 5.5V		360		µA
	AV_{DD} = 3.6V		348		µA
External reference current	External V_{REF} = 2.5V (when internal reference is disabled), all eight channels active		80		µA
V_{REF}IN Reference input range	TBD	0		AV_{DD}	V
	TBD	0		AV_{DD}/2	V
Reference input impedance			8		kΩ
REFERENCE OUTPUT					
Output voltage	T_A = +25°C; all grades	2.4995	2.5	2.5005	V
Initial accuracy	T_A = +25°C, all grades	–0.02	±0.004	0.02	%
Output voltage temperature drift	DAC8568/DAC8168/DAC7568(5); grades A, B		5	25	ppm/°C
	DAC8568/DAC8168/DAC7568(6); grades C, D		2	5	
Output voltage noise	f = 0.1Hz to 10Hz		12		μV_{PP}
Output voltage noise density (high-frequency noise)	T_A = +25°C, f = 1MHz, C_L = 0µF		50		nV/√Hz
	T_A = +25°C, f = 1MHz, C_L = 1µF		20		
	T_A = +25°C, f = 1MHz, C_L = 4µF		16		
Load regulation, sourcing	T_A = +25°C		30		µV/mA
Load regulation, sinking	T_A = +25°C		15		µV/mA
Output current load capability(4)			±20		mA
Line regulation	T_A = +25°C		10		µV/V
Long-term stability/drift (aging)	T_A = +25°C, time = 0 to 1900 hours		50		ppm
Thermal hysteresis	First cycle		100		ppm
	Additional cycles		25		
LOGIC INPUTS(4)					
Input current			±1		µA
V_{IN}L Logic input LOW voltage	2.7V ≤ IOV_{DD} ≤ 5.5V			0.8	V
	1.8V ≤ IOV_{DD} ≤ 2.7V			0.5	
V_{IN}H Logic input HIGH voltage	2.7V ≤ IOV_{DD} ≤ 5.5V	1.8			V
	1.8V ≤ IOV_{DD} ≤ 2.7V	1.1			
Pin capacitance				3	pF

(4) Specified by design or characterization; not production tested.
(5) Reference is trimmed and tested at room temperature, and is characterized from –40°C to +120°C.
(6) Reference is trimmed and tested at two temperatures (+25°C and +105°C), and is characterized from –40°C to +120°C.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

At AV_{DD} = 2.7V to 5.5V and –40°C to +105°C range, unless otherwise noted.

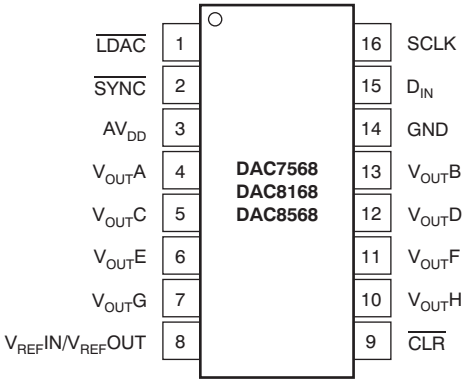
PARAMETER		TEST CONDITIONS	DAC7568/DAC8168/DAC8568 MIN	TYP	MAX	UNIT
POWER REQUIREMENTS						
AV_{DD}			2.7		5.5	V
I_{DD} (7)	Normal mode, including internal reference	AV_{DD} = IOV_{DD} = 3.6V to 5.5V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		1.2	1.6	mA
		AV_{DD} = IOV_{DD} = 2.7V to 3.6V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		1.1	1.5	
	All power-down modes	AV_{DD} = IOV_{DD} = 3.6V to 5.5V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		2	8	µA
		AV_{DD} = IOV_{DD} = 2.7V to 3.6V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		1	5	
Power Dissipation (7)	Normal mode, including internal reference	AV_{DD} = IOV_{DD} = 3.6V to 5.5V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		4	8.8	mW
		AV_{DD} = IOV_{DD} = 2.7V to 3.6V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		3	5.4	
	All power-down modes	AV_{DD} = IOV_{DD} = 3.6V to 5.5V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		7	44	µW
		AV_{DD} = IOV_{DD} = 2.7V to 3.6V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		1	18	
TEMPERATURE RANGE						
Specified performance			–40		+125	°C

(7) Input code = 2048, reference current included, no load.

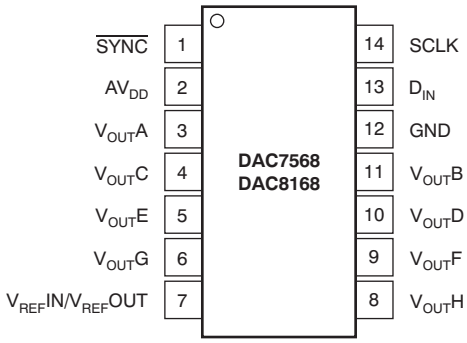
PRODUCT PREVIEW

PIN CONFIGURATIONS

**PW PACKAGE
TSSOP-16
(TOP VIEW)**



**PW PACKAGE
TSSOP-14
(TOP VIEW)**



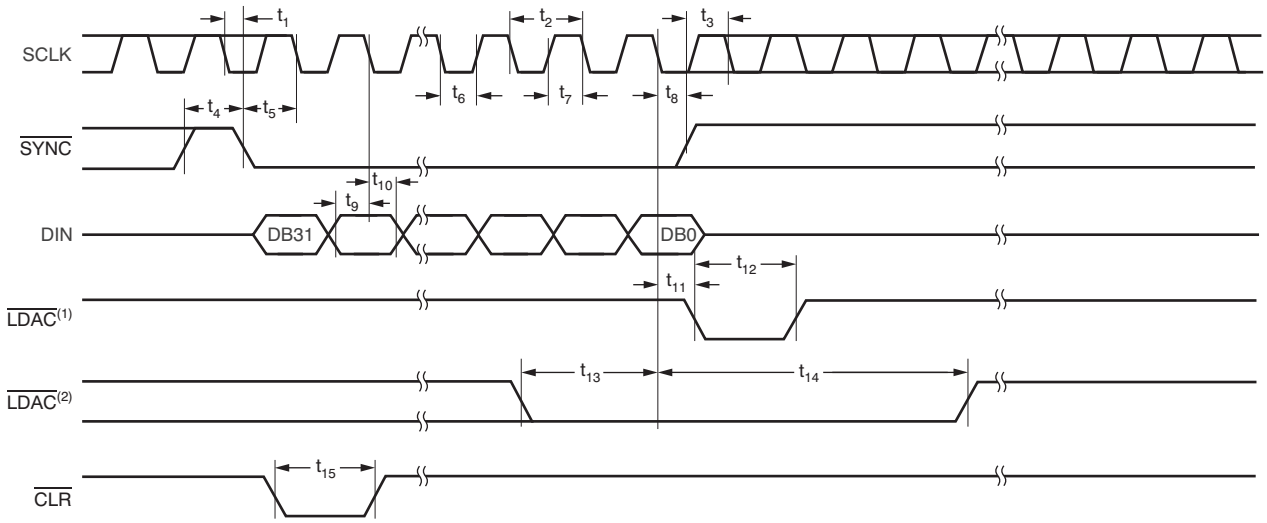
PIN DESCRIPTIONS

16-PIN	14-PIN	NAME	DESCRIPTION
1	—	$\overline{\text{LDAC}}$	Load DACs.
2	1	$\overline{\text{SYNC}}$	Level-triggered control input (active low). This input is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the input shift register, and data are sampled on subsequent falling clock edges. The DAC output updates following the 32nd clock. If $\overline{\text{SYNC}}$ is taken high before the 31st clock edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the DAC8568/DAC8168/DAC7568. Schmitt-Trigger logic input.
3	2	AV_{DD}	Power-supply input, 2.7V to 5.5V
4	3	$V_{OUT}A$	Analog output voltage from DAC A
5	4	$V_{OUT}C$	Analog output voltage from DAC C
6	5	$V_{OUT}E$	Analog output voltage from DAC E
7	6	$V_{OUT}G$	Analog output voltage from DAC G
8	7	$V_{REF}IN$/ $V_{REF}OUT$	Positive reference input / reference output 2.5V if internal reference used.(1)
9	—	$\overline{\text{CLR}}$	Asynchronous Clear Input.
10	8	$V_{OUT}H$	Analog output voltage from DAC H
11	9	$V_{OUT}F$	Analog output voltage from DAC F
12	10	$V_{OUT}D$	Analog output voltage from DAC D
13	11	$V_{OUT}B$	Analog output voltage from DAC B
14	12	GND	Ground reference point for all circuitry on the device
15	13	D_{IN}	Serial data input. Data are clocked into the 32-bit input shift register on each falling edge of the serial clock input. Schmitt-Trigger logic input.
16	14	SCLK	Serial clock input. Data can be transferred at rates up to 50MHz. Schmitt-Trigger logic input.

(1) Grades A and B, external $V_{REF}IN$ (max) = 5V; grades C and D, external $V_{REF}IN$ (max) = 2.5V

PRODUCT PREVIEW

SERIAL WRITE OPERATION



(1) Asynchronous LDAC update mode.

(2) Synchronous LDAC update mode.

TIMING REQUIREMENTS(1)(2)

At AV_{DD} = IOV_{DD}= 2.7V to 5.5V and –40°C to +105°C range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	DAC8568/DAC8168/DAC7568 MIN	TYP	MAX	UNIT
t_1	SCLK falling edge to $\overline{SYNC}$ falling edge (for successful write operation)	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	10			ns
t_2(3)	SCLK cycle time	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	20			ns
t_3	$\overline{SYNC}$ rising edge to 31st SCLK falling edge (for successful $\overline{SYNC}$ interrupt)	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	13			ns
t_4	Minimum $\overline{SYNC}$ HIGH time	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	80			ns
t_5	$\overline{SYNC}$ to SCLK falling edge setup time	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	13			ns
t_6	SCLK LOW time	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	8			ns
t_7	SCLK HIGH time	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	8			ns
t_8	SCLK falling edge to $\overline{SYNC}$ rising edge	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	7			ns
t_9	Data setup time	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	6			ns
t_{10}	Data hold time	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	4			ns
t_{11}	SCLK falling edge to $\overline{LDAC}$ falling edge (for successful write operation)	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	40			ns
t_{12}	$\overline{LDAC}$ pulse width LOW time	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	80			ns
t_{13}	$\overline{LDAC}$ falling edge to SCLK falling edge for synchronous LDAC update mode	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	4 × t_1			ns
t_{14}	32nd SCLK falling edge to $\overline{LDAC}$ rising edge	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	40			ns
t_{15}	$\overline{CLR}$ pulse width LOW time	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	80			ns

(1) All input signals are specified with t_R = t_F = 3ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
(2) See the *Serial Write Operation* timing diagram.
(3) Maximum SCLK frequency is 50MHz at IOV_{DD} = V_{DD} = 2.7V to 5.5V

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC7568IAPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC7568IAPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC7568ICPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC7568ICPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8168IAPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8168IAPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8168ICPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8168ICPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8568IAPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8568IAPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8568IBPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8568IBPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8568ICPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8568ICPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8568IDPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8568IDPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

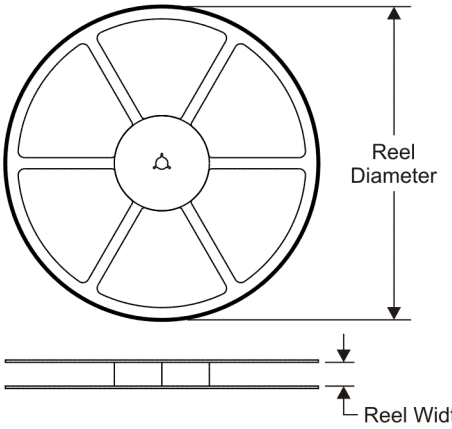
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

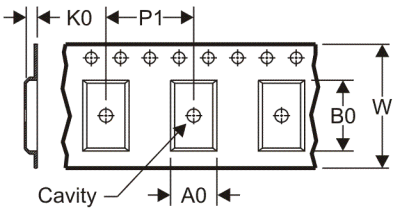
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

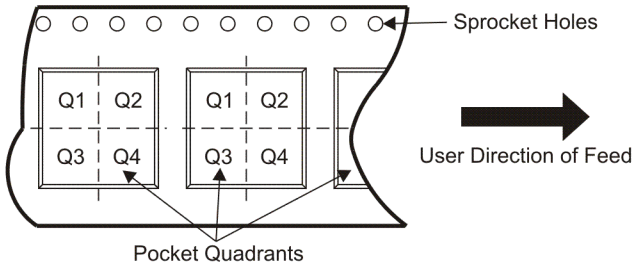


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

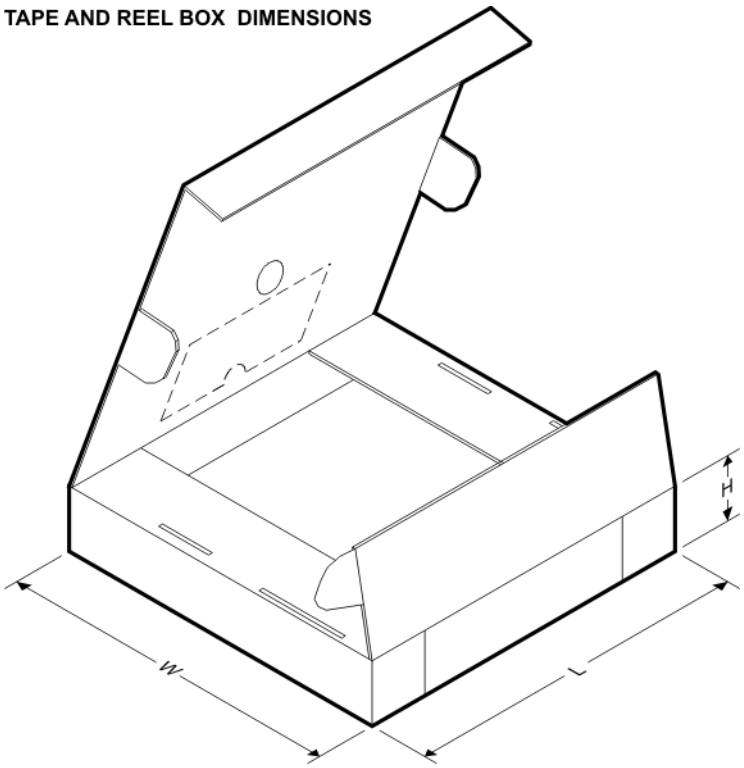
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8168ICPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

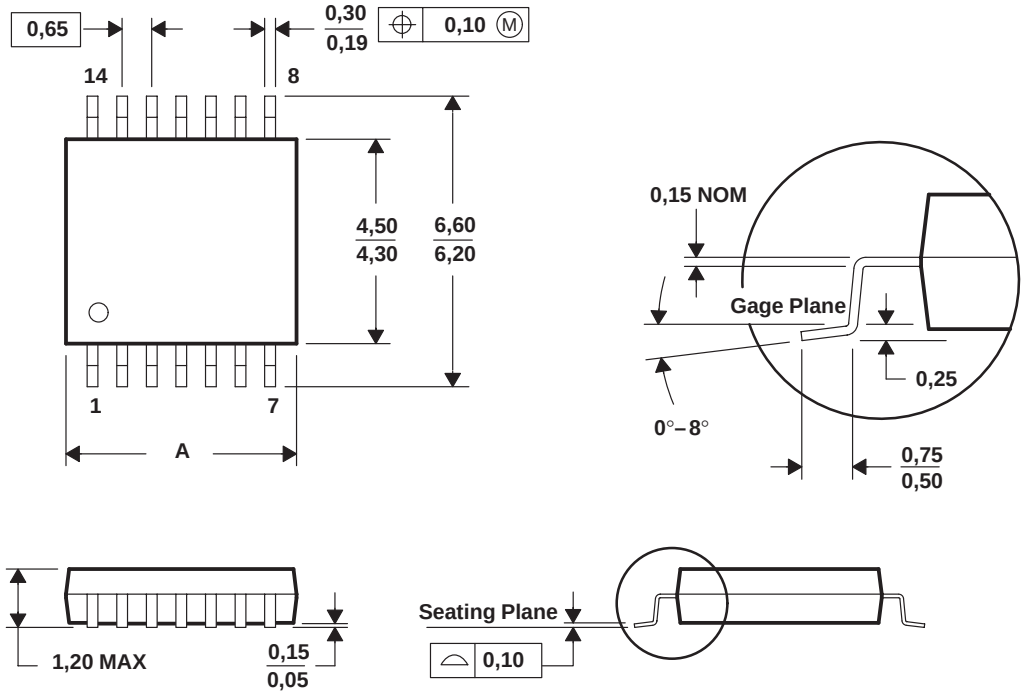


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8168ICPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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