

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74HC/HCT595

FEATURES

- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- 100 MHz (typ) shift out frequency
- Output capability:
 - parallel outputs; bus driver
 - serial output; standard
- I_{CC} category: MSI.

APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register.

DESCRIPTION

The 74HC/HCT595 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LS TTL). They are specified in compliance with JEDEC standard no. 7A.

The "595" is an 8-stage serial shift register with a storage register and 3-state outputs. The shift register and storage register have separate clocks.

Data is shifted on the positive-going transitions of the SH_{CP} input. The data in each register is transferred to the storage register on a positive-going transition of the ST_{CP} input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (D_S) and a serial standard output (Q_7') for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register

stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input (OE) is LOW.

QUICK REFERENCE DATA

$GND = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$.

SYMBOL	PARAMETER	CONDITIONS	TYP.		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q_7' ST_{CP} to Q_n $\overline{MR}$ to Q_7'	$C_L = 15\text{ pF}$ $V_{CC} = 5\text{ V}$	16	21	ns
			17	20	ns
			14	19	ns
f_{max}	maximum clock frequency SH_{CP} , ST_{CP}		100	57	MHz
C_i	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	115	130	pF

Notes

C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz C_L = output load capacitance in pF

f_o = output frequency in MHz V_{CC} = supply voltage in V

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

For HC the condition is $V_i = GND$ to V_{CC}

For HCT the condition is $V_i = GND$ to $V_{CC} - 1.5\text{ V}$.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT595N	16	DIL	plastic	SOT38Z
74HC/HCT595D	16	SO16	plastic	SOT109A

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PINNING

SYMBOL	PIN	DESCRIPTION
$Q_0 - Q_7$	15, 1 - 7	parallel data output
GND	8	ground (0 V)
Q_7'	9	serial data output
MR	10	master reset (active LOW)
SH_{CP}	11	shift register clock input
ST_{CP}	12	storage register clock input
$\overline{OE}$	13	output enable (active LOW)
D_S	14	serial data input
V_{CC}	16	positive supply voltage

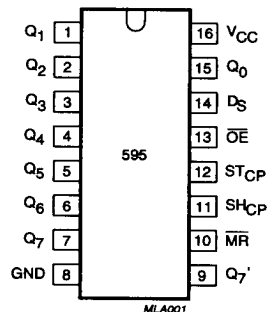


Fig.1 Pin configuration.

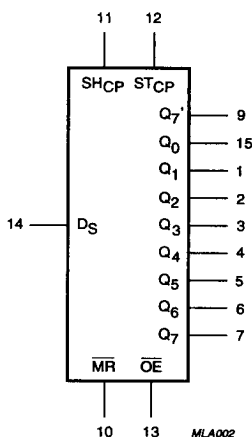


Fig.2 Logic symbol.

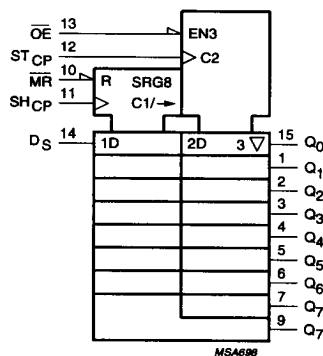


Fig.3 IEC logic symbol.

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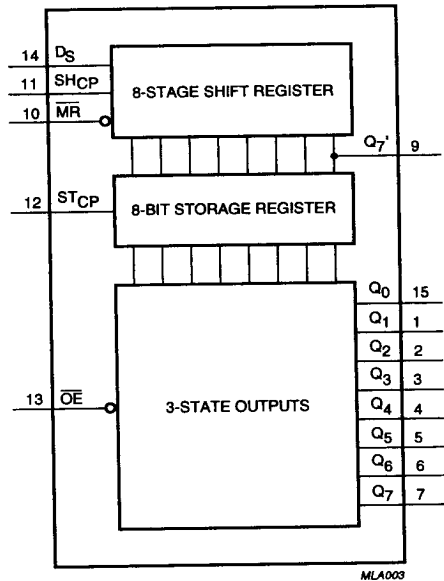


Fig.4 Functional diagram.

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

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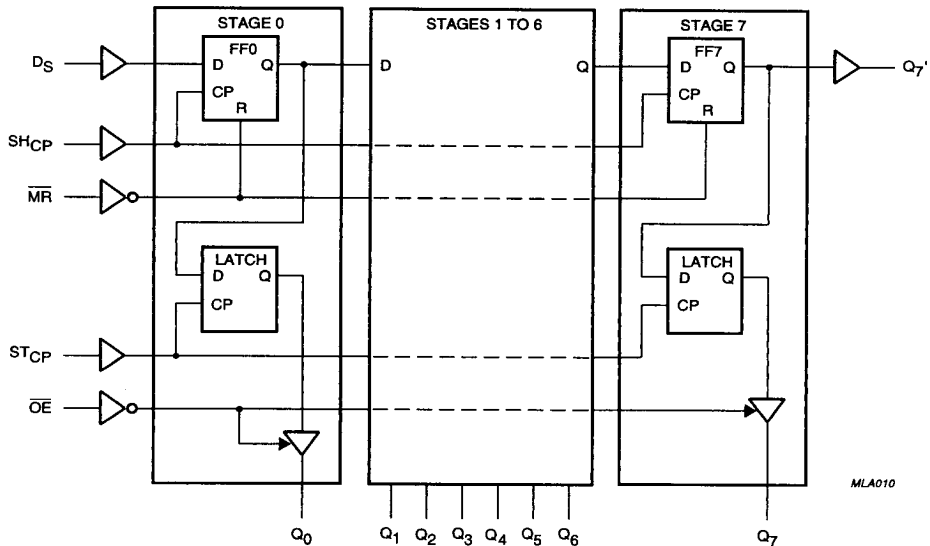


Fig.5 Logic diagram.

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FUNCTION TABLE

INPUTS					OUPUTS		FUNCTION
SH _{CP}	ST _{CP}	$\overline{OE}$	$\overline{MR}$	D _s	Q ₇ '	Q _n	
X	X	L	↓	X	L	NC	a LOW level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear. Parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q ₆ '	NC	logic high level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q ₆ ') appears on the serial output (Q ₇ ')
X	↑	L	H	X	NC	Q _n '	contents of shift register stages (internal Q _n ') are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q ₆ '	Q _n '	contents of shift register shifted through. Previous contents of the shift register is transferred to the storage register and the parallel output stages.

H = HIGH voltage level

L = LOW voltage level

↑ = LOW-to-HIGH transition

↓ = HIGH-to-LOW transition

Z = high-impedance OFF-state

NC = no change

X = don't care.

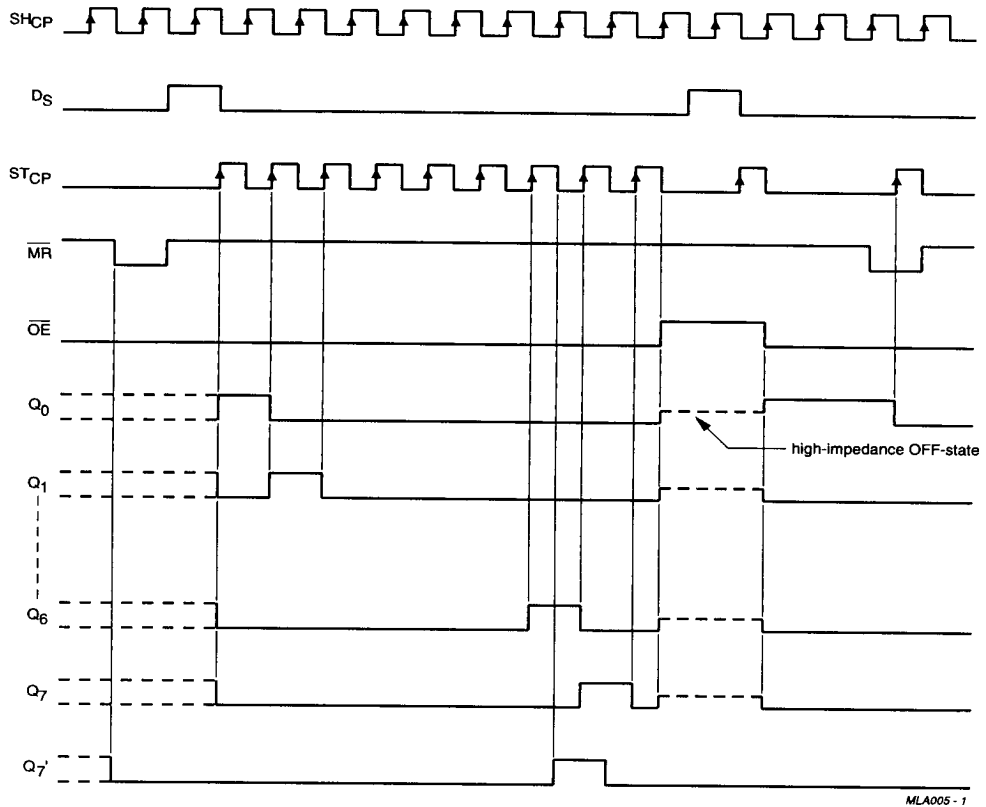
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Fig.6 Timing diagram.

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: parallel outputs, bus driver; serial output, standard I_{CC} category: MSI.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITION	
		+25			-40 to +85		-40 to +125			V _{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t _{PHL} /t _{PLH}	propagation delay SH _{CP} to Q ₇ '	—	52	160	—	200	—	240	ns	2.0	Fig.7
		—	19	32	—	40	—	48	ns	4.5	
		—	15	27	—	34	—	41	ns	6.0	
t _{PHL} /t _{PLH}	propagation delay ST _{CP} to Q _n	—	55	175	—	220	—	265	ns	2.0	Fig.8
		—	20	35	—	44	—	53	ns	4.5	
		—	16	30	—	37	—	45	ns	6.0	
t _{PHL}	propagation delay MR to Q ₇ '	—	47	175	—	220	—	265	ns	2.0	Fig.10
		—	17	35	—	44	—	53	ns	4.5	
		—	14	30	—	37	—	45	ns	6.0	
t _{PZH} /t _{PZL}	3-state output enable time OE to Q _n	—	47	150	—	190	—	225	ns	2.0	Fig.11
		—	17	30	—	38	—	45	ns	4.5	
		—	14	26	—	33	—	38	ns	6.0	
t _{PHZ} /t _{PLZ}	3-state output disable time OE to Q _n	—	41	150	—	190	—	225	ns	2.0	Fig.11
		—	15	30	—	38	—	45	ns	4.5	
		—	12	26	—	33	—	38	ns	6.0	
t _W	shift clock pulse width HIGH or LOW	75	17	—	95	—	110	—	ns	2.0	Fig.7
		15	6	—	19	—	22	—	ns	4.5	
		13	5	—	16	—	19	—	ns	6.0	
t _W	storage clock pulse width HIGH or LOW	75	11	—	95	—	110	—	ns	2.0	Fig.8
		15	4	—	19	—	22	—	ns	4.5	
		13	3	—	16	—	19	—	ns	6.0	
t _W	master reset pulse width LOW	75	17	—	95	—	110	—	ns	2.0	Fig.10
		15	6.0	—	19	—	22	—	ns	4.5	
		13	5.0	—	16	—	19	—	ns	6.0	
t _{su}	set-up time D _s to SH _{CP}	50	11	—	65	—	75	—	ns	2.0	Fig.9
		10	4.0	—	13	—	15	—	ns	4.5	
		9.0	3.0	—	11	—	13	—	ns	6.0	
t _{su}	set-up time SH _{CP} to ST _{CP}	75	22	—	95	—	110	—	ns	2.0	Fig.8
		15	8	—	19	—	22	—	ns	4.5	
		13	7	—	16	—	19	—	ns	6.0	
t _h	hold time D _s to SH _{CP}	3	-6	—	3	—	3	—	ns	2.0	Fig.9
		3	-2	—	3	—	3	—	ns	4.5	
		3	-2	—	3	—	3	—	ns	6.0	
t _{rem}	removal time MR to SH _{CP}	50	-19	—	65	—	75	—	ns	2.0	Fig.10
		10	-7	—	13	—	15	—	ns	4.5	
		9	-6	—	11	—	13	—	ns	6.0	

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SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V _{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
f _{max}	maximum clock pulse frequency SH _{CP} or ST _{CP}	6	30	—	4.8	—	4	—	MHz	2.0	Figs 7 and 8
		30	91	—	24	—	20	—	MHz	4.5	
		35	108	—	28	—	24	—	MHz	6.0	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: parallel outputs, bus driver; serial output, standard

I_{CC} category: MSI.

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

INPUT	UNIT LOAD COEFFICIENT
D_S	0.25
$\overline{MR}$	1.50
SH_{CP}	1.50
ST_{CP}	1.50
$\overline{OE}$	1.50

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AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V _{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t _{PHL} /t _{PLH}	propagation delay SH _{CP} to Q ₇ '	−	25	42	−	53	−	63	ns	4.5	Fig.7
t _{PHL} /t _{PLH}	propagation delay ST _{CP} to Q _n	−	24	40	−	50	−	60	ns	4.5	Fig.8
t _{PHL}	propagation delay MR to Q ₇ '	−	23	40	−	50	−	60	ns	4.5	Fig.10
t _{PZH} / t _{PZL}	3-state output enable time OE to Q _n	−	21	35	−	44	−	53	ns	4.5	Fig.11
t _{PHZ} /t _{PLZ}	3-state output disable time OE to Q _n	−	18	30	−	38	−	45	ns	4.5	Fig.11
t _W	shift clock pulse width HIGH or LOW	16	6	−	20	−	24	−	ns	4.5	Fig.7
t _W	storage clock pulse width HIGH or LOW	16	5	−	20	−	24	−	ns	4.5	Fig.8
t _W	master reset pulse width LOW	20	8	−	25	−	30	−	ns	4.5	Fig.10
t _{su}	set-up time D _s to SH _{CP}	16	5	−	20	−	24	−	ns	4.5	Fig.9
t _{su}	set-up time SH _{CP} to ST _{CP}	16	8	−	20	−	24	−	ns	4.5	Fig.8
t _h	hold time D _s to SH _{CP}	3	−2	−	3	−	3	−	ns	4.5	Fig.9
t _{rem}	removal time MR to SH _{CP}	10	−7	−	13	−	15	−	ns	4.5	Fig.10
f _{max}	maximum clock pulse frequency SH _{CP} or ST _{CP}	30	52	−	24	−	20	−	MHz	4.5	Figs 7 and 8

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AC WAVEFORMS

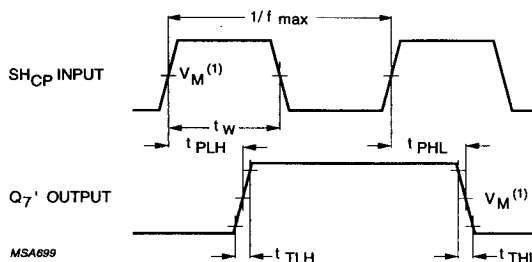


Fig.7 Waveforms showing the clock (SH_{CP}) to output (Q_7') propagation delays, the shift clock pulse width and maximum shift clock frequency.

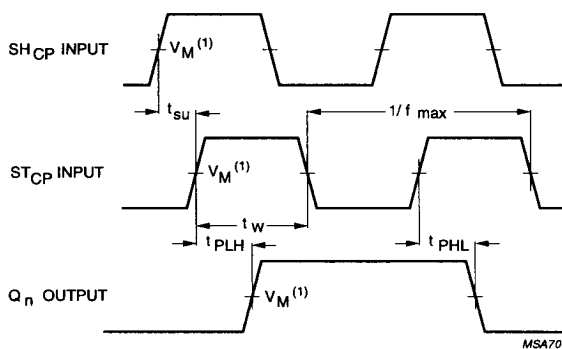


Fig.8 Waveforms showing the storage clock (ST_{CP}) to output (Q_n) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time.

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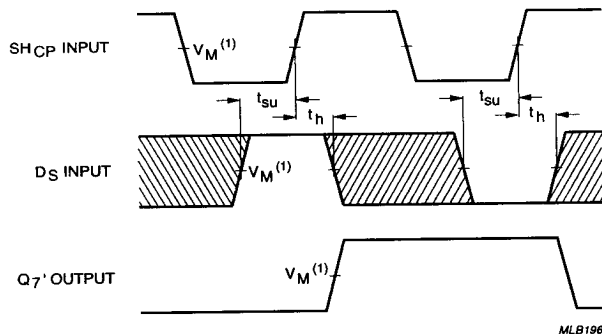


Fig.9 Waveforms showing the data set-up and hold times for the D_S input.

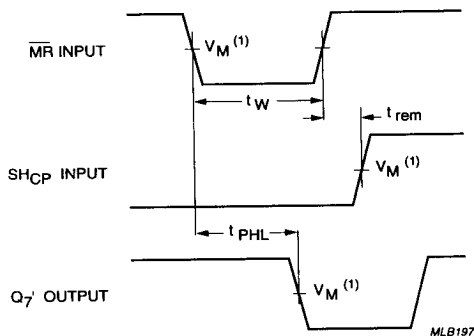


Fig.10 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q₇') propagation delay and the master reset to shift clock (SH_{CP}) removal time.

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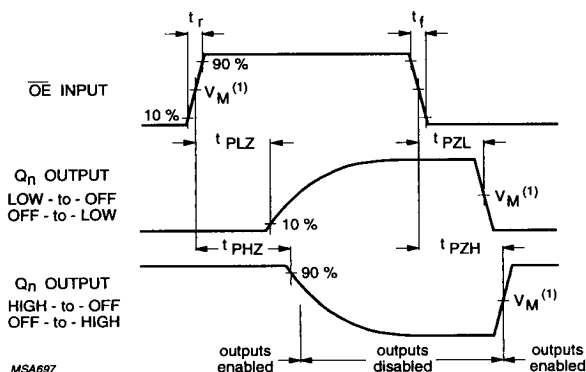


Fig.11 Waveforms showing the 3-state enable and disable times for input $\overline{OE}$.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$
 HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.