TPS40051-Based Design Converts 12-V Bus to 1.8 V at 15 A (SLUP195)

User's Guide

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TPS40051-Based Design Converts 12-V Bus to 1.8 V at 15 A (SLUP195)

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Contents

1 Introduction

In many modern electronic applications there is a growing demand for circuits to convert a12-V bus to digital voltages as low as, but not limited to 1.8 V. The current requirements can range from below 1 A to over 15 A. For high-efficiency and small circuit size the TPS40051 wide-input synchronous buck controller can be used to provide the necessary control and drive functions to implement these converters. The TPS40051EVM–001 operates at 300 kHz and delivers 1.8 V at 15 A with efficiency over 90% for much of the load range, and a full load efficiency of 88%.

The TPS40051 synchronous buck controller offers a variety of user programmable functions such as operating frequency, soft-start time, voltage feed-forward, high-side current limit, and external loop compensation. This controller also provides a regulated 10-V bias voltage which supplies onboard drivers for the N-channel switch and synchronous rectifier MOSFETs, utilizing adaptive gate drive logic to prevent cross conduction of the power MOSFETs.[1]

2 Features

The specification of this design is as follows:

- 92% peak efficiency at 6 A
- 88% peak efficiency at 15 A
- 1.8V output at 15 A
- V_{IN} range from 10 V_{DC} to 14 V_{DC}
- Small circuit size 1.4” x 2.5” SMT design, components on single side
- Line/load regulation < 0.5%
- High-frequency 300-kHz operation
- Transient deviation 60 mV with 10-A load step

3 Schematic

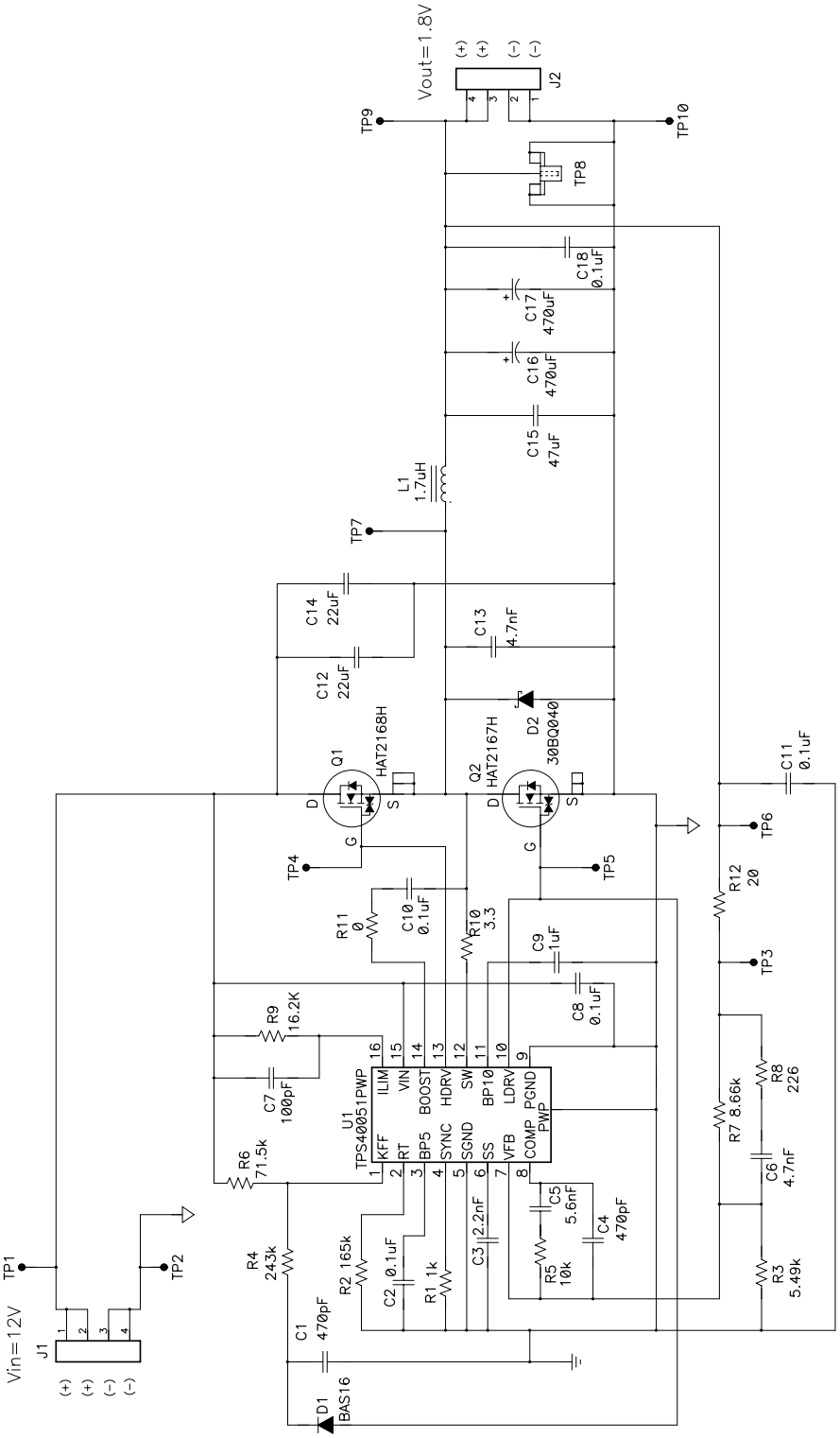


Figure 1. TPS40051EVM–001 (SLUP195) Schematic

4 Component Selection

4.1 TPS40051 Device Selection

The TPS4005x family of parts offers a range of output current configurations including source only (TPS40050), source/sink (TPS40051), or source/sink with V_{OUT} prebias (TPS40053). In this converter the TPS40051 with source/sink capability is selected. This serves to maintain continuous inductor ripple current all the way to zero load to improve the small signal loop response by preventing the inductor current from transitioning to the discontinuous current mode.

The TPS4005x family is packaged in TI's PWP PowerPAD thermally enhanced package which should be soldered to the PCB using standard solder flow techniques. The PowerPAD™ technology uses a thermally conductive epoxy to attach the integrated circuit die to the leadframe die pad, which is exposed on the bottom of the completed package. The PWP PowerPAD package has a θ_{JC} = 2°C/W which helps keep the junction temperature rise relatively low even with the power dissipation inherent in the onboard MOSFET drivers. This power loss is proportional to switching frequency, drive voltage, and the gate charge needed to enhance the N-channel MOSFETs. Effective heat removal allows the use of ultra-small packaging while maintaining high component reliability.

The technical brief, PowerPAD Thermally Enhanced Package[2] contains more information on the PowerPAD package.

4.2 Frequency of Operation

The clock oscillator frequency for the TPS40051 is programmed with a single resistor from RT (pin 2) to signal ground. The following equation (1) from the datasheet allows selection of RT in kΩ for a given switching frequency in kHz.

$$R_T = R2 = \frac{1}{f_{SW} \times 17.82 \times 10^{-6}} - 23\ (k\Omega) \quad (1)$$

For 300-kHz operation, R2 is selected to be 165 kΩ.

For a particular operating frequency, the PWM ramp time must be programmed via the resistor R_{KFF} connected to V_{IN}. Also, the selection of R_{KFF} programs the V_{IN} voltage at which the circuit starts operation. This prevents the circuit from starting at low voltages, which can lead to current flow larger than desired. R_{KFF} is programmed using equation (2).

$$R_{KFF} = R6 = \left(V_{IN(min)} - 3.5\right) \times \left(58.14 \times R_T + 1340\right)\ (k\Omega) \quad (2)$$

Where $V_{IN(min)}$ is the minimum startup input voltage, and R_T is in kΩ. Note that internal tolerances have been incorporated into this equation, so the actual $V_{IN(min)}$ of the input voltage should be used. For an oscillator frequency of 300-kHz, the R_{KFF} value of 71.5 kΩ is selected.

4.3 UVLO Circuitry

The user programmable UVLO built into the TPS4005x provides hysteresis for transients shorter than a total count of seven cycles. If the input voltage to the converter can be slowly rising around the minimum V_{IN} range, external hysteresis can be incorporated to prevent multiple on/off cycles during startup or shutdown. These on/off cycles are a result of line impedance external to the EVM causing V_{IN} to the module to drop when under load, which causes the programmable UVLO threshold to be crossed repetitively.

In this converter, C1 and D1 are added to form a peak detector from the lower gate drive which is only active when the converter is operating. This provides a bias source to deliver hysteresis current from the peak detector voltage to the lower KFF voltage of 3.5 V, enabling the designer to alter the programmable UVLO shutdown point. The bias is not present during startup, so the circuit starts as expected from the R_{KFF} calculation.

In this application, R4 is selected to provide a hysteresis current of 20% I_{KFF}. R4 can be calculated from equation (3).

$$R_{HYS} = R4 = \frac{R_{KFF} \times \left(V_{PD} - 3.5\right)}{0.2 \times \left(V_{IN(min)} - 3.5\right)} \tag{3}$$

where

- V_{PD} is the voltage on the peak detector
- $V_{IN(min)}$ is the desired start voltage used in the determination of R_{KFF}

In a typical case, V_{PD} = 8V, and R4 is found to be 247 kΩ, and a standard value of 243kΩ is selected. Testing shows the startup voltage to be 9.2 V, and the shutdown voltage to be 8.5 V.

4.4 Inductance Value

The output inductor L1 value used in the circuit of Figure 2 was selected from equation (4).

$$L = \frac{V_{OUT}}{f \times I_{RIPPLE}} \times 1 - \frac{V_{OUT}}{V_{IN(min)}} \tag{4}$$

in which I_{RIPPLE} is usually chosen to be in the range between 10% and 40% of I_{OUT}. With I_{RIPPLE} = 20% of $I_{OUT(max)}$ there is a ripple current of 3 A, and the inductance value is 1.7 μH.

4.5 Input capacitor selection

Bulk input capacitor selection is based on allowable input voltage ripple and required RMS current carrying capability. In typical buck converter applications, the converter is fed from an upstream power converter with its own output capacitance. In this converter, ceramic capacitors capable of meeting circuit requirements are provided onboard. For this power level, input voltage ripple of approximately 250 mV is reasonable, and the minimum capacitance is calculated in (5).

$$C_{IN} = \frac{I \times \Delta t}{\Delta V} = \frac{I \times V_O}{\Delta V \times V_{IN} \times f_S} = \frac{15\ A \times 1.8\ V}{0.25\ V \times 10\ V \times 300\ kHz} = 36\ \mu F \tag{5}$$

Also consider the RMS current rating required for the input capacitors (6).

$$i \cong I_{OUT} \times \sqrt{D} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}}} = 15 \times \sqrt{\frac{1.8}{10}} = 6.4\ A \tag{6}$$

To meet this requirement with the smallest cost and size two 22 μF, 16 V, X5R ceramic capacitors (C12, C14) are installed on the board. In the 1812 case, the parts are able to carry approximately 4 A_{RMS} each. These capacitors function as power bypass components and should be located close to the MOSFET packages to keep the high-frequency current flow in a small, tight loop.

4.6 Output Capacitor Selection

Selection of the output capacitor is based on many application variables, including function, cost, size, and availability. The minimum allowable output capacitance is determined by the amount of inductor ripple current and the allowable output ripple, as given in equation (7).

$$C_{OUT(min)} = \frac{I_{RIPPLE}}{8 \times f \times V_{RIPPLE}} = \frac{3\ A}{8 \times 300\ kHz \times 15\ mV} = 83\ \mu F \quad (7)$$

In this design, $C_{OUT(min)}$ is 83 μF with V_{RIPPLE}=15 mV to allow for some margin. However, this only affects the capacitive component of the ripple voltage, and the final value of capacitance is generally influenced by ESR and transient considerations. The voltage component due to the capacitor ESR.

$$C_{ESR} \leq \frac{V_{RIPPLE}}{I_{RIPPLE}} = \frac{15\ mA}{3\ A} = 5\ \mu\Omega \quad (8)$$

An additional consideration in the selection of the output inductor and capacitance value can be derived from examining the transient voltage overshoot which can be initiated with a load step from full load to no load. By equating the inductive energy with the capacitive energy the equation (9) can be derived:

$$C_O \leq \frac{L \times I^2}{V^2} = \frac{L \times \left(\left(I_{OH}\right)^2 - \left(I_{OL}\right)^2 \right)}{\left(V_f\right)^2 - \left(V_i\right)^2} = \frac{1.7\ \mu H \times (15\ A)}{\left((1.9\ V)^2 - (1.8\ V)^2\right)} = 1034\ \mu F \quad (9)$$

where

- I_{OH} = full load current
- I_{OL} = no load current
- V_f = allowed transient voltage rise
- V_i = initial voltage

For compactness while maintaining transient response capability, two 470-μF POSCAP capacitors (C16, C17) are fitted in parallel. The total ESR of these capacitors is approximately 5 mΩ. An additional 47-μF, 6.3-V ceramic capacitor C15 is placed in parallel with the POSCAPs to help suppress high frequency noise generated by the fast current transitions as the current switches between the input and output circuits during each switching cycle.

4.7 MOSFET selection

Proper MOSFET selection is essential to optimize circuit efficiency. To operate with high current it is important to choose a package which allows the generated heat to be removed from the package as easily as possible. Various MOSFETs with a package similar to the SO–8 footprint are considered for this application, and devices with reduced junction-case thermal impedance are selected.

For the upper switch Q1, a Hitachi HAT2168H MOSFET with low gate charge (typically 27 nC at 10 V) and with an $R_{DS(on)}$ of 6 mΩ is selected to keep the switching losses to a minimum. The low-side rectifier switch Q2 was chosen as a Hitachi HAT2167H, which has slightly more gate charge (43 nC at 10 V) but lower $R_{DS(on)}$ = 4.2 mΩ to minimize conduction losses. A schottky diode, D2, is placed across Q2 in this high current design to carry some of the high circulating current during short circuit conditions.

4.8 Short Circuit Protection

The TPS40051 implements short circuit protection by comparing the voltage across the topside MOSFET while it is ON to a voltage developed across R_{LIM} due to an internal current source of 10 μA inside pin 16. Both of these voltages are negative with respect to V_{IN}. From the datasheet equation, R_{LIM} is defined as:

$$R_{LIM} = R9 = \frac{I_{OC} \times R_{DS(on)\ (max)}}{1.12 \times I_{SINK}} = \frac{V_{OS}}{I_{SINK}} = (\Omega) \tag{10}$$

where

- I_{OC} is the overcurrent set point equal to the DC output current plus one-half the inductor ripple current
- V_{OS} is the overcurrent comparator offset, and Isink is the current into ILIM (pin 16).

Using worst case tolerances the value of R_{LIM} should be maximized to ensure that the converter can deliver full rated current under all conditions. In a worst case condition, R_{LIM}=R9 and

$$R_{LIM} = \frac{(15\ A + 1.5\ A) \times (7.9\ m\Omega \times 1.45)}{1.12 \times 8.65\ \mu A} + \frac{-\ 30\ mV}{8.65\ \mu A} = 16.0\ k\Omega \tag{11}$$

The standard value of 16.2 kΩ was selected. This ensures that we can deliver a minimum of 15 A before current limit is activated. There is also a small capacitor, C7, placed in parallel with R9 to filter the signal.

4.9 Snubber Component Selection

Initially, the junction of Q1, Q2, and L1 was ringing at a frequency near 100 MHz with a peak voltage near 30 V. This was due to the extremely fast switching speed of the MOSFETs and the lack of any cross–conduction. C13 was added to shunt the high-frequency ringing to ground and the peak voltage is now below 25 V.

4.10 Compensation Components

The TPS40051 uses voltage mode control with feed-forward in conjunction with a high-frequency error amplifier to implement closed loop control. The power circuit L-C double pole corner frequency f_C occurs at 3.8 kHz, and the output capacitor ESR zero is located at approximately 38 kHz. The feedback compensation network is implemented to provide two zeroes and three poles. The first pole is placed at the origin to improve DC regulation.

The first zero is placed at 2.8 kHz, just below the L-C corner frequency.

$$f_{Z1} = \frac{1}{2\pi \times R5 \times C5} \tag{12}$$

The second zero is selected to be coincident with the L-C corner frequency of 3.8 kHz,

$$f_{Z2} = \frac{1}{2\pi \times (R7 + R8) \times C6} \tag{13}$$

The second pole is placed near the ESR zero frequency at 37 kHz.

$$f_{P1} = \frac{1}{2\pi \times R5 \times \left(\frac{C4 \times C5}{C4 + C5}\right)} \tag{14}$$

and the third pole is placed at 150 kHz, which is one-half the switching frequency.

$$f_{P2} = \frac{1}{2\pi \times R8 \times C6} \tag{15}$$

5 Test Setup

Figure 2 illustrates the basic test setup needed to evaluate the TPS40051EVM–001.

5.1 DC Input Source

The input voltage source should be capable of supplying between 10 V_{DC} and 14 V_{DC} and rated for at least 4 A of current. For best results the input leads should be made with a wire of 18AWG or larger.

5.2 Output Load

The output load can be either an electronic load or a resistive load configured to draw between 0 A and 15 A. The output leads should be made with a wire of 16AWG or larger diameter wire. Monitor the output voltage on the PCB by connecting a voltmeter to TP9 and TP10 to prevent voltage drops through PCB traces and the output terminal block which can lead to substantial measurement errors.

5.3 Oscilloscope Probe Test Jacks

An oscilloscope probe test jack (TP8) has been included to allow monitoring the ourput voltage ripple.

5.4 Fan

There is no cover to prevent the user from probing the internal circuit nodes. There are components that can get hot to the touch (above 60°C) in normal operation. A small fan delivering more than 15 cfm should be used when operating at and near full load.

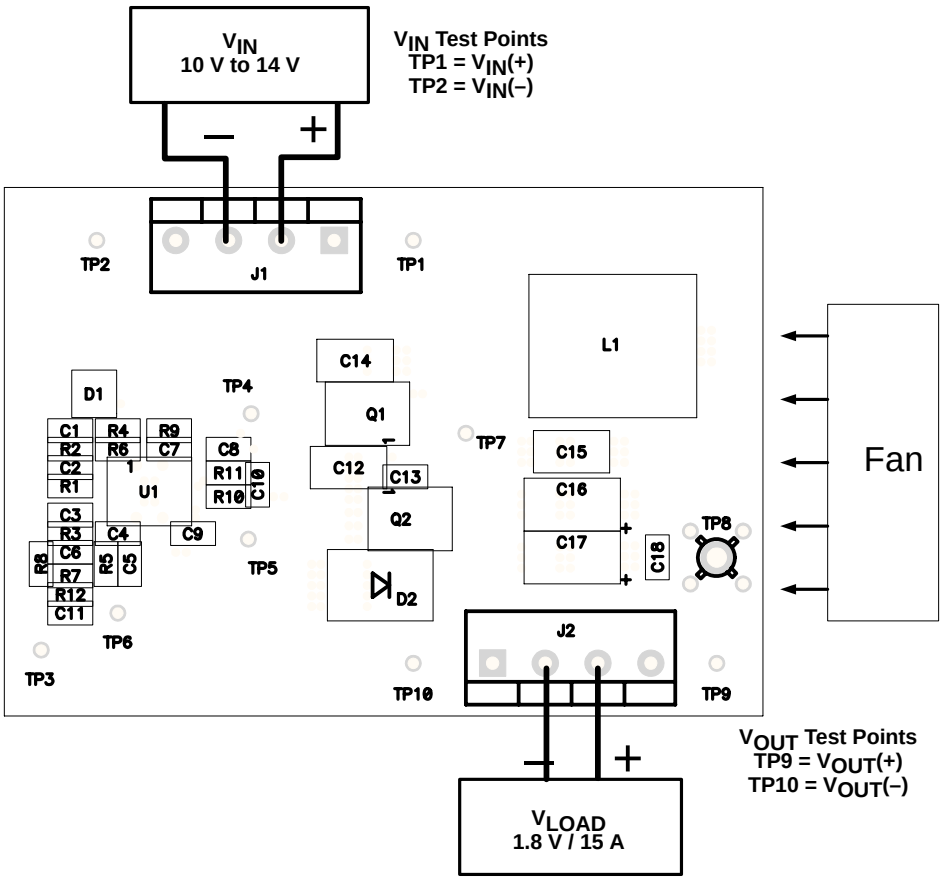


Figure 2. Test Setup

6 Test Results / Performance Data

6.1 Efficiency and Power Loss

Figure 3 shows the efficiency as the load is varied from 1 A to over 15 A. The typical efficiency remains over 90% as the load ranges from 3 A to 12 A.

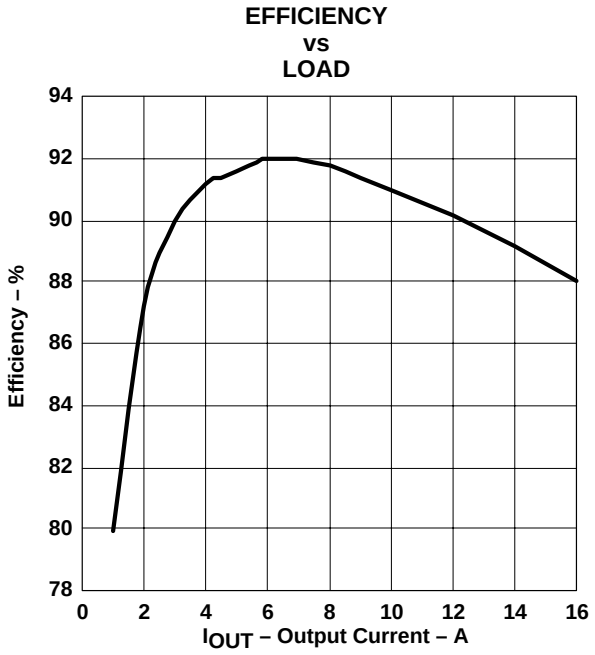


Figure 3

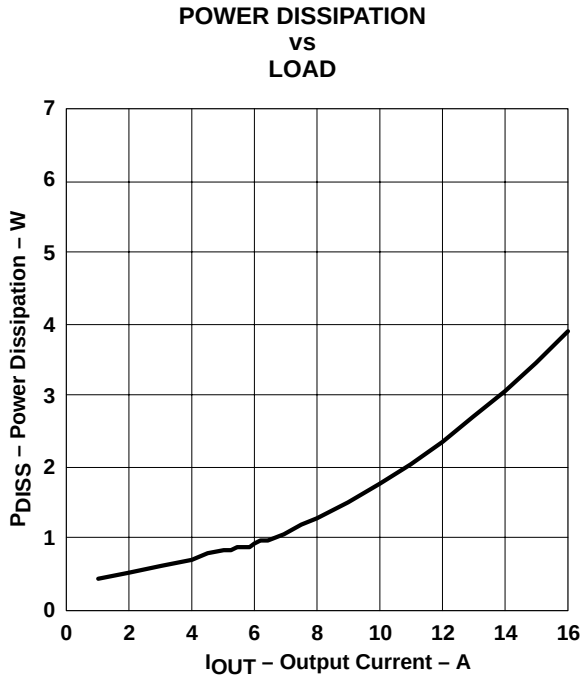


Figure 4

6.2 Closed Loop Performance

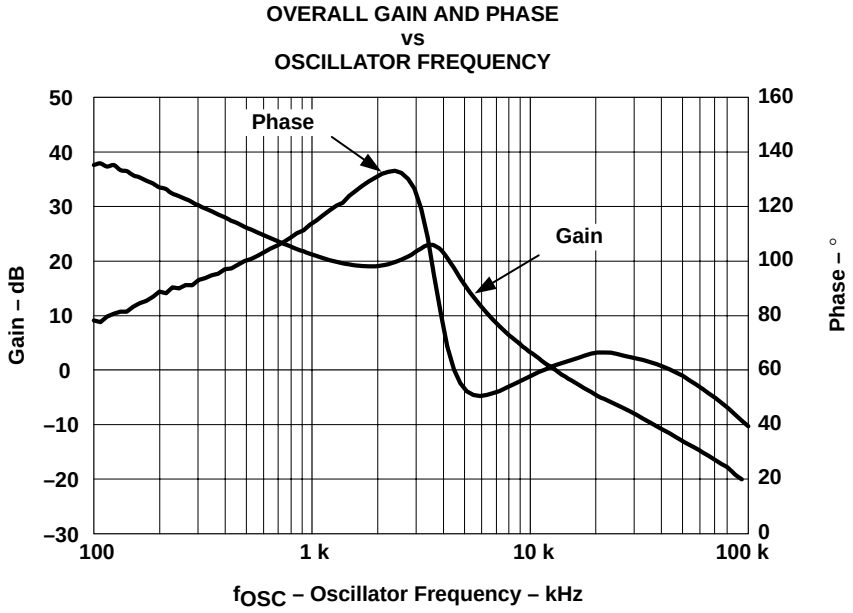


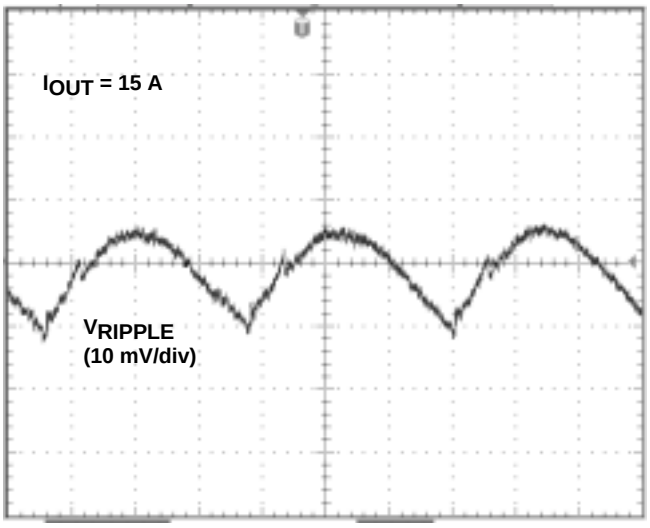
Figure 5.

6.3 Output Ripple and Transient Response

Figure 6 shows the typical output voltage ripple with I_{OUT}=15 A to be less than 20 mVpp.

The transient response is shown in Figure 7 as the load is stepped from 5 A to 15 A. The voltage deviation is less than 60 mV.

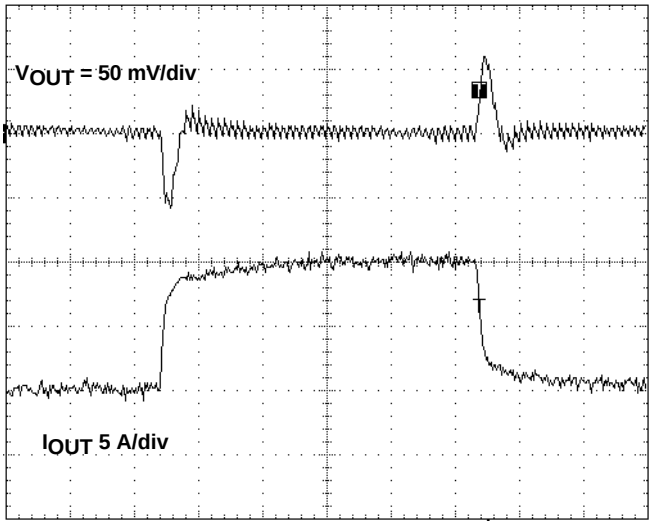
OUTPUT VOLTAGE RIPPLE



t – Time – 1 μs/div

Figure 6

TRANSIENT RESPONSE



t – Time – 200 μs/div

Figure 7

7 EVM Assembly Drawing and PCB Layout

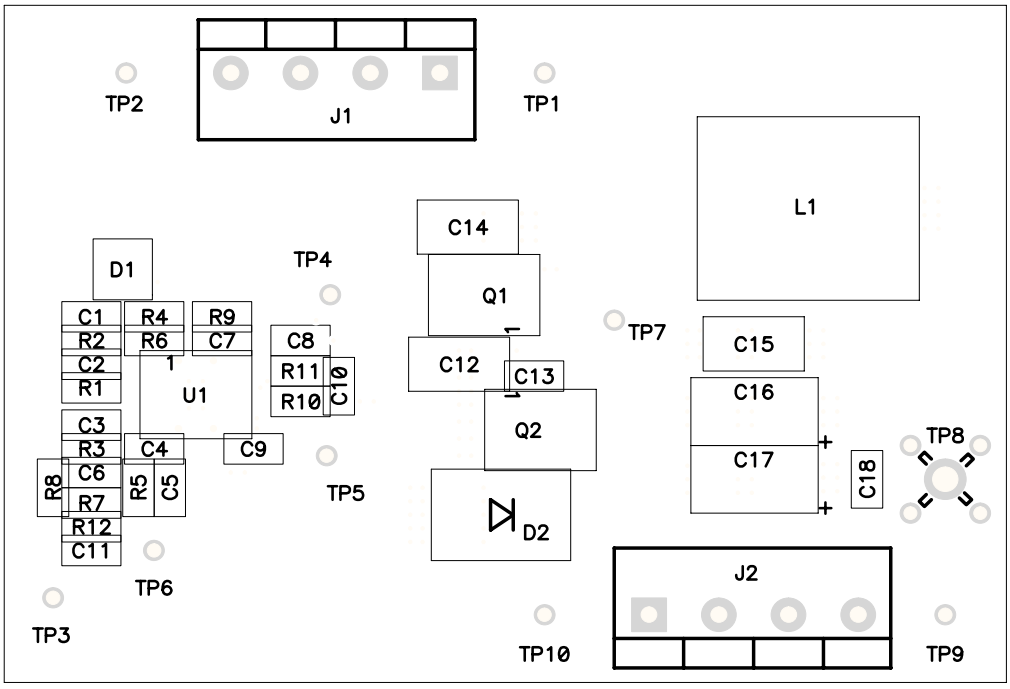


Figure 8. Top Side Component Assembly

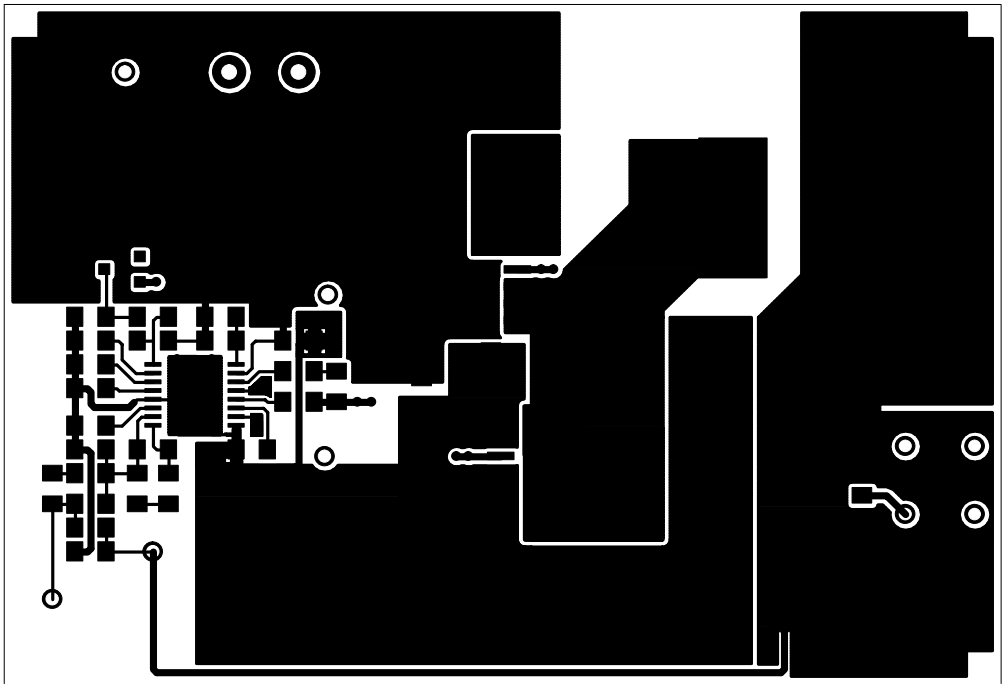


Figure 9. Top Side Copper

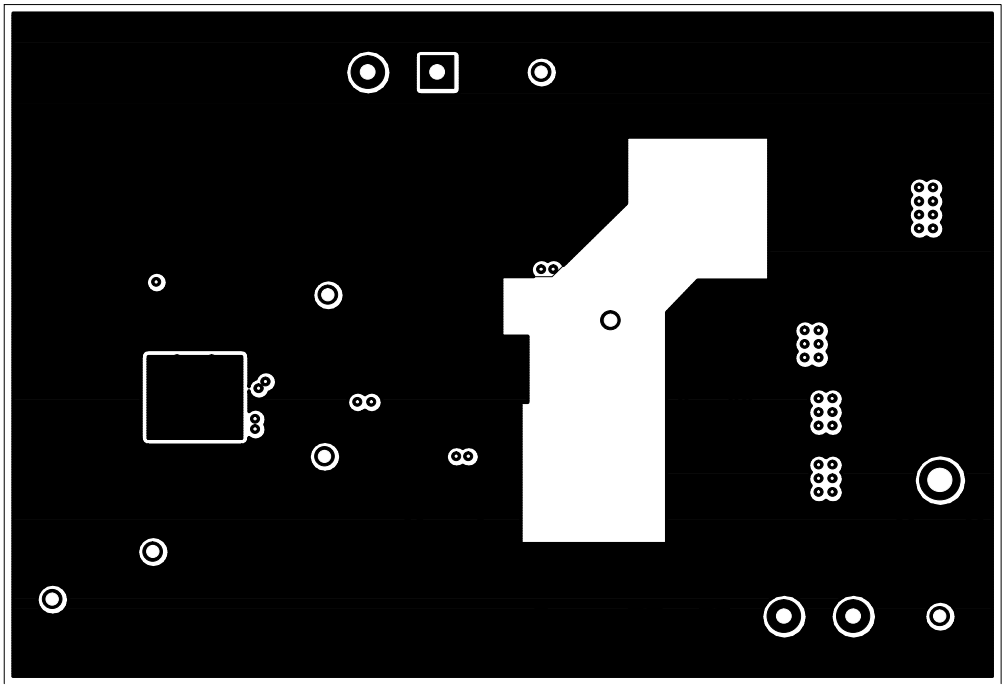


Figure 10. Internal Layer 1 Copper

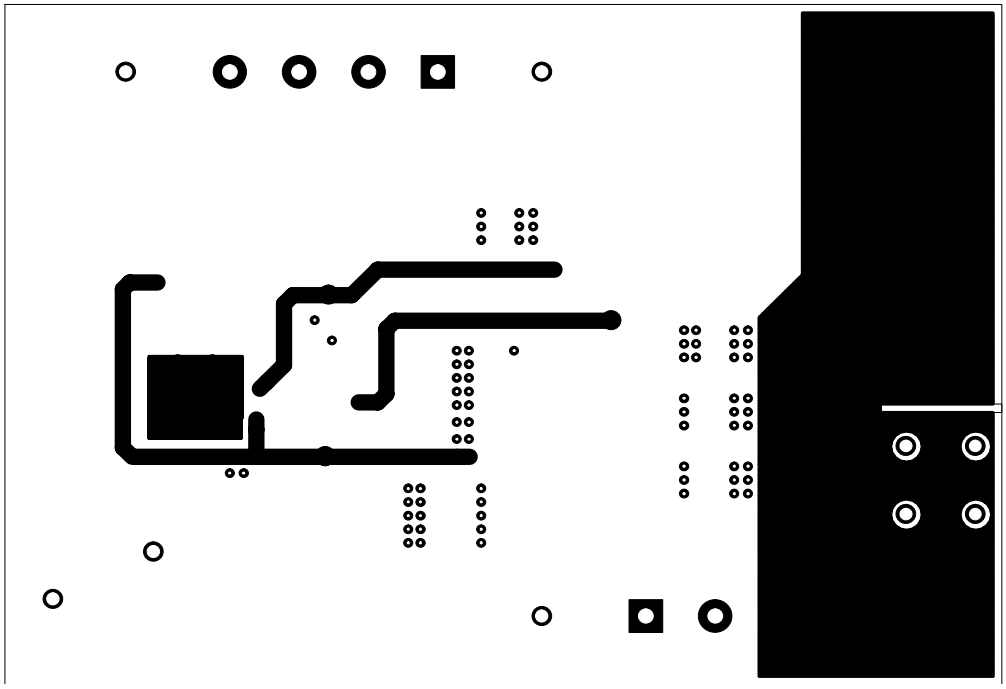


Figure 11. Internal Layer 2 Copper

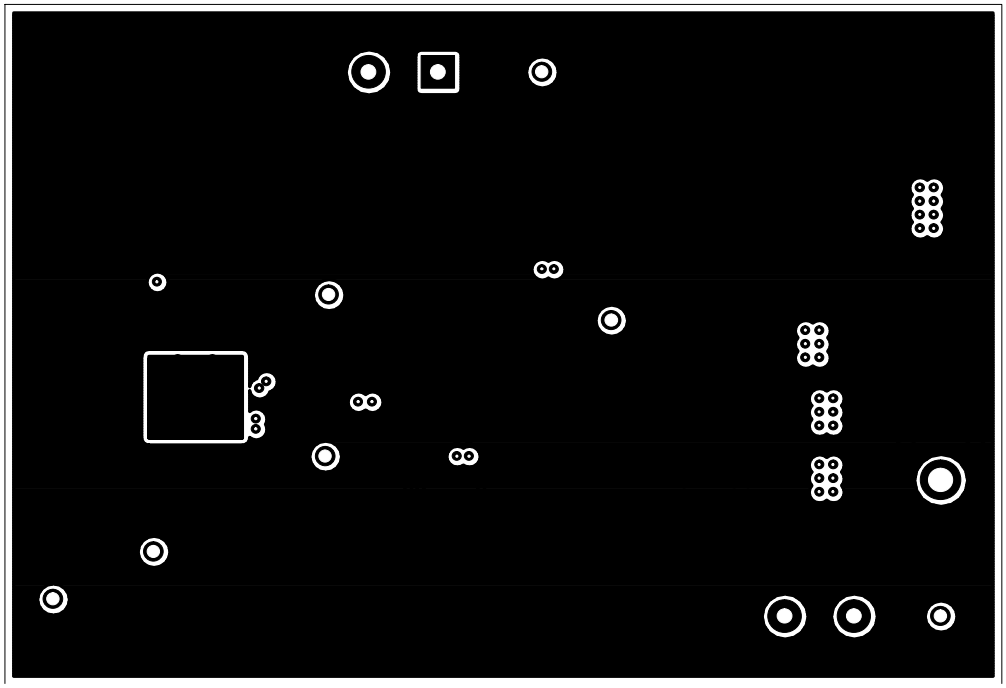


Figure 12. Bottom Layer Copper

8 List of Materials

Table 1 lists the parts values of the evaluation board. These values can be modified to meet the application requirements.

Table 1. TPS40051EVM–001 (SLUP195) List of Materials

REFERENCE DESIGNATOR	QTY	DESCRIPTION	SIZE	MFR	PART NUMBER
C1, C4	2	Capacitor, ceramic, 470 pF, 50 V, X7R, 10%	805	Vishay	VJ0805Y471KXAAT
C12, C14	2	Capacitor, ceramic, 22 μF, 16 V, X5R, 20%	1812	TDK	C4532X5R1C226MT
C15	1	Capacitor, ceramic, 47 μF, 6.3 V, X5R, 20%	1812	TDK	C4532X5R0J476MT
C16, C17(1)	2	Capacitor, POSCAP, 470 μF, 4 V, 10 mΩ, 20%	7343 (D)	Sanyo	4TPD470M
C2, C8, C10, C11, C18	5	Capacitor, ceramic, 0.1 μF, 25 V, X7R, 10%	805	Vishay	VJ0805Y104KXXAT
C3	1	Capacitor, ceramic, 2.2 nF, 50 V, X7R, 10%	805	Vishay	VJ0805Y222KXAAT
C5	1	Capacitor, ceramic, 5.6 nF, 50 V, X7R, 10%	805	Vishay	VJ0805Y562KXAAT
C6,C13	2	Capacitor, ceramic, 4.7 nF, 50 V, X7R, 10%	805	Vishay	VJ0805Y472KXAAT
C7	1	Capacitor, ceramic, 100 pF, 50 V, NPO, 10%	805	Vishay	VJ0805A101KXAAT
C9	1	Capacitor, ceramic, 1 μF, 16–V, X5R, 10%	805	TDK	C2012X5R1C105KT
D1	1	Diode, switching, 10 mA, 85 V, 350 mW	SOT23	Vishay–Liteon	BAS16
D2	1	Diode, schottky, 3 A, 40 V	SMC	IR	30BQ040
J1, J2	2	Terminal block, 4-pin, 15 A, 5.1 mm	0.80 x 0.35	OST	ED2227
L1(1)	1	Inductor, SMT, 1.7–μH, 22.3 A, 1.8 mΩ	0.512 x 0.512	Coiltronics	HC1–1R7
Q1(1)	1	MOSFET, N–channel, V_{DS} 30 V, R_{DS} 6 mΩ, I_D 30 A	LFPAK	Hitachi	HAT2168H
Q2(1)	1	MOSFET, N–channel, V_{DS} 30 V, R_{DS} 4.2 mΩ, I_D 40 A	LFPAK	Hitachi	HAT2167H
R1	1	Resistor, chip, 1 kΩ, 1/10–W, 1%	805	Std	Std
R10	1	Resistor, chip, 3.3 Ω, 1/10–W, 5%	805	Std	Std
R11	1	Resistor, chip, 0 Ω, 1/10–W, yy%	805	Std	Std
R12	1	Resistor, chip, 20 Ω, 1/10–W, 5%	805	Std	Std
R2	1	Resistor, chip, 165 kΩ, 1/10–W, 1%	805	Std	Std
R3	1	Resistor, chip, 5.49 kΩ, 1/10–W, 1%	805	Std	Std
R4	1	Resistor, chip, 243 kΩ, 1/10–W, 1%	805	Std	Std
R5	1	Resistor, chip, 10 kΩ, 1/10–W, 1%	805	Std	Std
R6	1	Resistor, chip, 71.5 kΩ, 1/10–W, 1%	805	Std	Std
R7	1	Resistor, chip, 8.66 kΩ, 1/10–W, 1%	805	Std	Std
R8	1	Resistor, chip, 226 Ω, 1/10–W, 1%	805	Std	Std
R9	1	Resistor, chip, 16.2 kΩ, 1/10–W, 1%	805	Std	Std
TP1, TP4, TP5, TP7, TP9	5	JACK, test point, red		Farnell	240–345
TP2, TP3, TP6, TP10	4	JACK, test point, black		Farnell	240–333
TP8	1	Adaptor, 3.5 mm probe clip	0.2	Tektronix	131–4244–00 or 131–5031–00
U1(1)	1	Wide input synchronous buck controller	PWP16	TI	TPS40051PWP
—	1	PCB, 2.85” x 2” x .062 In		Std	SLUP195

(1) Should not be substituted.

9 References

1. Data Sheet, TPS40051 Wide-Input Synchronous Buck Controller, Texas Instruments Literature Number SLUS540.
2. Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature Number SLMA002

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