MP3217

36V, 670kHz Step-up Converter with a 0.5A Switch

The Future of Analog IC Technology

DESCRIPTION

The MP3217 is a monolithic step up converter integrating a 0.5A, 0.6Ω internal switch. The MP3217 uses current mode, fixed frequency architecture to regulate the output voltage, providing fast transient response and cycle by cycle current limit.

The MP3217 includes under-voltage lockout, over voltage protection and thermal overload protection preventing damage in the event of an output overload.

The MP3217 is available in small 6-pin TSOT23 package. The device is ROHS compliance.

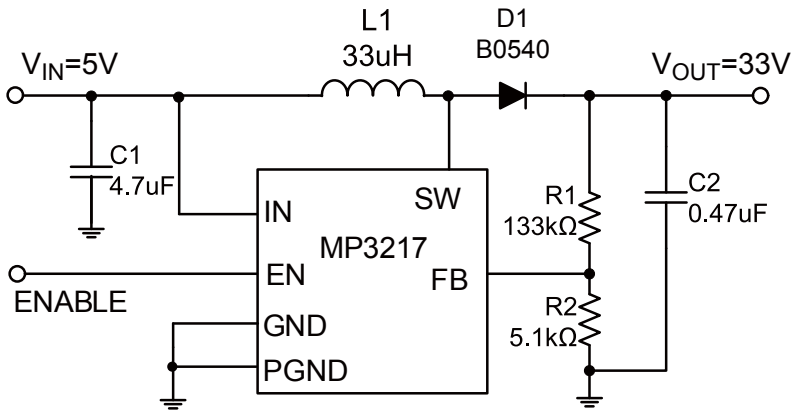
FEATURES

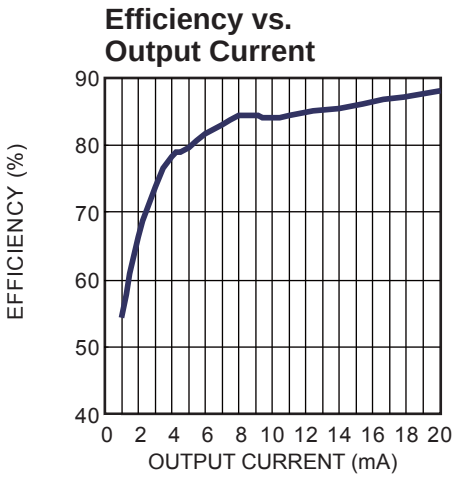
- Internal 0.6Ω Power MOSFET
- Up to 36V Output Voltage
- 670kHz Fixed Switching Frequency
- 42V Over Voltage Shutdown
- Cycle-by-Cycle Over Current Protection
- UVLO, Thermal Shutdown
- Available in TSOT23-6 Packages

APPLICATIONS

- APD Bias Generation
- Portable Applications
- Handheld Computers and PDAs
- Digital Still Cameras

TYPICAL APPLICATION



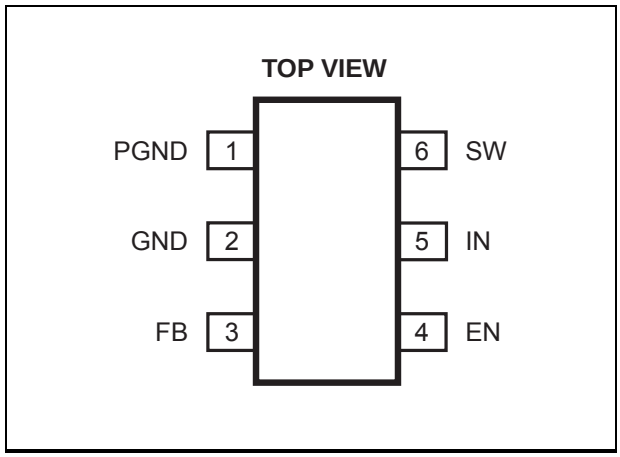


ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP3217DJ	TSOT23-6	7H	-40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP3217DJ–Z);
For RoHS Compliant Packaging, add suffix –LF (e.g. MP3217DJ–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

SW Pin.....-0.5V to +44V
All Other Pins.....-0.3V to +6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
..... 0.56W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -55°C to +150°C

Recommended Operating Conditions (3)

IN Supply Voltage .....2.5V to 6V
SW Pin.....V_{IN} to 36V
Operating Junct. Temp (T_J)..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6 .....220 .... 110 .. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 5V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Operating Input Voltage	V_{IN}		2.5		6	V
Supply Current (Shutdown)		V_{EN} = 0V			10	μA
Supply Current (Quiescent)		V_{FB} = 0.15V		460	560	μA
Switching Frequency	f_{SW}		570	670	770	kHz
Maximum Duty Cycle		V_{FB} = 0V	92			%
Under Voltage Lockout						
IN Under Voltage Lockout	UVLO	V_{IN} Rising		2.25	2.45	V
Under Voltage Lockout Hysteresis				92		mV
Over Voltage Shutdown Threshold	V_{OV}	V_{OV} Rising		42		V
Enable						
EN OFF Threshold		V_{EN} Falling	0.8			V
EN ON Threshold		V_{EN} Rising			2	V
Feedback						
FB Voltage	V_{FB}		1.20	1.24	1.28	V
FB Input Bias Current		V_{FB} = 1.2V		-100		nA
Output Switch						
SW On-Resistance (5)	R_{ON}			0.6		Ω
SW Current Limit (5)		Duty Cycle = 60%		0.50		A
Thermal Shutdown (5)				150		°C

Notes:

5) Guaranteed by design.

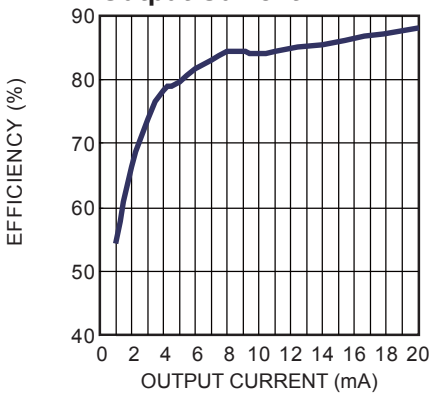
PIN FUNCTIONS

Pin #	Name	Pin Function
1	PGND	Power Ground.
2	GND	Ground.
3	FB	Feedback Input. Reference voltage is 1.24V, Connect a resistor divider from the output to this pin.
4	EN	ON/OFF Control Input. A voltage greater than 2V will turn the part on and less than 0.8V will turn the part off. When not used, float EN to the input source for automatic startup.
5	IN	Input Supply Pin. Must be locally bypassed.
6	SW	Power Switch Output. SW is the drain of the internal MOSFET switch. Connect the power inductor and output rectifier to SW.

TYPICAL PERFORMANCE CHARACTERISTICS

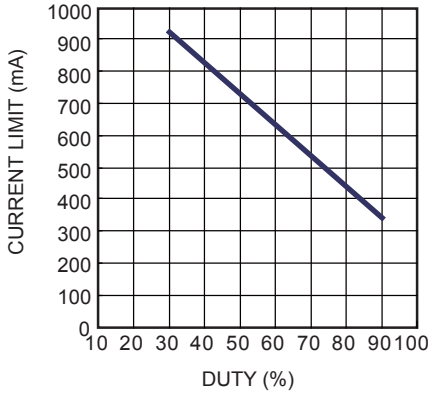
Circuit refer to Figure 2, V_{IN}=5V, V_{OUT}=33V, T_A=+25°C, unless otherwise noted.

Efficiency vs. Output Current

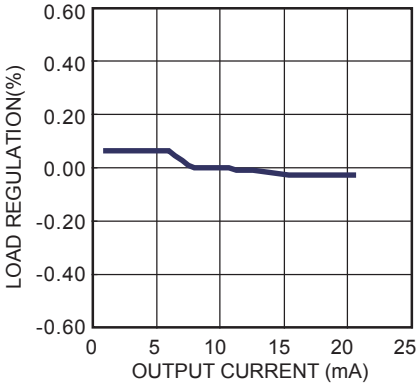


Current Limit vs. Duty

V_{FB}=0V

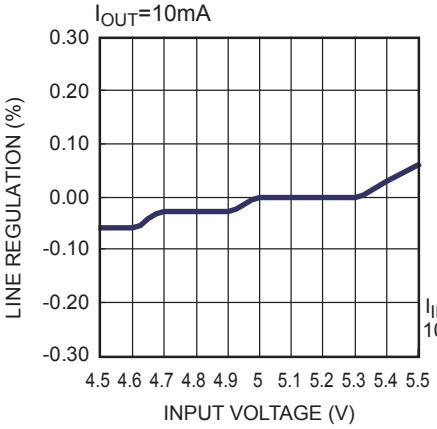


Load Regulation



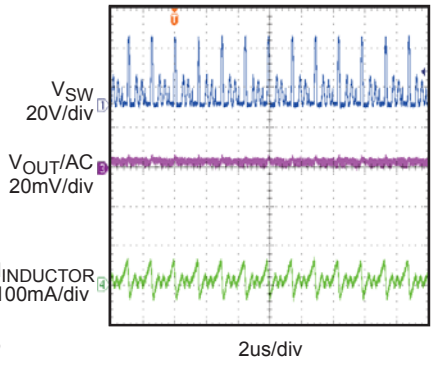
Line Regulation

I_{OUT}=10mA



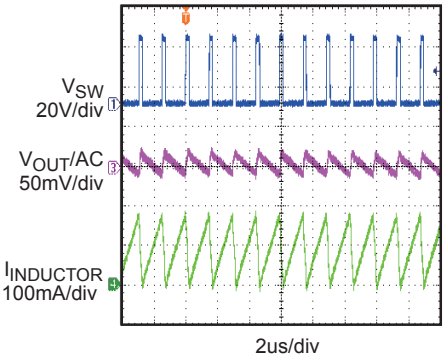
Steady State

I_{OUT}=0mA



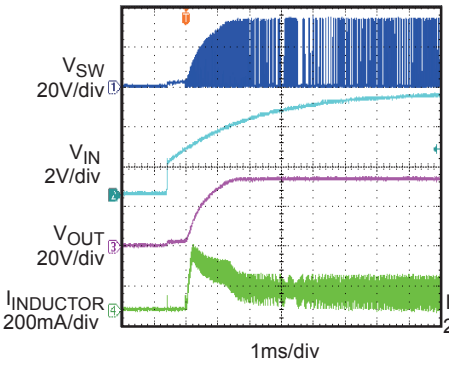
Steady State

I_{OUT}=10mA



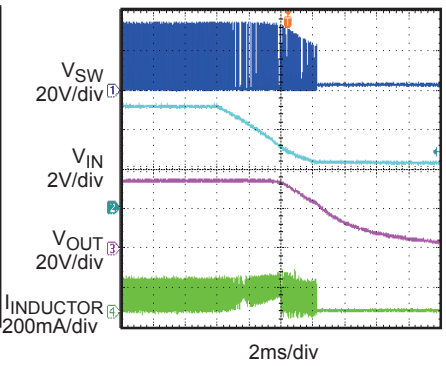
V_{IN} Power On

I_{OUT}=10mA



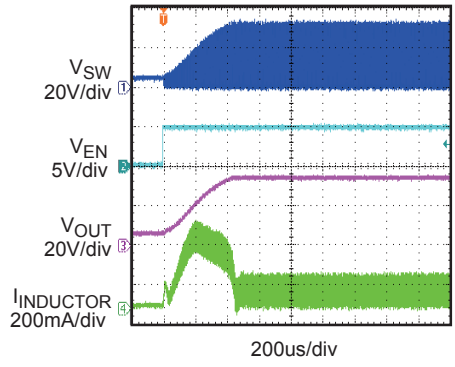
V_{IN} Power Off

I_{OUT}=10mA



EN Power On

I_{OUT}=10mA

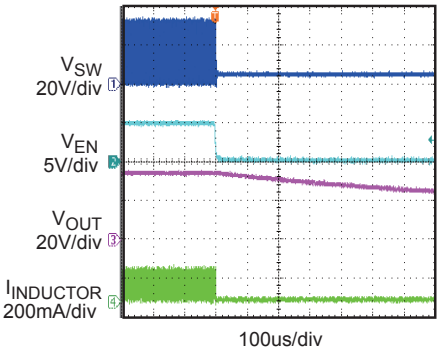


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Circuit refer to Figure 2, V_{IN}=5V, V_{OUT}=33V, T_A=+25°C, unless otherwise noted.

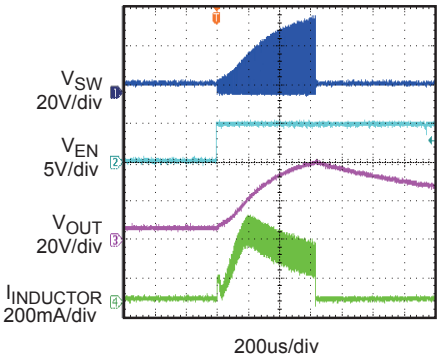
EN Power Off

I_{OUT}=10mA



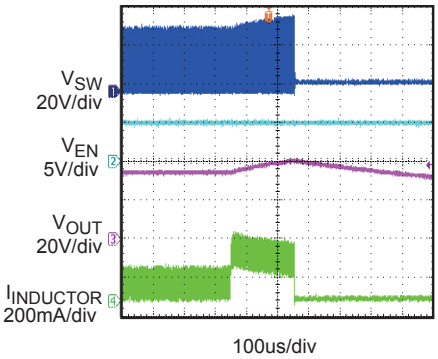
Over Voltage Protection

Start up without R1



Over Voltage Protection

Remove R1 at working



OPERATION

The MP3217 uses a constant frequency, peak current mode boost regulator architecture to regulate the output voltage. The operation of the MP3217 can be understood by referring to the block diagram of Figure 1.

At the start of each oscillator cycle the FET is turned on through the control circuitry. To prevent sub-harmonic oscillations at duty cycles greater than 50 percent, a stabilizing ramp is added to the output of the current sense amplifier and the result is fed into the positive input of the PWM comparator. When this voltage equals the output voltage of the error amplifier the power FET is turned off.

The voltage at the output of the error amplifier is an amplified version of the difference between the 1.24V reference voltage and the feedback voltage. In this way the peak current level keeps the output in regulation.

If the feedback voltage starts to drop, the output of the error amplifier increases. This results in more current flowing through the power FET, thus increasing the power delivered to the output.

Over voltage protection shuts off the MP3217 if the output voltage goes too high. In some cases, loose high side resistor or improper divided resistor; this results in the feedback voltage is always below reference. The part runs at maximum duty cycle boosting the output voltage higher and higher. If the output ever exceeds 42V, the MP3217 shuts down. And It does not switch again until the power is recycled.

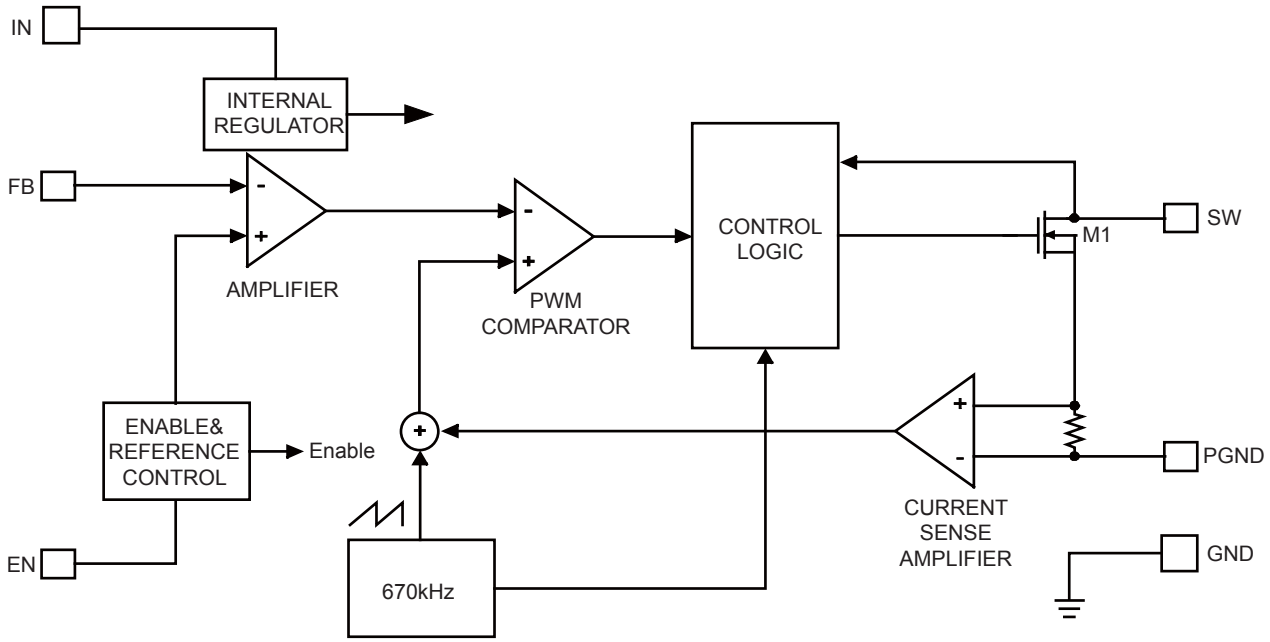


Figure 1—Functional Block Diagram

APPLICATION INFORMATION

Components referenced below apply to Typical Application Circuit refer to Figure 2.

Setting the Output Voltage

Set the output voltage by selecting the resistive voltage divider ratio. Use 5.1kΩ for the low-side resistor R2 of the voltage divider. Determine the high-side resistor R1 by the equation:

$$R1 = \frac{R2 \times (V_{OUT} - V_{FB})}{V_{FB}}$$

Where, V_{OUT} is the output voltage, V_{FB} = 1.24V.

For R2 = 5.1kΩ and V_{OUT} = 33V, then R1 = 130.6kΩ. There choose a 133kΩ standard 1% value.

Selecting the Input Capacitor

An input capacitor is required to supply the AC ripple current to the inductor, while limiting noise at the input source. This capacitor must have low ESR, so ceramic is the best choice. Use an input capacitor value of 4.7μF or greater. This capacitor must be placed physically close to the IN pin. Since it reduces the voltage ripple seen at IN, it also reduces the amount of EMI passed back along that line to the other circuitry.

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple to a minimum. The characteristic of the output capacitor also affects the stability of the regulation control system. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. In the case of ceramic capacitors, the impedance of the capacitor at the switching frequency is dominated by the capacitance, and so the output voltage ripple is mostly independent of the ESR. The output voltage ripple is estimated to be:

$$V_{RIPPLE} \approx \frac{\left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times I_{LOAD}}{C2 \times f_{SW}}$$

Where V_{RIPPLE} is the output ripple voltage, V_{IN} and V_{OUT} are the DC input and output voltages respectively, I_{LOAD} is the load current, f_{SW} is the switching frequency, and C2 is the capacitance of the output capacitor.

Selecting the Inductor

The inductor is required to force the higher output voltage while being driven by the lower input voltage. A larger value inductor results in less ripple current that results in lower peak inductor current, reducing stress on the internal power switch. However, the larger value inductor has a larger physical size, higher series resistance, and/or lower saturation current.

Inductance from 2.2μH to 33μH is a good choice for high efficiency and small size. To prevent saturation, use an inductor with a saturation current rating that is higher than the device current limit.

Selecting the Diode

The output rectifier diode supplies current to the inductor when the internal power MOSFET is off. To reduce losses due to diode forward voltage and recovery time, use a Schottky diode with the MP3217. The diode should be rated for a reverse voltage equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current.

Layout Consideration

High frequency switching regulators require very careful layout for stable operation and low noise. All components must be placed as close to the IC as possible. Keep the path between the SW pin, output diode, output capacitor and GND pin extremely short for minimal noise and ringing. The input capacitor must be placed close to the IN pin for best decoupling. All feedback components must be kept close to the FB pin to prevent noise injection on the FB pin trace. The ground return of the input and output capacitors should be tied close to the GND pin. See the MP3217 demo board layout for reference.

TYPICAL APPLICATION CIRCUIT

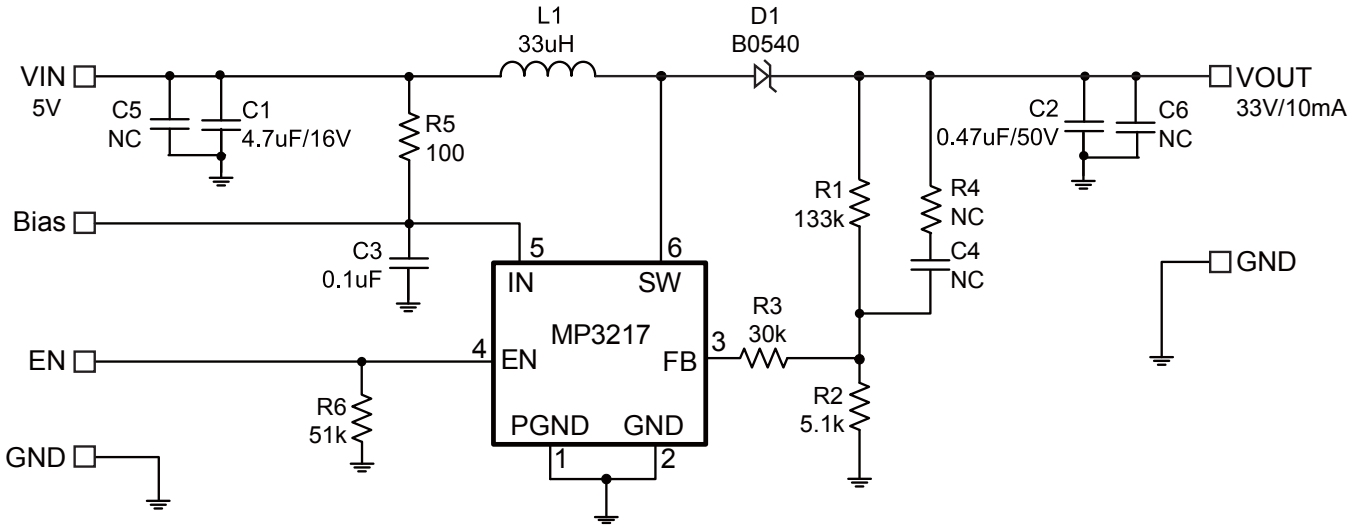


Figure 2—V_{IN}=5V V_{OUT}=33V I_{OUT}=10mA Boost Circuit

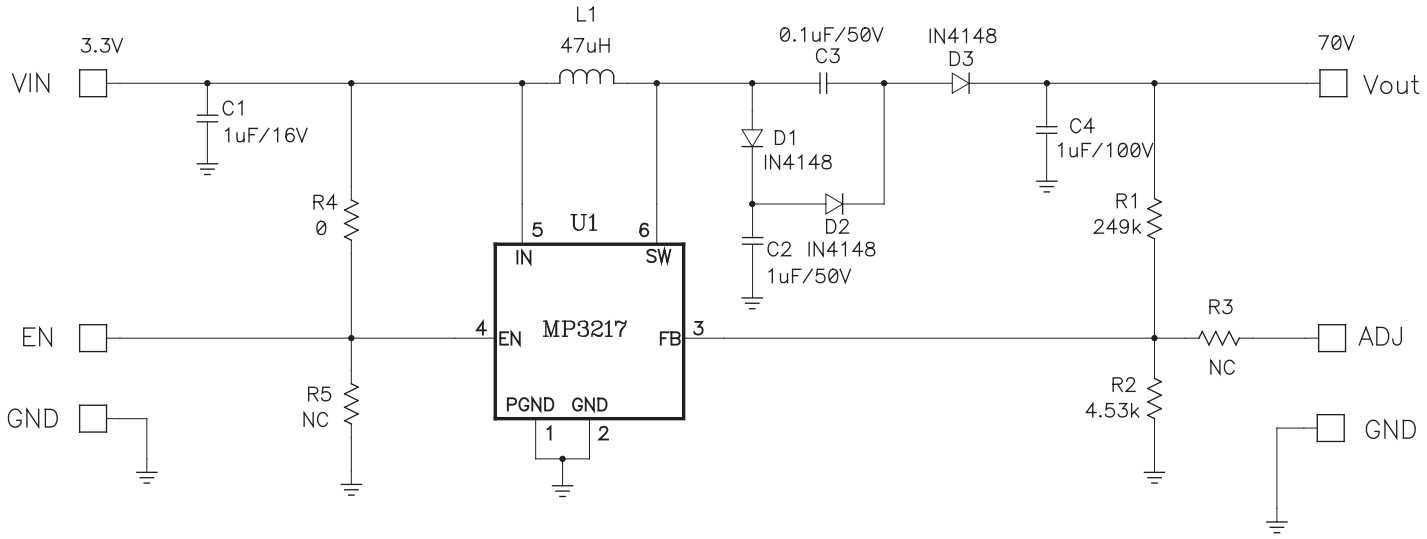
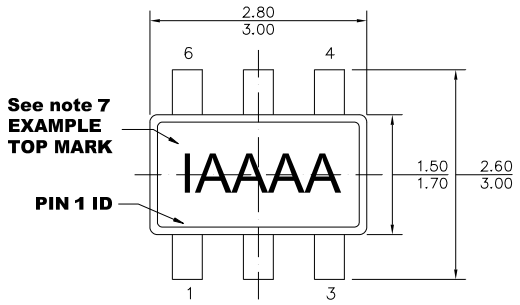


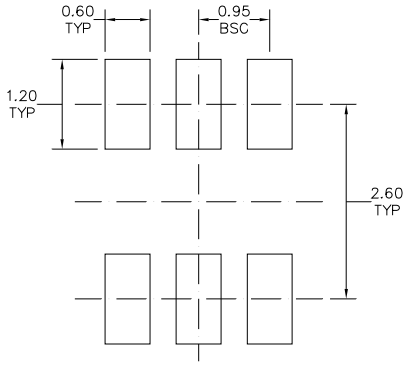
Figure 3—V_{IN}=3.3V V_{OUT}=70V Voltage Doubler Circuit

PACKAGE INFORMATION

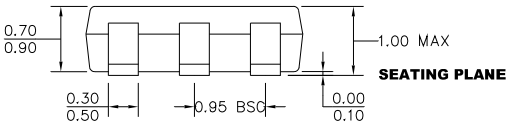
TSOT23-6



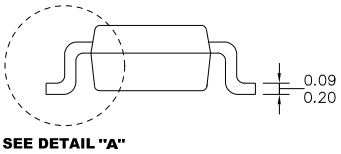
TOP VIEW



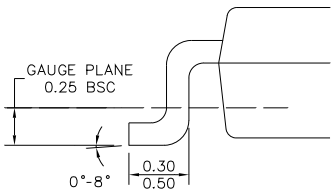
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)