

F100104 Quint AND/NAND Gate

October 1985 - Rev. 1

Memory & High Speed Logic

Description

The F100104 is a monolithic quint AND/NAND gate. The Function output is the wire-NOR of all five AND gate outputs.

$$F = (\overline{D_{1a}} \bullet \overline{D_{2a}}) + (\overline{D_{1b}} \bullet \overline{D_{2b}}) + (\overline{D_{1c}} \bullet \overline{D_{2c}}) + (\overline{D_{1d}} \bullet \overline{D_{2d}}) + (\overline{D_{1e}} \bullet \overline{D_{2e}})$$

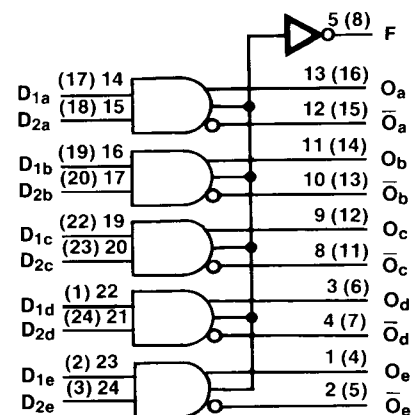
All inputs have 50K Ω pull-down resistors.

- Available in Ceramic DIP or Flatpak
- Data Input to Output Propagation Delay 1.75 ns Max
- Outputs Specified to Drive a 50 Ω Load
- Moderate Edge Rates Minimize Ringing and Reflections on Interconnecting Wiring

Pin Names

D _{1a} –D _{1e}	Data Inputs
F	Function Output
O _a –O _e	Data Outputs
$\overline{O}_a$ – $\overline{O}_e$	Complementary Data Outputs

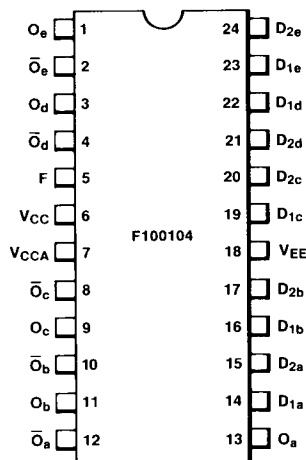
Logic Symbol



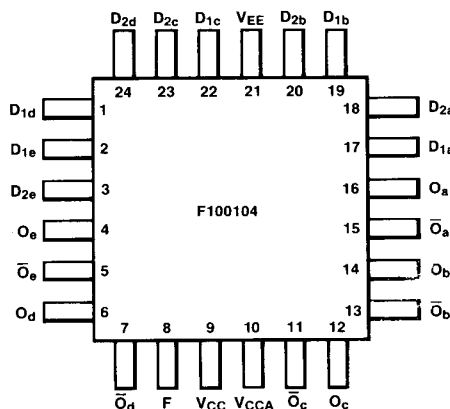
V_{CC} = Pin 6 (9)
V_{CCA} = Pins 7 (10)
V_{EE} = Pin 18 (21)
() = Flatpak

Connection Diagrams

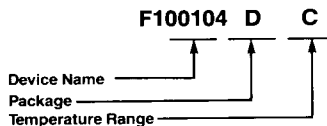
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Ordering Information



Packages

D = Ceramic DIP
F = Flatpak

Temperature Range

C = 0°C to +85°C

26

Res
003974

Org

3974

FSC

F100104

DC Characteristics: $V_{EE} = -4.2\text{ V to }-4.8\text{ V}$ unless otherwise specified, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^\circ\text{C to }+85^\circ\text{C}$

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current D _{2a} -D _{2e} D _{1a} -D _{1e}			250 350	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	-96	-66	-46	mA	Inputs Open

For further information, see F100K DC Specification in the F100K ECL Data Book.

Ceramic Dual In-line Package AC Characteristics: $V_{EE} = -4.2\text{ V to }-4.8\text{ V}$, $V_{CC} = V_{CCA} = \text{GND}$

Symbol	Characteristic	$T_C = 0^\circ\text{C}$		$T_C = +25^\circ\text{C}$		$T_C = +85^\circ\text{C}$		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay D _{na} -D _{ne} to O, $\bar{O}$	0.40	1.75	0.40	1.65	0.40	1.75	ns	Figures 1 and 2
t _{PLH} t _{PHL}	Propagation Delay Data to F	1.00	2.60	1.00	2.60	1.15	3.20	ns	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.70	0.35	1.55	0.35	1.70	ns	

Flatpak AC Characteristics: $V_{EE} = -4.2\text{ V to }-4.8\text{ V}$, $V_{CC} = V_{CCA} = \text{GND}$

Symbol	Characteristic	$T_C = 0^\circ\text{C}$		$T_C = +25^\circ\text{C}$		$T_C = +85^\circ\text{C}$		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay D _{na} -D _{ne} to O, $\bar{O}$	0.40	1.55	0.40	1.45	0.40	1.55	ns	Figures 1 and 2
t _{PLH} t _{PHL}	Propagation Delay Data to F	1.00	2.40	1.00	2.40	1.15	3.00	ns	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.60	0.35	1.45	0.35	1.60	ns	

Absolute Maximum Ratings: Above which the useful life may be impaired

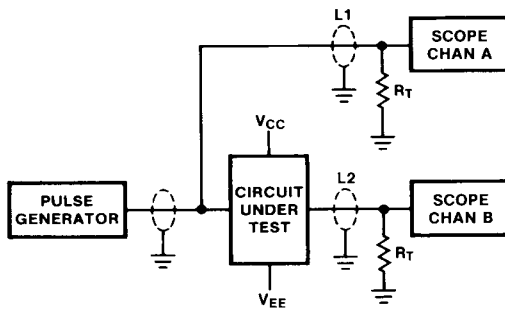
Storage Temperature	-65°C to +150°C
Maximum Junction Temperature (T _J)	+150°C
Supply Voltage Range	-7.0 V to +0.5 V
Input Voltage (dc)	V _{EE} to +0.5 V
Output Current (dc Output HIGH)	-50 mA
Operating Range	-5.7 V to -4.2 V*
Lead Temperature (Soldering 10 sec.)	300°C

Guaranteed Operating Ranges

Supply Voltage (V _{EE})			Case Temperature (T _C)
Min	Typ	Max	
-4.8 V	-4.5 V	-4.2 V	0° C to +85° C

*Parametric values specified at -4.8V to -4.2V

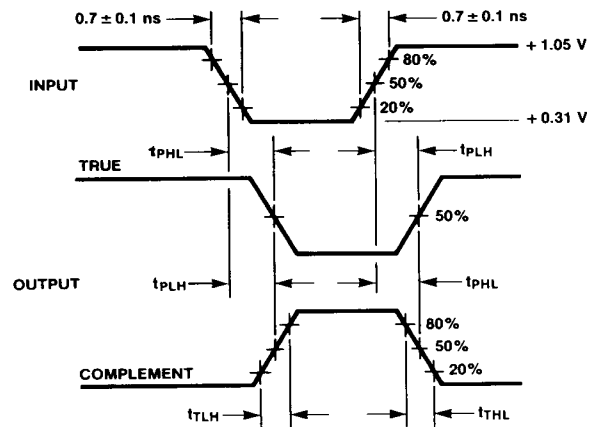
Figure 1 AC Test Circuit



Notes

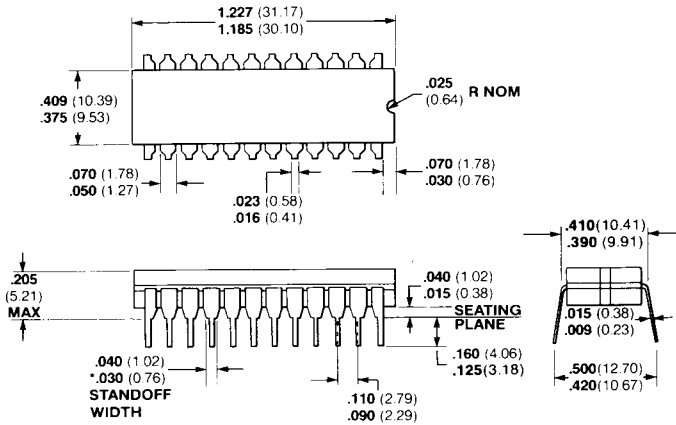
V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
 L1 and L2 = equal length 50 Ω impedance lines
 R_T = 50 Ω terminator internal to scope
 Decoupling 0.1 μ F from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50 Ω to GND
 C_L = Fixture and stray capacitance $\leq$ 3 pF

Figure 2 Propagation Delay and Transition Times



Package Outlines

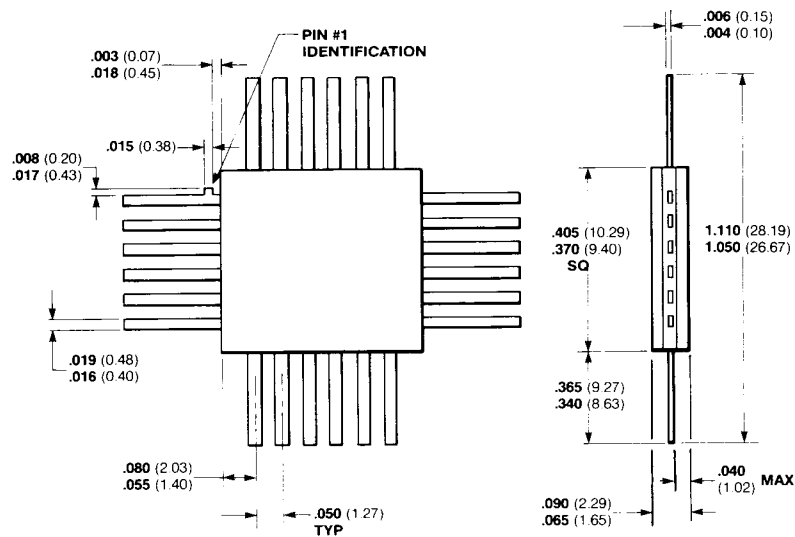
24-Pin Cerdip (.400)



Notes

Pins are tin-plated alloy 42 or equivalent
 Hermetically sealed alumina package
 Pins are intended for insertion in hole rows on .400 (10.16) centers
 They are purposely shipped with "positive" misalignment to facilitate insertion
 Package weight is 6.0 grams
 Board-drilling dimensions should equal your practice for .030 (0.76) inch diameter holes
 These dimensions include misalignment, glass over-run etc. . . .
 * The .040 - .030 dimension does not apply to the corner pins

24-Pin Quad Cerpak



Notes

Pins are tin-plated alloy 42 or equivalent
 Cavity size is .200" SQ. (5.08 SQ.)
 Package weight is 0.7 gram
 These dimensions include misalignment, glass over-run etc....

All dimensions in inches **bold** and millimeters (parentheses)

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Manufactured under one of the following U.S. Patents: 2981877, 3015048, 3064167, 3108359, 3117260; other patents pending.