

Sup/IRBuck™**USER GUIDE FOR IRDC3871 EVALUATION BOARD****DESCRIPTION**

The IR3871 Sup/IRBuck™ is an easy-to-use, fully integrated and highly efficient DC/DC voltage regulator. The onboard constant on time hysteretic controller and MOSFETs make IR3871 a space-efficient solution that delivers up to 8A of precisely controlled output voltage at 60°C ambient temperature without airflow. IR3871 is housed in a 20-lead 5mmx6mm QFN package.

Key features offered by IR3871 include: programmable switching frequency, soft start, and over current protection allowing a very flexible solution suitable for many different applications and an ideal choice for battery powered applications.

Additional features include pre-bias startup, a very precise 0.5V reference, over/under voltage protection, power good output, and enable input with voltage monitoring capability.

This user guide contains the schematic, bill of materials, and operating instructions of the IRDC3871 evaluation board. Detailed product specifications, application information and performance curves at different operating conditions are available in the IR3871 data sheet.

BOARD FEATURES

- $V_{IN} = +12V$
- $V_{CC} = +5V$
- $V_{OUT} = +1.05V$
- $I_{OUT} = 0 \text{ to } 8A$
- $F_S = 300kHz @ CCM$
- $L = 1.5\mu H$
- $C_{IN} = 22\mu F \text{ (ceramic 1210)} + 68\mu F \text{ (electrolytic)}$
- $C_{OUT} = 47\mu F \text{ (ceramic 0805)} + 330\mu F \text{ (PC-CON)}$

CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +12V input supply should be connected to VIN and PGND. A maximum load of 8A may be connected to V_{OUT} and PGND. The connection diagram is shown in Fig. 1 and inputs and outputs of the board are listed in Table 1.

IRDC3871 has two input supplies, one for biasing (VCC) and the other for input voltage (VIN). Separate supplies should be applied to these inputs. VCC input should be a well regulated 4.5V to 5.5V supply connected to VCC and PGND. Enable (EN) is controlled by the first switch of SW1. The absolute maximum voltage of the external signal applied to EN (TP4) is +8V.

Table 1. Connections

Connection	Signal Name
VIN (TP2)	VIN (+12V)
PGND (TP5)	Ground for VIN
VCC (TP16)	VCC Input (+5.0V)
PGND (TP17)	Ground for VCC Input
VOUT (TP7)	V_{OUT} (+1.05V)
PGND (TP10)	Ground for V_{OUT}
EN (TP4)	Enable Input
AGND (TP26)	Ground for Enable

LAYOUT

The PCB is a 4-layer board. All layers are 2 oz. copper. IR3871 and other components are mounted on the top and bottom layers of the board.

The power supply decoupling capacitors, bootstrap capacitor and feedback components are located close to IR3871. To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

CONNECTION DIAGRAM

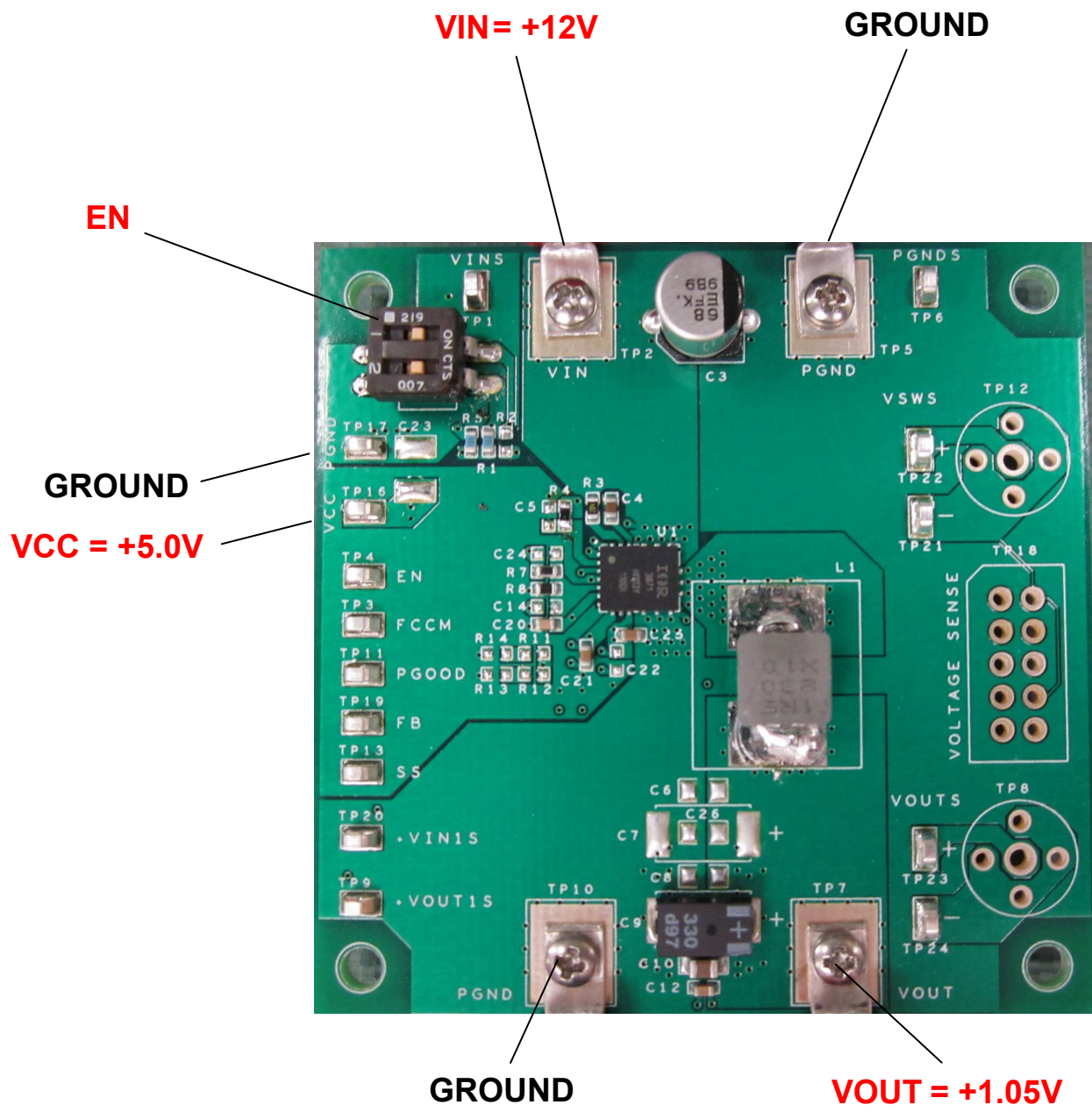


Fig. 1: Connection Diagram of IRDC3871 Evaluation Board

The diagram illustrates a complex PCB layout for a power management system. Key components and sections include:

- Power Input Section:** VIN, PGND, SW1, TP1, TP2, C3, TP5, TP6, VINS, PGND5.
- Control and Monitoring Section:** VSW5, TP22, TP21, TP18, TP17, C23, R5, R2, R1, TP16, TP4, EN, TP3, FCCM, TP11, PGOOD, TP19, FB, TP13, SS, TP20, +VIN1S, TP9, +VOUT1S, TP10, TP7, VOUT, TP23, TP24.
- Filtering and Regulation Section:** C24, R7, R8, C14, C20, R14, R1, C21, C22, C25, U1, L1, C6, C26, C7, C8, C27, C9, C10, C12.
- Grounding and Sensing Section:** PGND, VCC, PGND, VOLTAGE SENSE, TP18, TP21, TP22, TP23, TP24.

The layout is organized into functional blocks, with components labeled with their respective values and positions. The diagram shows a detailed view of the PCB design, including component footprints, traces, and labels for various components and sections.

- Single point connection between analog and power ground.

Fig. 3: Board Layout, Bottom Components

PCB Board Layout

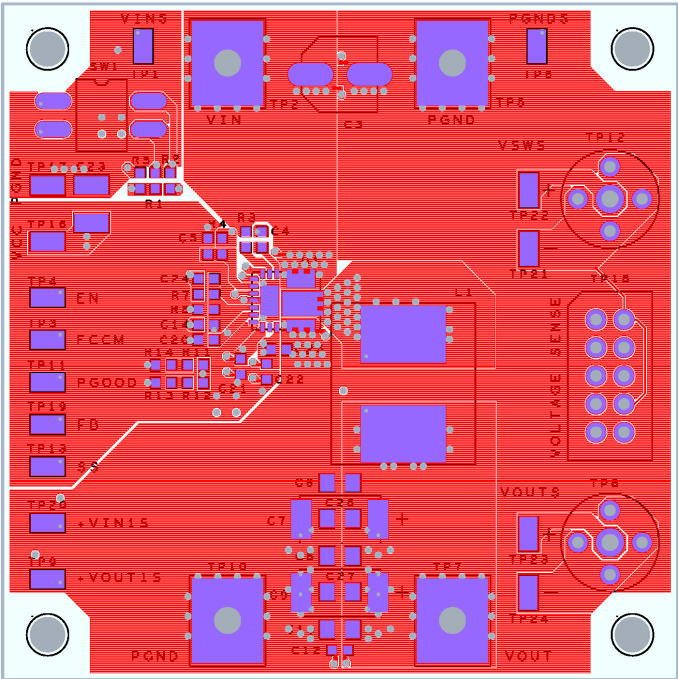


Fig. 4: Board Layout, Top Layer

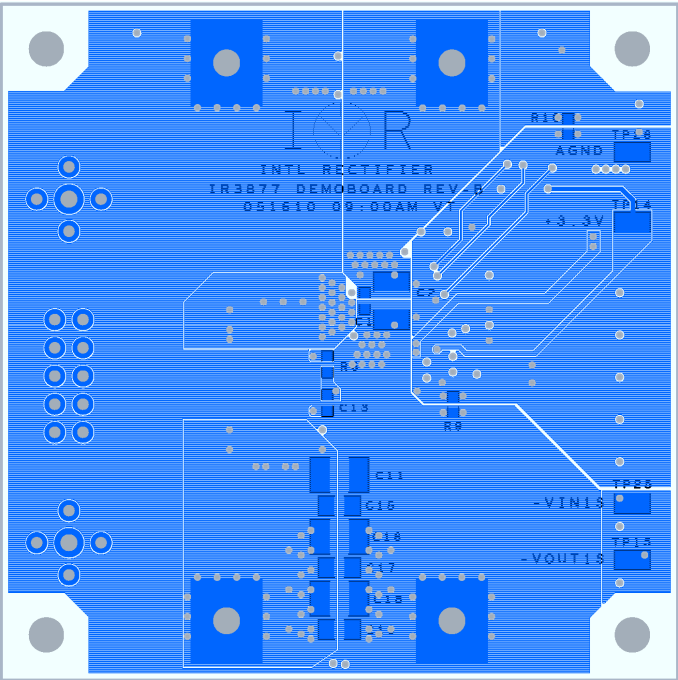


Fig. 5: Board Layout, Bottom Layer

PCB Board Layout

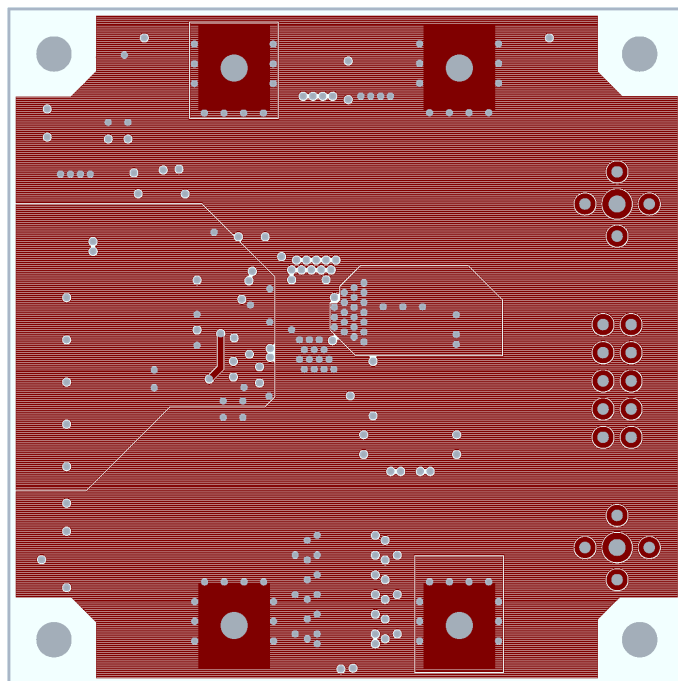


Fig. 6: Board Layout, Mid-layer I

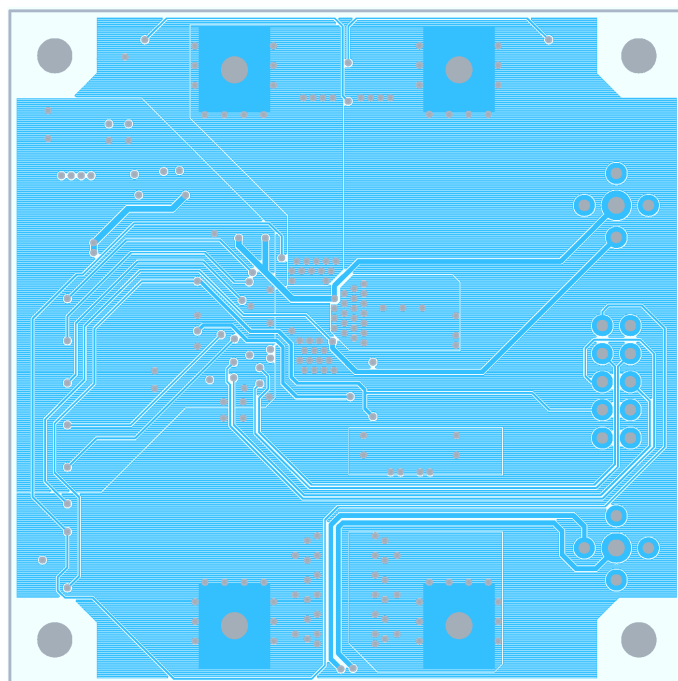


Fig. 7: Board Layout, Mid-layer II

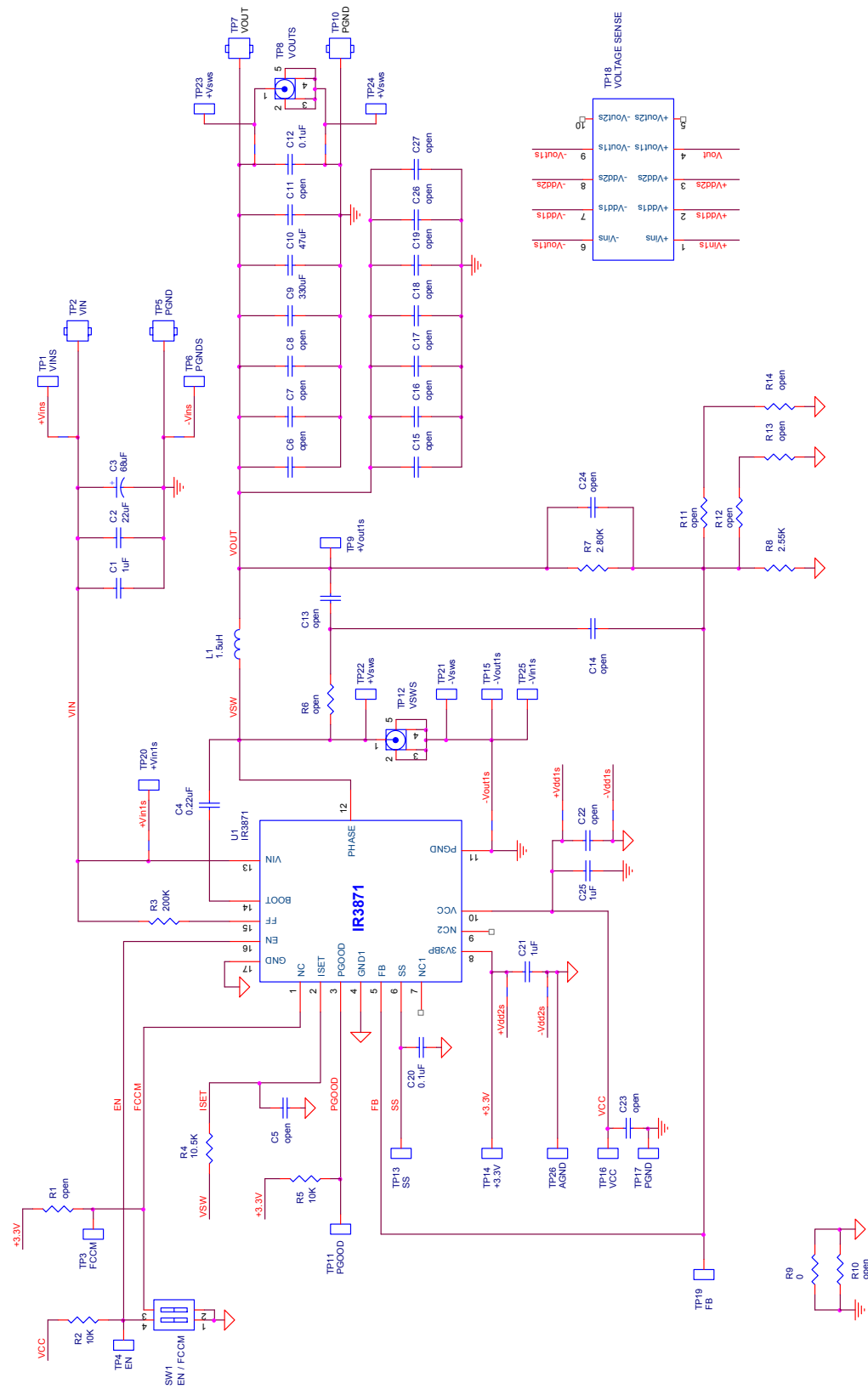


Fig. 8: Schematic of the IRDC3871 Evaluation Board

Bill of Materials

Quantity	Reference	Value	Description	Manufacturer	Part-Number
1	C4	0.22uF	CAP,CER,0.22uF,50V,10%,X7R,0603	Murata Electronics	GRM188R71H224KA64D
3	C1, C21, C25	1uF	CAP,CER,1.0uF,25V,X7R,0603	Murata Electronics	GRM188R71E105KA12D
1	C2	22uF	CAP,22uF,25V,CERAMIC,X5R,1210	Panasonic	ECJ-4YB1E226M
1	C3	68uF	CAP,68uF,25V,ELECT,FK,SMD	Panasonic	EEV-FK1E680P
1	C9	330uF	POSCAP, 330uF, 2.5V, SMD	Sanyo	2R5TPE330M9
1	C10	47uF	CAP,CER,47uF,6.3V,X5R,0805	TDK	C2012X5R0J476M
2	C12, C20	0.1uF	CAP,CER,0.1uF,50V,10%,X7R,0603	TDK	C1608X7R1H104K
1	L1	1.5uH	INDUCTOR, 1.5uH, 11A, 6.7mOhm,SMD	CYNTEC	PCMB065T-1R5MS
2	R2, R5	10K	RES,10.0K,OHM,1/10W,1%,0603,SMD	Vishay/Dale	CRCW060310K0FKEA
1	R9	0	RES,0.0,OHM,1/10W,1%,0603,SMD	Vishay/Dale	CRCW06030000Z0EAHP
1	R3	200K	RES,200K,OHM,1/10W,1%,0603,SMD	Vishay/Dale	CRCW0603200KFKEA
1	R4	10.5K	RES,10.5K,OHM,1/10W,1%,0603,SMD	Vishay/Dale	CRCW060310K5FKEA
1	R7	2.8K	RES,2.8K,OHM,1/10W,1%,0603,SMD	Vishay/Dale	CRCW06032K80FKEA
1	R8	2.55K	RES,2.55K,OHM,1/10W,1%,0603,SMD	Vishay/Dale	CRCW06032K55FKEA
1	SW1	SPST	SWITCH, DIP, SPST, SMT	C&K Components	SD02H0SK
1	U1	IR3871	5mm x 6mm QFN	IR	IR3871MPBF

TYPICAL OPERATING WAVEFORMS

Tested with demoboard shown in Fig. 8, VIN = 12V, VCC = 5V, VOUT = 1.05V, Fs = 300kHz, TA = 25°C, no airflow, unless otherwise specified

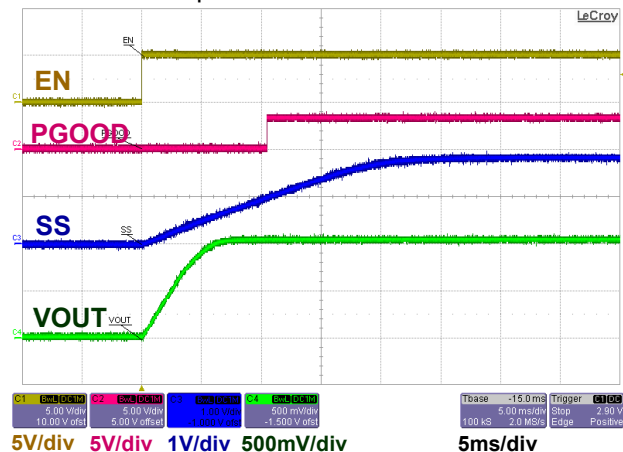


Fig. 9: Startup¹

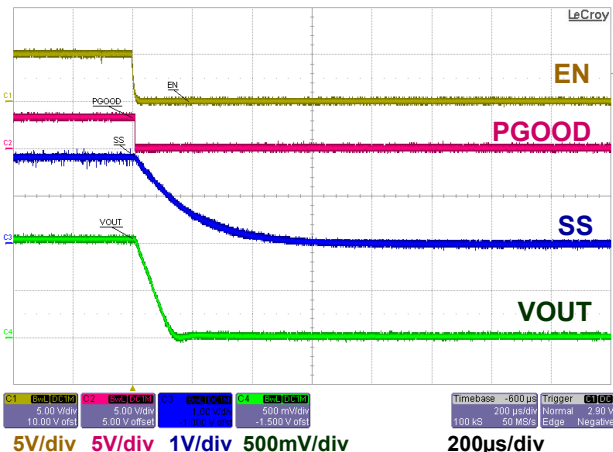


Fig. 10: Shutdown¹

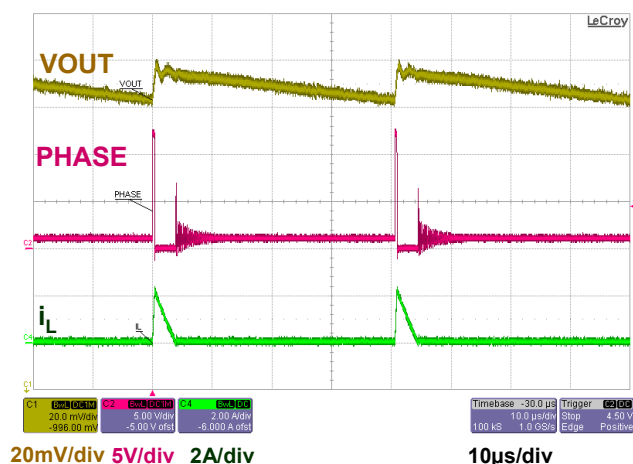


Fig. 11: DCM ($I_{OUT} = 0.1A$)²

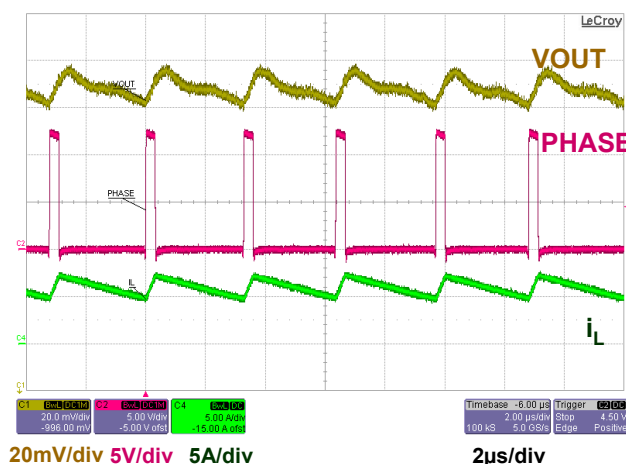


Fig. 12: CCM ($I_{OUT} = 6A$)²

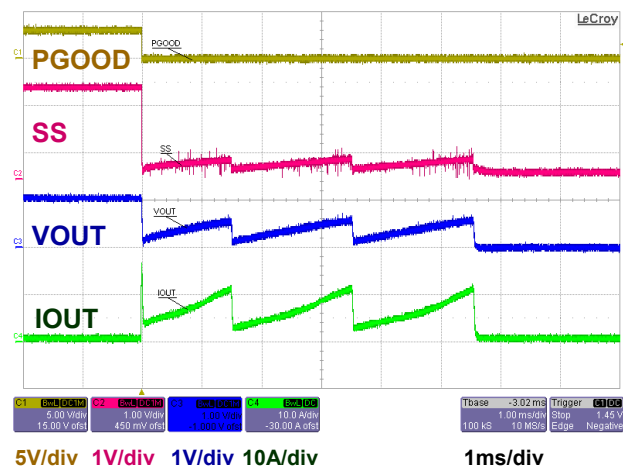


Fig. 13: Over Current Protection (tested by shorting VOUT to PGND on demoboard)

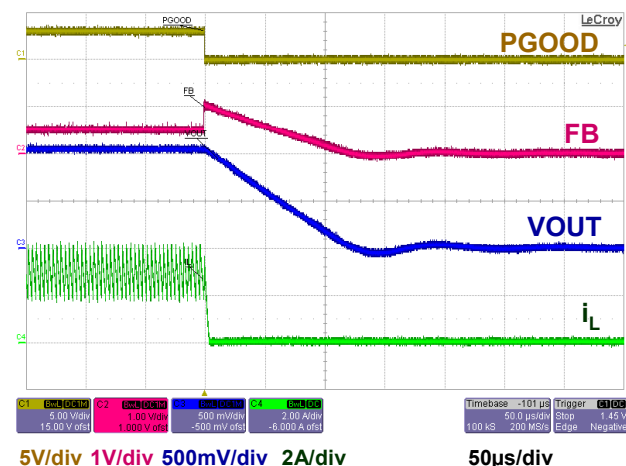


Fig. 14: Over Voltage Protection (tested by shorting FB to VOUT)

Note1: Enable is pulled up to VCC after VIN = 12V and VCC = 5V are applied.

Note2: VOUT ripple is measured across the 47µF output capacitor.

TYPICAL OPERATING WAVEFORMS

Tested with demoboard shown in Fig. 8, VIN = 12V, VCC = 5V, VOUT = 1.05V, Fs = 300kHz, TA = 25°C, no airflow, unless otherwise specified

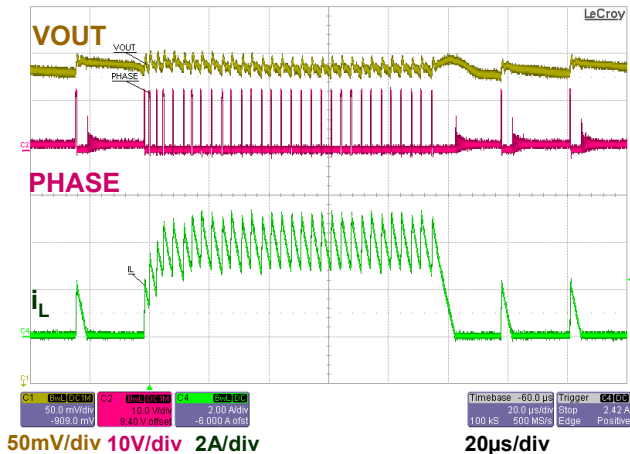


Fig. 15: Load Transient 0-4A

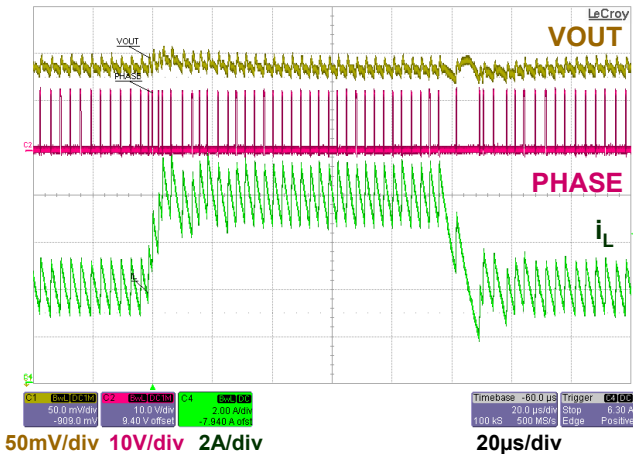


Fig. 16: Load Transient 4-8A

TYPICAL PERFORMANCE

VIN = 12V, VCC = 5V, VOUT = 1.05V, Fs = 300kHz, IOUT = 8A, TA = 25°C, no airflow

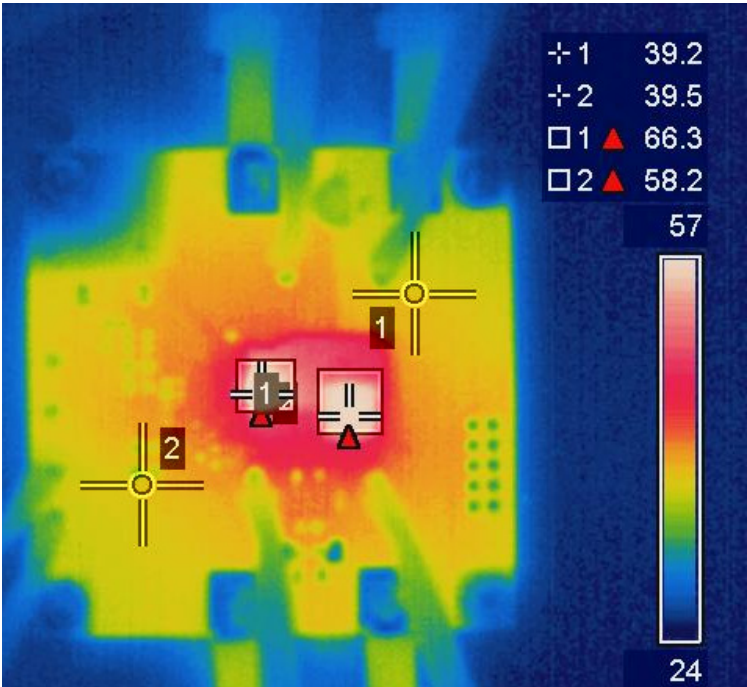


Fig. 17: Thermal Image (IR3871: 66°C, Inductor: 58°C, PCB: 40°C)

TYPICAL OPERATING DATA

VIN = 12V, VCC = 5V, VOUT = 1.05V, Fs = 300kHz, IOUT = 0 ~ 8A, TA = 25°C, no airflow,
unless otherwise specified

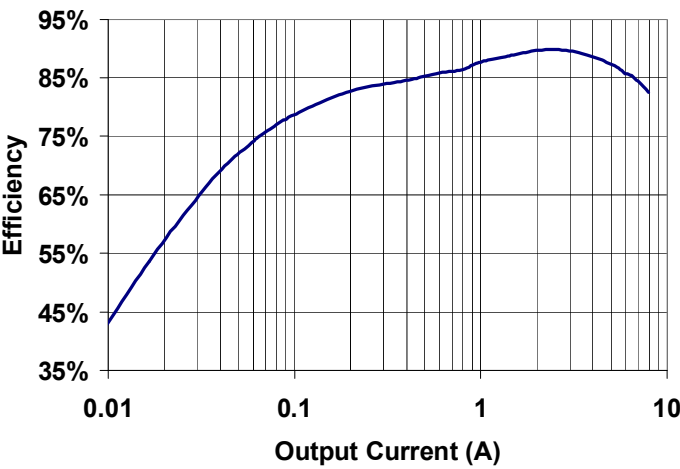


Fig. 18: Efficiency vs. Output Current

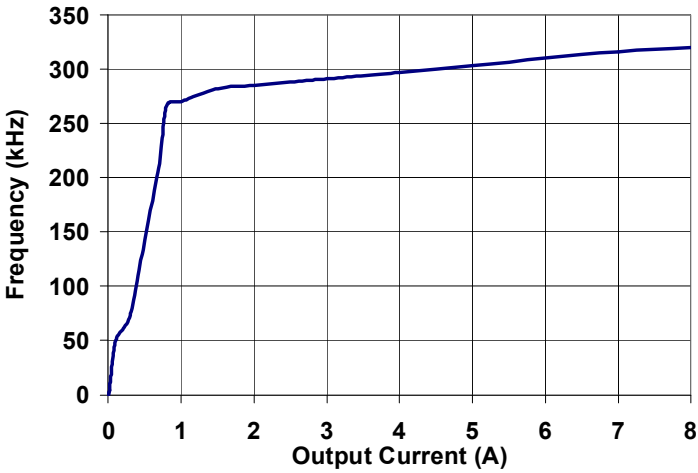


Fig. 19: Switching Frequency vs. Output Current

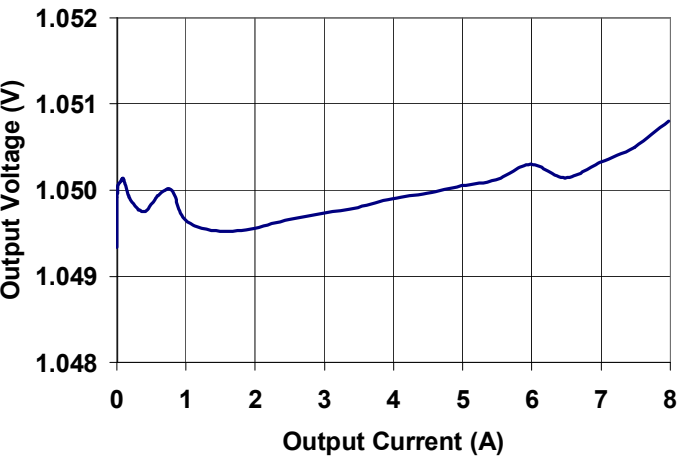


Fig. 20: Load Regulation

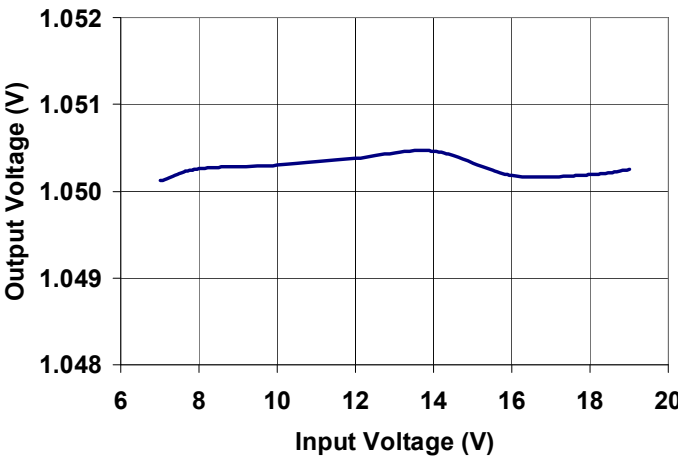


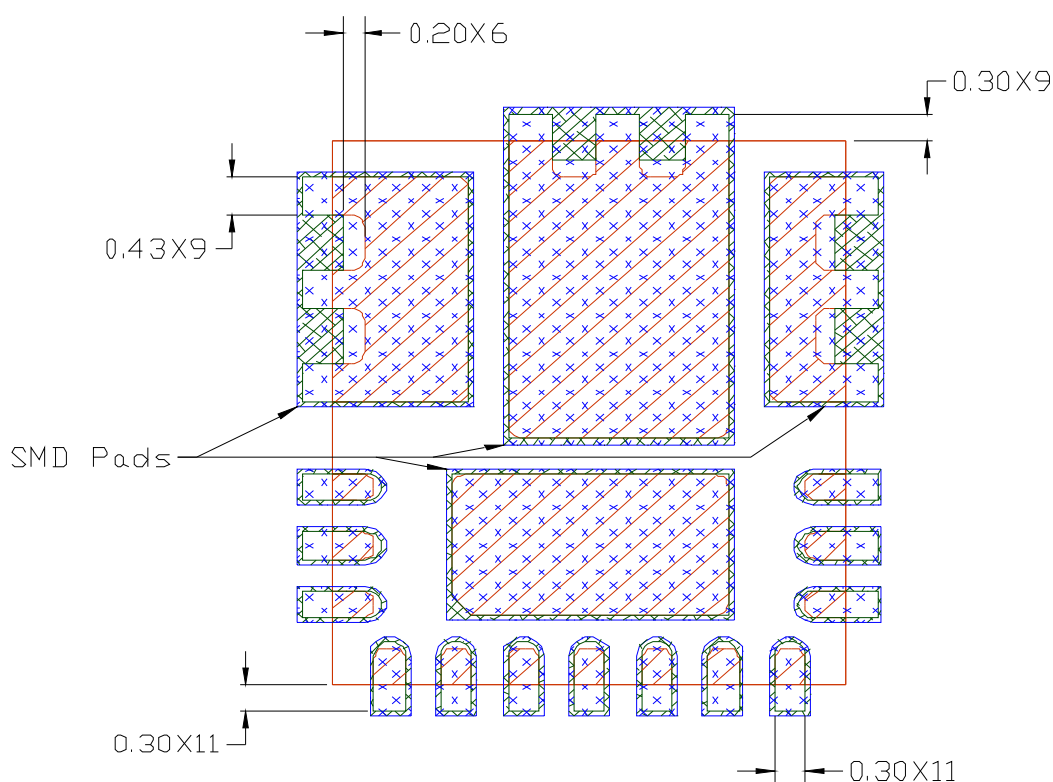
Fig. 21: Line Regulation at 8A Load

PCB Metal and Components Placement

Lead lands (the 13 IC pins) width should be equal to nominal part lead width. The minimum lead to lead spacing should be $\geq 0.2\text{mm}$ to minimize shorting.

Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension. The outboard extension ensures a large toe fillet that can be easily inspected.

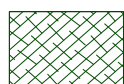
Pad lands (the 4 big pads) length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be no less than 0.17mm for 2 oz. Copper, or no less than 0.1mm for 1 oz. Copper, or no less than 0.23mm for 3 oz. Copper.



All Dimensions In mm



PCB Copper



PCB Solder Resist



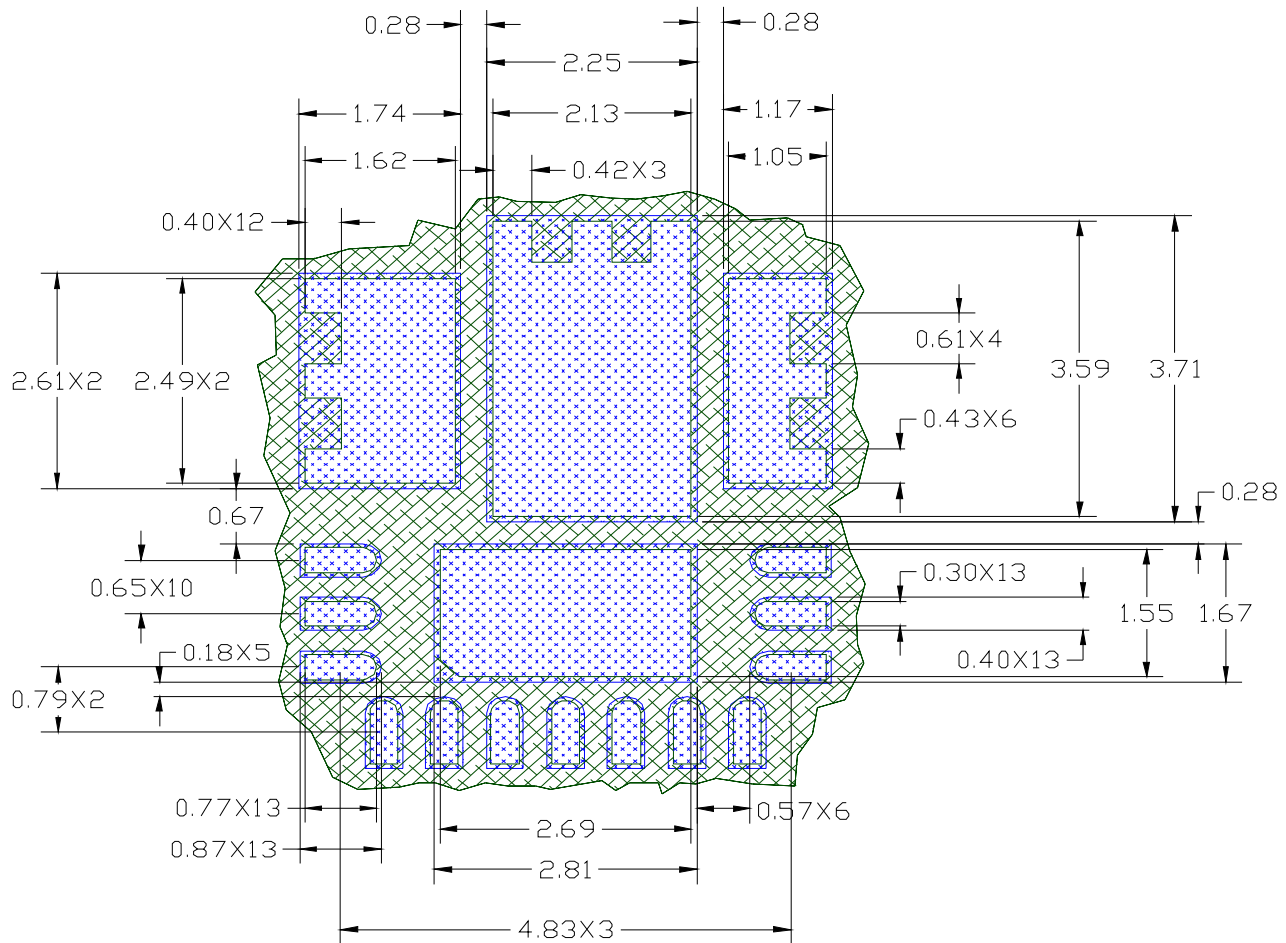
Component Pad

Solder Resist

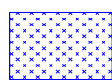
It is recommended that the lead lands are Non Solder Mask Defined (NSMD). The solder resist should be pulled away from the metal lead lands by a minimum of 0.025mm to ensure NSMD pads.

The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.05mm to accommodate solder resist misalignment.

Ensure that the solder resist in between the lead lands and the pad land is $\geq 0.15\text{mm}$ due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.



All Dimensions In mm



PCB Copper

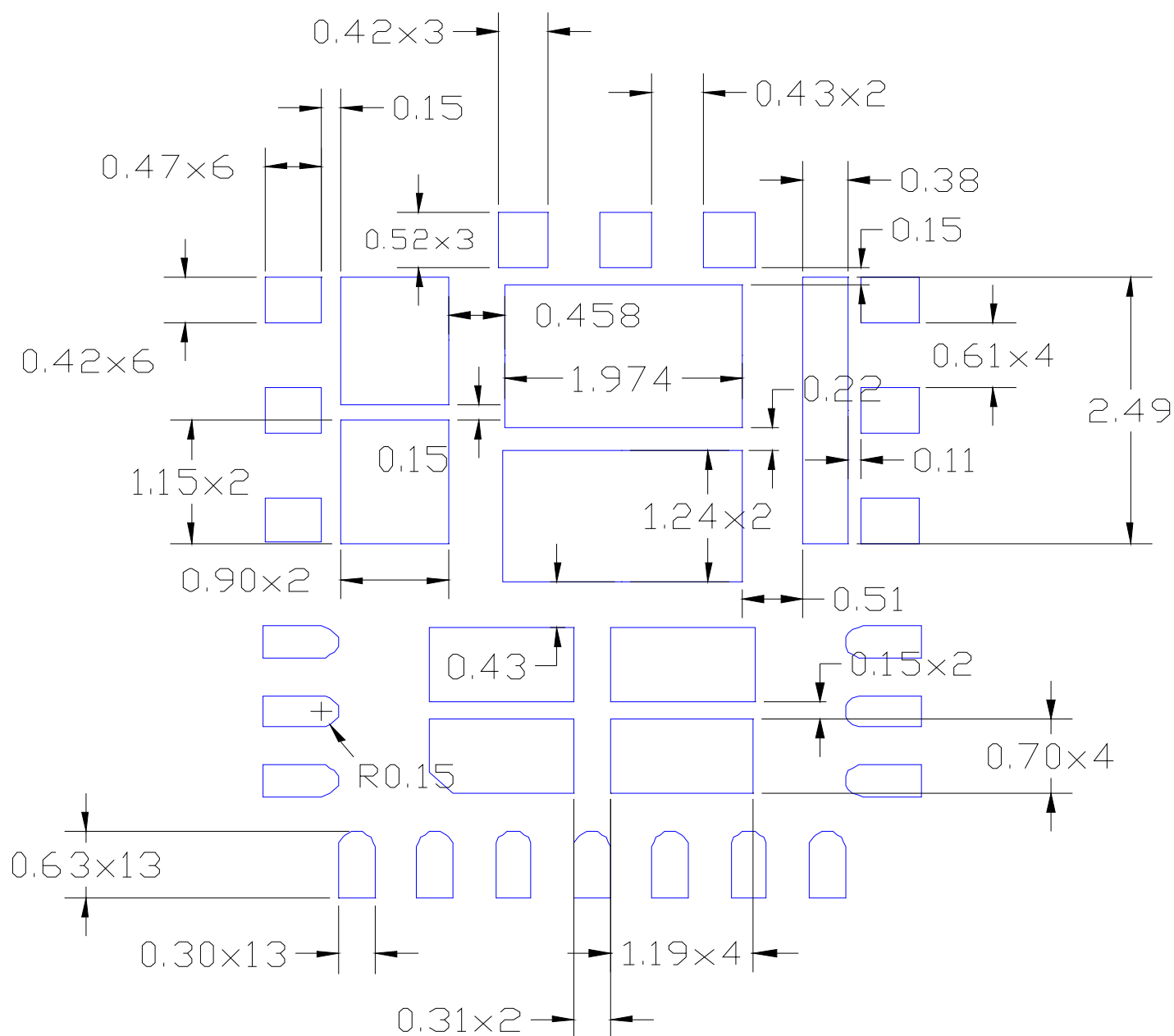


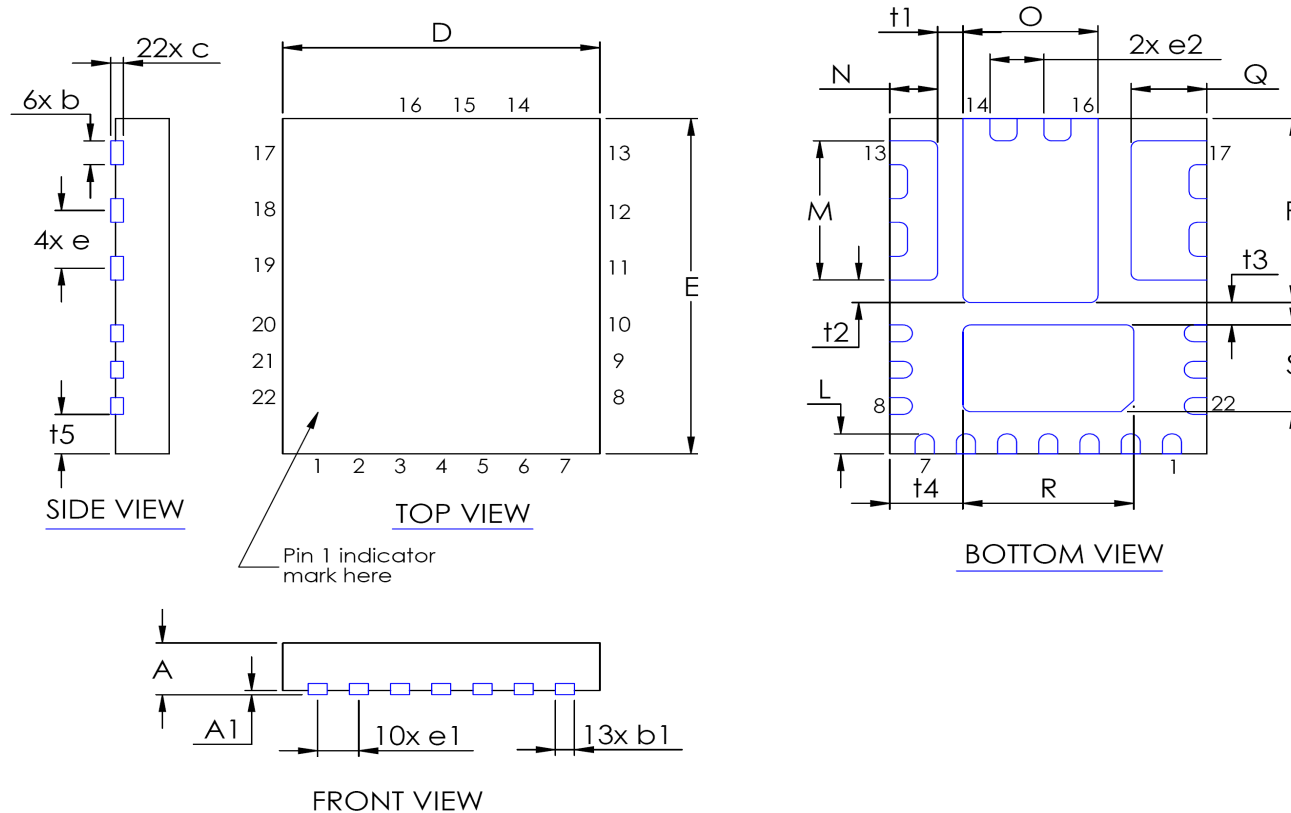
PCB Solder Resist

Stencil Design

The Stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrences of lead shorts. If too much solder is deposited on the center pad, the part will float and the lead lands will open.

The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back in order to decrease the risk of shorting the center land to the lead lands when the part is pushed into the solder paste.





DIM	MILIMITERS		INCHES		DIM	MILIMITERS		INCHES	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	0.8	1	0.0315	0.0394	L	0.35	0.45	0.0138	0.0177
A1	0	0.05	0	0.002	M	2.441	2.541	0.0962	0.1001
b	0.375	0.475	0.1477	0.1871	N	0.703	0.803	0.0277	0.0314
b1	0.25	0.35	0.0098	0.1379	O	2.079	2.179	0.0819	0.0858
c	0.203 REF.		0.008 REF.		P	3.242	3.342	0.1276	0.1316
D	5.000 BASIC		1.970 BASIC		Q	1.265	1.365	0.0498	0.05374
E	6.000 BASIC		2.364 BASIC		R	2.644	2.744	0.1042	0.1081
e	1.033 BASIC		0.0407 BASIC		S	1.5	1.6	0.0591	0.063
e1	0.650 BASIC		0.0256 BASIC		t1, t2, t3	0.401 BASIC		0.016 BACIS	
e2	0.852 BASIC		0.0259 BASIC		t4	1.153 BASIC		0.045 BASIC	
					t5	0.727 BASIC		0.0286 BASIC	

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