

MC74LVX14

Hex Schmitt Inverter

With 5 V-Tolerant Inputs

The MC74LVX14 is an advanced high speed CMOS Schmitt inverter. The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

The MC74LVX14 is pin and functionally compatible to the MC74LVX04, but the inputs have hysteresis and, with its Schmitt trigger function, can be used as a line receiver which will receive slow input signals.

Features

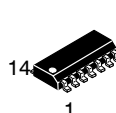
- High Speed: $t_{PD} = 6.8$ ns (Typ) at $V_{CC} = 3.3$ V
- Low Power Dissipation: $I_{CC} = 2$ μ A (Max) at $T_A = 25^\circ\text{C}$
- Powerdown Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: $V_{OLP} = 0.5$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model > 2000 V;
Machine Model > 200 V
- These Devices are Pb-Free and are RoHS Compliant



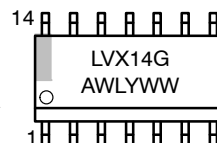
ON Semiconductor®

<http://onsemi.com>

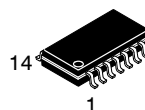
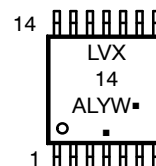
MARKING DIAGRAMS



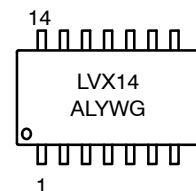
**SOIC-14
D SUFFIX
CASE 751A**



**TSSOP-14
DT SUFFIX
CASE 948G**



**SOEIAJ-14
M SUFFIX
CASE 965**



LVX14 = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC74LVX14

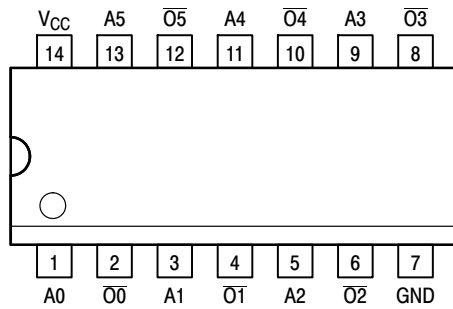


Figure 1. 14-Lead Pinout (Top View)

PIN NAMES

Pins	Function
A _n	Data Inputs
$\overline{O}_n$	Data Outputs

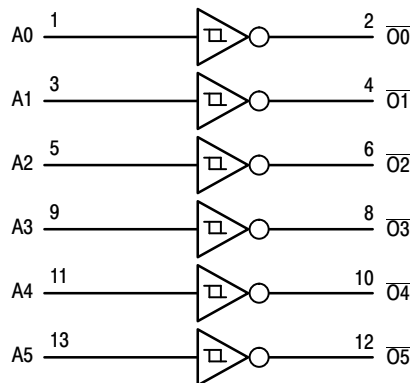


Figure 2. Logic Diagram

FUNCTION TABLE

A _n	$\overline{O}_n$
L	H
H	L

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74LVX14DR2G	SOIC-14 (Pb-Free)	2500 Tape & Reel
MC74LVX14DTR2G	TSSOP-14*	2500 Tape & Reel
MC74LVX14MG	SOEIAJ-14 (Pb-Free)	50 Units / Rail
MC74LVX14MELG	SOEIAJ-14 (Pb-Free)	2000 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MC74LVX14

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_{in}	DC Input Voltage	-0.5 to +7.0	V
V_{out}	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	Input Diode Current	-20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	-65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
V_{T+}	Positive Threshold Voltage (Figure 5)		3.0			2.20		2.20	V
V_{T-}	Negative Threshold Voltage (Figure 5)		3.0	0.90			0.90		V
V_H	Hysteresis Voltage (Figure 5)		3.0	0.30		1.20	0.30	1.20	V
V_{OH}	High-Level Output Voltage ($V_{in} = V_{IH}$ or V_{IL})	$I_{OH} = -50 \mu\text{A}$	2.0	1.9	2.0		1.9		V
		$I_{OH} = -50 \mu\text{A}$	3.0	2.9	3.0		2.9		
		$I_{OH} = -4 \text{ mA}$	3.0	2.58			2.48		
V_{OL}	Low-Level Output Voltage ($V_{in} = V_{IH}$ or V_{IL})	$I_{OL} = 50 \mu\text{A}$	2.0		0.0	0.1		0.1	V
		$I_{OL} = 50 \mu\text{A}$	3.0		0.0	0.1		0.1	
		$I_{OL} = 4 \text{ mA}$	3.0			0.36		0.44	
I_{in}	Input Leakage Current	$V_{in} = 5.5 \text{ V or GND}$	3.6			±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	$V_{in} = V_{CC} \text{ or GND}$	3.6			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ ns}$)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
t_{PLH} , t_{PHL}	Propagation Delay, Input-to-Output	$V_{CC} = 2.7 \text{ V}$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		8.7 11.2	16.3 19.8	1.0 1.0	19.5 23.0	ns
		$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		6.8 9.3	10.6 14.1	1.0 1.0	12.5 16.0	
t_{OSHL} , t_{OSLH}	Output-to-Output Skew (Note 1)	$V_{CC} = 2.7 \text{ V}$ $C_L = 50 \text{ pF}$			1.5		1.5	ns
		$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $C_L = 50 \text{ pF}$			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
		Min	Typ	Max	Min	Max	
C_{in}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 2)		21				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/6$ (per buffer). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

MC74LVX14

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 3.3$ V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.3	-0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.9	V

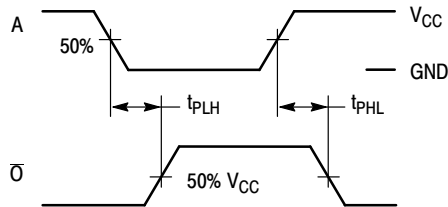
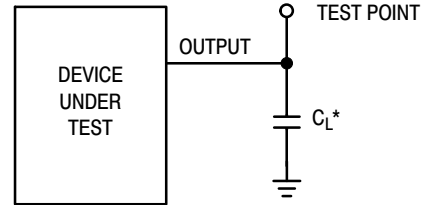


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

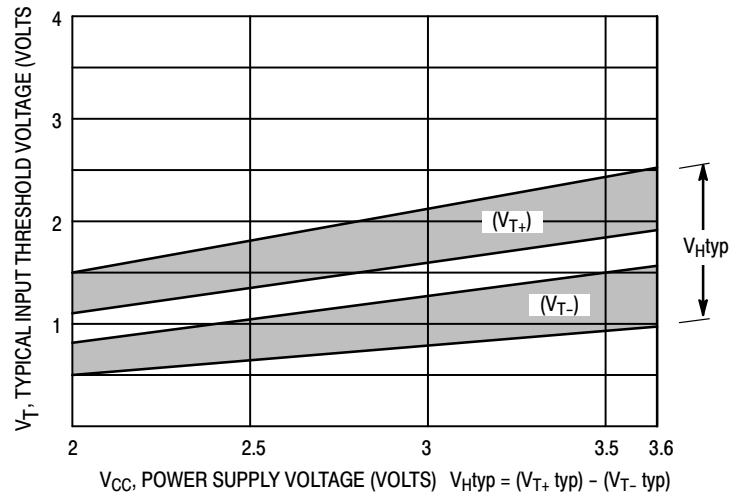
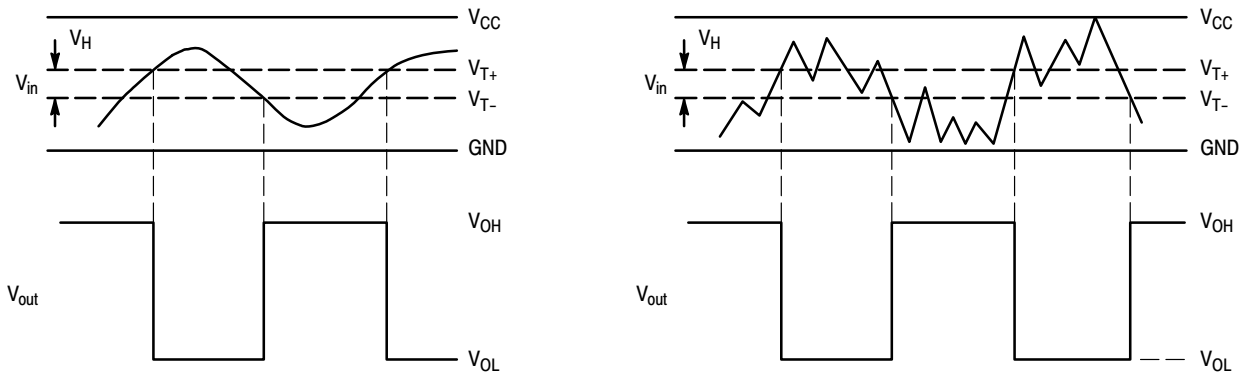


Figure 5. Typical Input Threshold, V_{T+} , V_{T-} versus Power Supply Voltage



(a) A Schmitt-Trigger Squares Up Inputs With Slow Rise and Fall Times

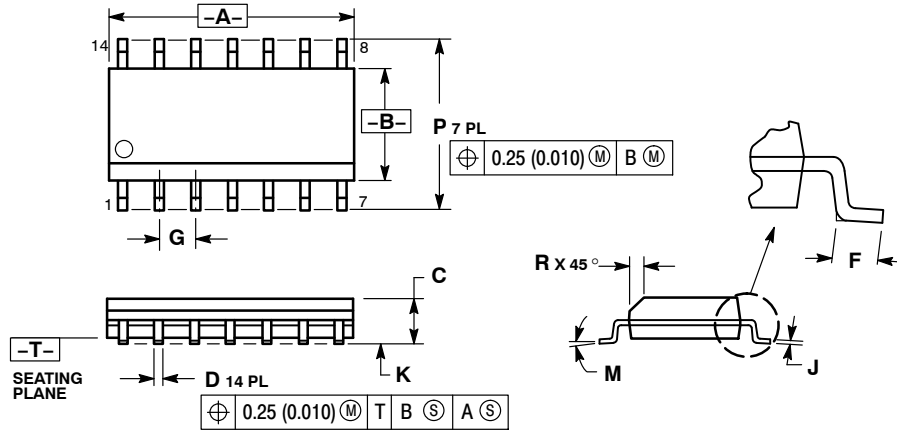
(b) A Schmitt-Trigger Offers Maximum Noise Immunity

Figure 6. Typical Schmitt-Trigger Applications

MC74LVX14

PACKAGE DIMENSIONS

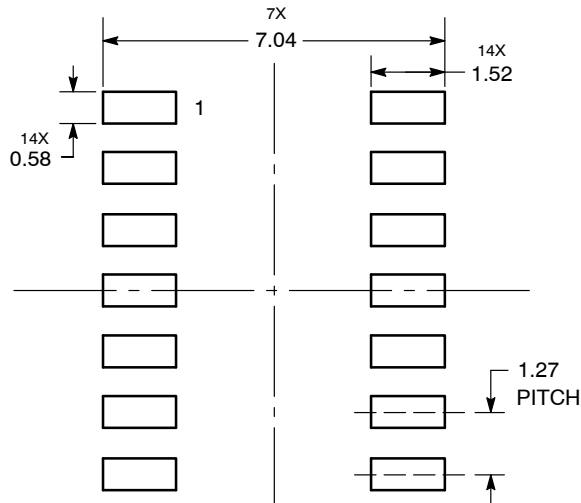
SOIC-14
D SUFFIX
CASE 751A-03
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
E	0.40	1.25	0.016	0.049
F	1.27	BSC	0.050	BSC
G	0.19	0.25	0.008	0.009
H	0.10	0.25	0.004	0.009
I	0°	7°	0°	7°
J	5.80	6.20	0.228	0.244
K	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT

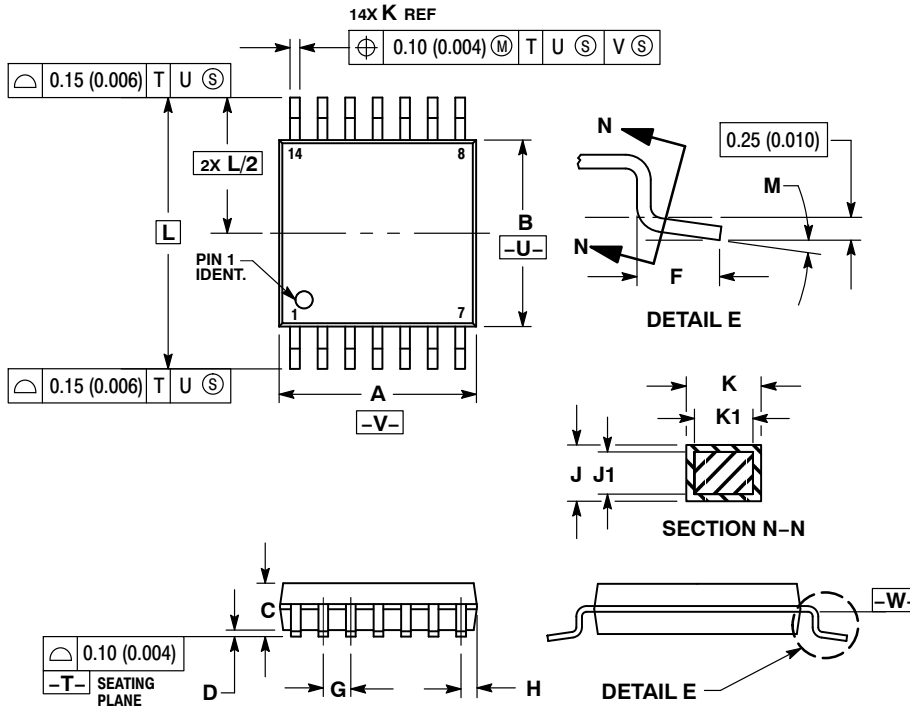


DIMENSIONS: MILLIMETERS

MC74LVX14

PACKAGE DIMENSIONS

TSSOP-14
DT SUFFIX
CASE 948G-01
ISSUE B

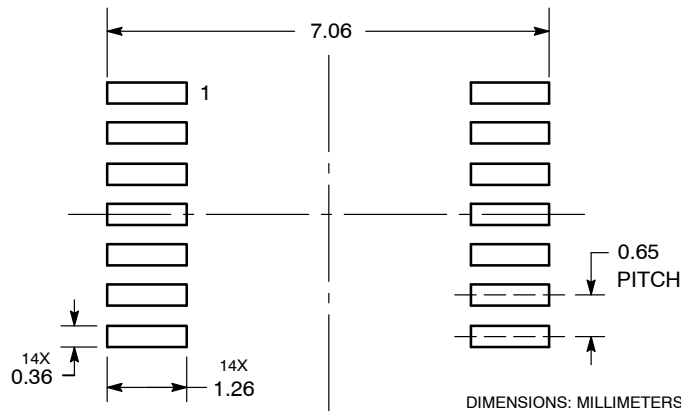


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT

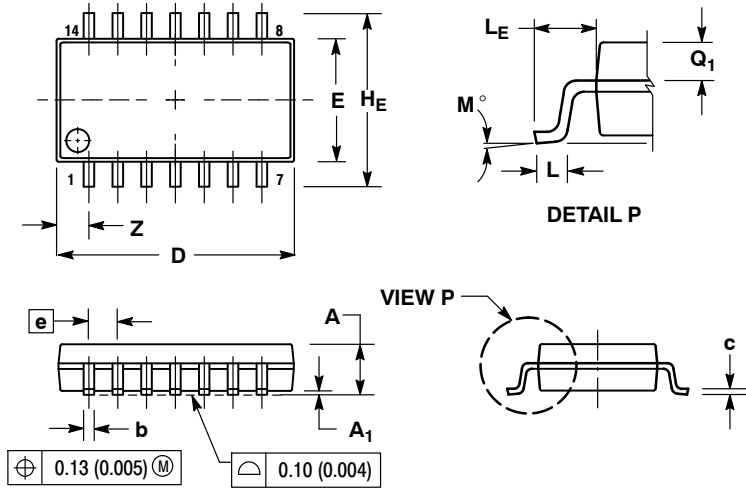


DIMENSIONS: MILLIMETERS

MC74LVX14

PACKAGE DIMENSIONS

SOEIAJ-14
CASE 965-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative