SiT8033

Low Power 2-Frequency Select Oscillator

SiTime™ It's About Time

Features, Benefits and Applications

- The world's lowest power programmable oscillator with 3.2 mA typical active current
- Selectable Output Frequency: F_0 or F_1 where $F_1 = F_0/2$, $F_0/3$, $F_0/4$, or $F_0/8$
- 1-110 MHz frequency range
- LVCMOS/LVTTL compatible output
- Frequency stability as low as ±20 PPM
- Four industry-standard packages: 2.5 x 2.0, 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm
- All-silicon device with outstanding reliability of 2 FIT (10x improvement over quartz-based devices), enhancing system mean-time-to-failure (MTBF)
- Outstanding mechanical robustness for portable applications
- Ultra short lead time
- Ideal for applications with common and related frequencies: 48/24/12 MHz for USB, 50/25 MHz for Ethernet, 24.576/12.288 MHz for audio, 54/27 MHz for video, 66/33 MHz for CPU

Specifications

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range	f	1	–	110	MHz	
Output Frequency	F_0	2	–	110	MHz	The actual output frequency of the CLK pin is selected by the FS (frequency select pin) to be either F_0 or F_1.
	F_1	1	–	55	MHz	
Frequency Stability	F_stab	-20	–	+20	PPM	Inclusive of: Initial stability, operating temperature, rated power, supply voltage change, load change, shock and vibration
		-25	–	+25	PPM	
		-30	–	+30	PPM	**± 20 PPM available in extended commercial temperature only**
		-50	–	+50	PPM	
Aging	Ag	-1.0	–	1.0	PPM	1st year at 25°C
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage	Vdd	1.71	1.8	1.89	V	
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.97	3.3	3.63	V	
Current Consumption	Idd	–	3.7	4.1	mA	No load condition, f = 20 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V
		–	3.2	3.5	mA	No load condition, f = 20 MHz, Vdd = 1.8 V
Duty Cycle	DC	45	50	55	%	All Vdds. f <= 75 MHz
		40	50	60	%	All Vdds. f > 75 MHz
Rise/Fall Time	Tr, Tf	–	1	2	ns	20% - 80% Vdd=2.5 V, 2.8 V or 3.3 V, 15 pf load
		-	1.3	2.5	ns	20% - 80% Vdd=1.8 V, 15 pf load
Output Voltage High	VOH	90%	–	–	Vdd	IOH = -4 mA (Vdd = 3.3 V) IOH = -3 mA (Vdd = 2.8 V and Vdd = 2.5 V) IOH = -2 mA (Vdd = 1.8 V)
Output Voltage Low	VOL	–	–	10%	Vdd	IOL = 4 mA (Vdd = 3.3 V) IOL = 3 mA (Vdd = 2.8 V and Vdd = 2.5 V) IOL = 2 mA (Vdd = 1.8 V)
Output Load	Ld	–	–	15	pF	At maximum frequency and supply voltage. Contact SiTime for higher output load option.
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE or $\overline{ST}$
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE or $\overline{ST}$
Startup Time	T_osc	–	–	10	ms	Measured from the time Vdd reaches its rated minimum value
Resume Time	T_resume	–	3.0	4	ms	Measured from the time ST pin crosses 50% threshold
RMS Period Jitter	T_jitt	–	–	4.0	ps	f = 75 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V
		–	–	6.5	ps	f = 75 MHz, Vdd = 1.8 V
RMS Phase Jitter (random)	T_phj	–	0.6	–	ps	f = 75 MHz, Integration bandwidth = 900 kHz to 7.5 MHz, VDD = 2.5 V, 2.8 V, or 3.3 V
		–	0.8	–	ps	f = 75 MHz, Integration bandwidth = 900 kHz to 7.5 MHz, VDD = 1.8 V

■ Specifications (Cont.)

Pin Description Tables

Pin #1 Functionality
FS
H or Open[1]: output frequency F_0
L: output frequency F_1

Pin Map	
Pin	Connection
1	FS
2	GND
3	CLK
4	VDD

Absolute Maximum Ratings

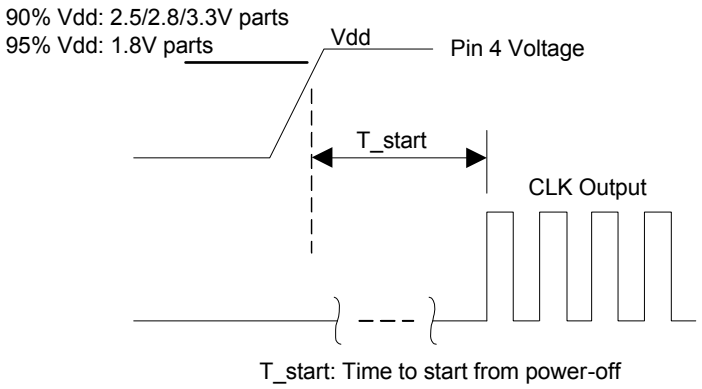
Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge	–	6000	V
Theta JA (with copper plane on VDD and GND)	–	75	°C/W
Theta JC (with PCB traces of 0.010 inch to all pins)	–	24	°C/W
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Number of Program Writes	–	1	NA
Program Retention over -40 to 125°C, Process, VDD (0 to 3.65 V)	1,000+	–	years

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensibility Level	MSL1 @ 260°C

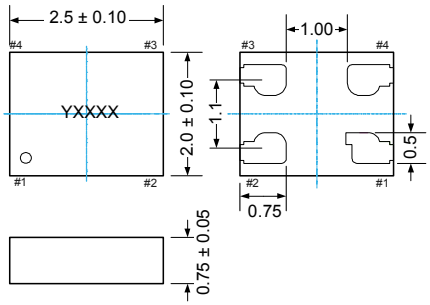
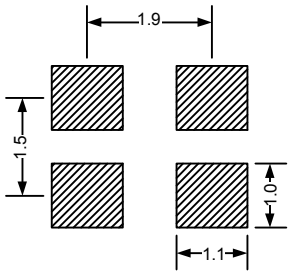
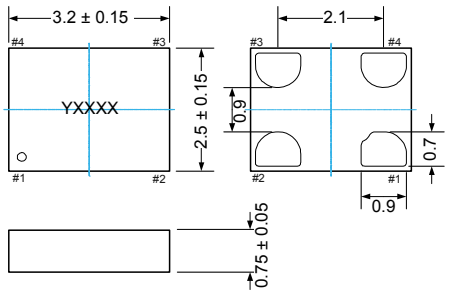
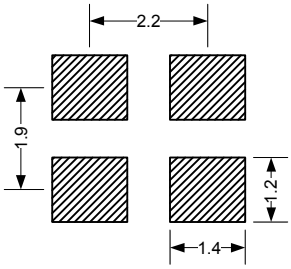
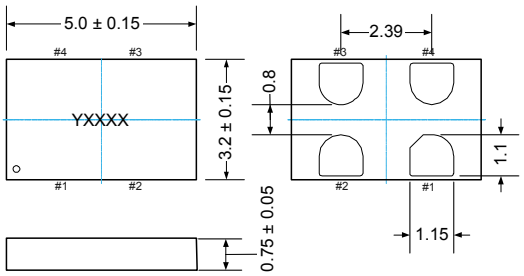
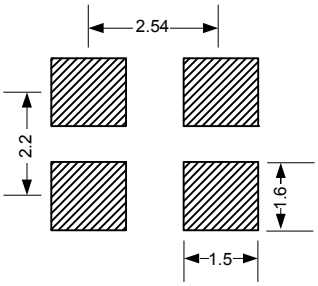
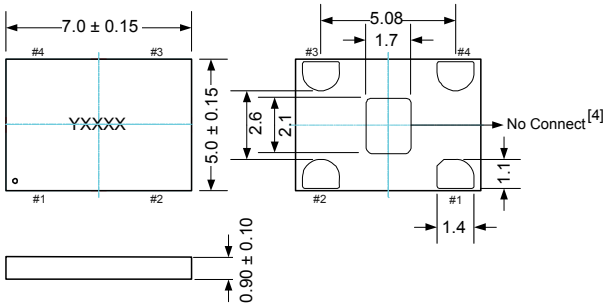
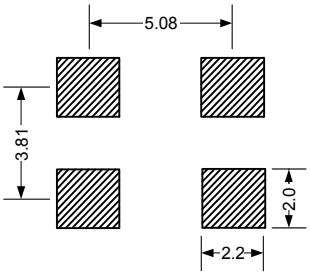
Startup Timing Diagram



T_start: Time to start from power-off

Note:
1. In 1.8 V mode, a resistor of <100 kΩ between OE pin and VDD is recommended.

Dimensions and Land Patterns

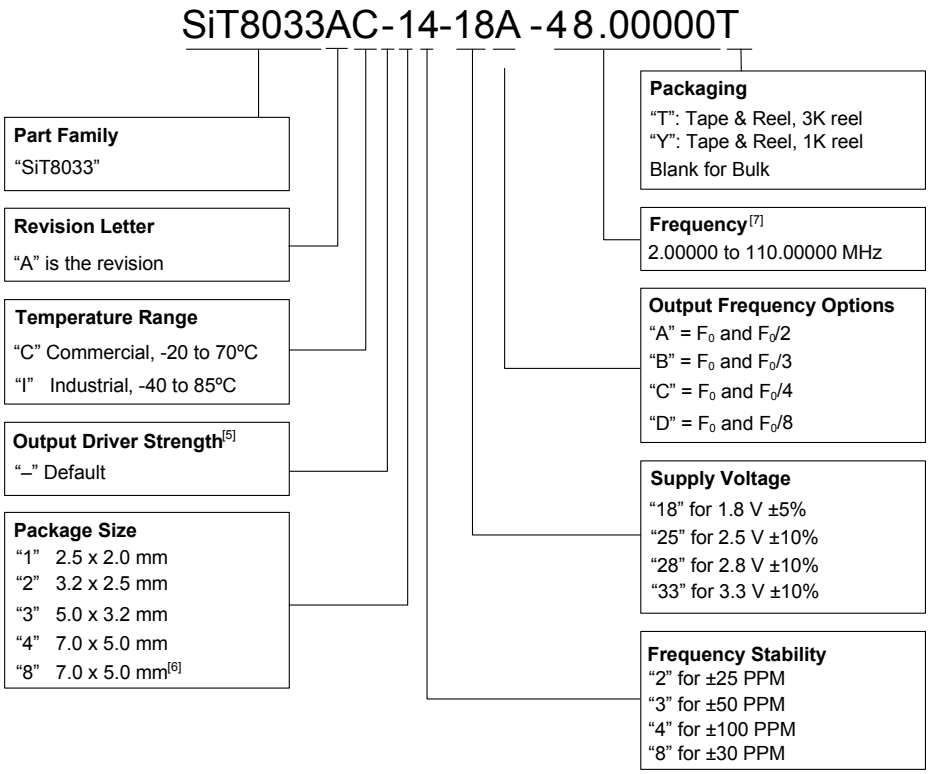
Package Size – Dimensions (Unit: mm)[2]	Recommended Land Pattern (Unit: mm)[3]
2.5 x 2.0 x 0.75 mm	
	
3.2 x 2.5 x 0.75 mm	
	
5.0 x 3.2 x 0.75 mm	
	
7.0 x 5.0 x 0.90 mm	
	

Notes:

2. Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
3. A capacitor of value 0.1 µF between Vdd and GND is recommended.
4. The 7050 package with part number designation "-8" has NO center pad.

■ Part No. Guide - How to Order

The Part No. Guide is for reference only. For real-time customization and exact part number, use the SiTime Part Number Generator.



Notes:
5. Contact SiTime for different drive strength options for driving higher loads or reducing EMI.
6. Without Center Pad.
7. Frequency is for F_0 (see table below for mimum output frequencies).

Frequency Stability vs. Temperature Range Options

Frequency Stability (PPM)	Temperature Range	Supply Voltage			
		1.8 V	2.5 V	2.8 V	3.3 V
±20	C (-20 to +70°C)	✓	✓	✓	✓
	I (-40 to +85°C)	–	–	–	–
±25	C (-20 to +70°C) I (-40 to +85°C)	✓	✓	✓	✓
±30	C (-20 to +70°C) I (-40 to +85°C)	✓	✓	✓	✓
±50	C (-20 to +70°C) I (-40 to +85°C)	✓	✓	✓	✓

Frequency Select Options vs. Mimimum Output Frequency

Output Frequency Option	Minimum Frequency (F_0)
A = F_0 and $F_0/2$	2 MHz
B = F_0 and $F_0/3$	3 MHz
C = F_0 and $F_0/4$	4 MHz
D = F_0 and $F_0/8$	8 MHz

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