ANALOG DEVICES

Evaluation Board User Guide
UG-057

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Evaluating the ADP1872/ADP1873 PWM Buck Controllers

FEATURES

Wide power input voltage (V_{IN}): 2.75 V to 20 V
Bias supply voltage (V_{DD}) range: 2.75 V to 5.5 V
Available in 1.8 V and 3.3 V fixed-output voltages
Available in 300 kHz, 600 kHz, and 1.0 MHz switching frequency options
Available in power saving mode (PSM) for light loads (ADP1873 only)
Starts into a precharged or preloaded output

APPLICATIONS

Perform basic evaluation board operations
Evaluate IC and application board performance

GENERAL DESCRIPTION

This document describes the evaluation board hardware for the ADP1872/ADP1873 PWM buck controllers. The evaluation boards can be used to evaluate the ADP1872 or ADP1873 and application circuits using these ICs without requiring any additional software.

The ADP1872/ADP1873 are versatile current-mode, synchronous step-down controllers that provide superior transient response, optimal stability, and current limit protection by using a constant on-time, pseudo-fixed frequency with a programmable current-sense gain, current-control scheme. The ADP1873 is the power saving mode (PSM) version of the device and is capable of pulse skipping to maintain output regulation while achieving improved system efficiency at light loads (see the ADP1872/ADP1873 data sheet for more information). Both devices are available in a small, 10-lead MSOP package and can operate over the −40°C to +125°C temperature range.

The ADP1872/ADP1873 evaluation boards employ a power input voltage (V_{IN}) that ranges between 2.75 V and 20 V and a bias supply voltage (V_{DD}) that ranges between 2.75 V and 5.5 V. Both inputs can be tied together for application input voltage conditions equal to or less than 5.5 V. The evaluation boards are available in two fixed-output voltage options (V_{OUT} = 1.8 V and V_{OUT} = 3.3 V), as well as in a 300 kHz, 600 kHz, or 1 MHz switching frequency (test trimmed in production). The ADP1872/ADP1873 evaluation boards offer an output accuracy of 2% over the full temperature range and provide a high input voltage (V_{IN} ± 10%) and a full-scale load current up to 15 A.

TYPICAL APPLICATIONS CIRCUIT

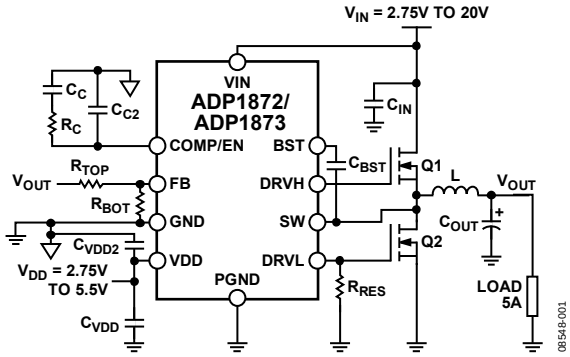

Figure 1.

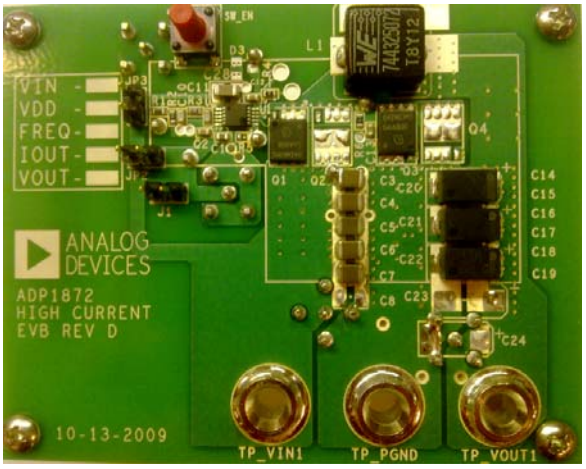

Figure 2. ADP1872 Evaluation Board Configured for 300 kHz Switching Frequency Operation

The ADP1872/ADP1873 data sheet provides more information, including details about how to modify the evaluation board while maintaining system stability throughout the entire load current range and, therefore, should be consulted in conjunction with this user guide when using the evaluation boards.

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REVISION HISTORY

3/10—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

Upon receipt of the ADP1872/ADP1873 evaluation board, the following criteria have already been determined:

- The IC is either the ADP1872 (forced pulse-width modulation [PWM]) or the ADP1873 (power saving mode [PSM]).
- The switching frequency is 300 kHz, 600 kHz, or 1 MHz.

SETTING UP THE EVALUATION BOARD

Before powering up the system, set up the evaluation board as follows to ensure that all passive and active components are properly soldered to the evaluation board:

1. Ensure that the Headers JP2 and J1 connections are correct for a given application (see Table 1 and the Headers JP2 and J1 section).
2. Ensure that the main power supply (V_{IN}) is off but set to 0 V, and then connect the main power supply to the evaluation board, connecting the positive terminal to TP_VIN1 and the negative terminal to TP_PGND.
3. Optionally, place a current meter in series with the main power supply to monitor the input current.
4. Ensure that the low input voltage supply (V_{DD}) is off but set to 0 V, and then connect the low input voltage supply to the evaluation board, connecting the positive terminal to J1 and the negative terminal to TP_PGND.
5. Ensure that the electronic load is turned off, and then connect the load to the evaluation board, connecting the positive terminal to TP_VOUT1 and the negative terminal to TP_PGND.
6. Optionally, connect a power resistor of the appropriate value for your application across the TP_VOUT1 and TP_PGND terminals of the evaluation board.
7. Optionally, to continually monitor V_{IN}, V_{DD}, and V_{OUT}, solder SMB jacks to each of the following measuring points: VIN1, VOUT1, and VREG1 (see Figure 35).

Table 1. Header Connections

Header	Input Voltage (V)	Description of Connection
J1	≤5.5	Floating (no jumper), single input configuration.
	>5.5	Connect to V_{DD} (dual input configuration), and, optionally, add a voltmeter across J1 and TP_PGND to monitor the low input voltage.
JP2	≤5.5	Jumper between V_{IN} and V_{DD} (single input configuration).
	>5.5	Open (no jumper), dual input configuration.
JP3	N/A	Jumper at all times.

Headers JP2 and J1

When the power input voltage is greater than 5.5 V, the device is in dual input configuration. If this configuration is chosen, ensure that Header JP2 is open (no jumper), and connect J1 to V_{DD}. Optionally, you can also add a voltmeter across J1 and TP_PGND to monitor the low input voltage.

If the power input voltage is less than or equal to 5.5 V, the device is in single input configuration. In this case, a jumper can be placed on Header JP2 that connects V_{IN} to V_{DD}. If a jumper is used in this way, leave Header J1 floating (no jumper), and ensure that V_{IN} does not exceed 5.5 V.

Header JP3

Always put a jumper on Header JP3 to connect the high voltage input to Pin 1 (VIN) of the IC.

High Input Voltage Power Source (V_{IN})

Ensure that the main power supply equipment is turned off but set to 0 V before connecting the main power supply to the evaluation board. Place a current meter in series with this power supply to monitor the input current. Connect the positive terminal (+) of the power supply to the TP_VIN1 terminal of the evaluation board. Connect the negative terminal of the power supply (−) to the TP_PGND terminal of the evaluation board.

Low Input Voltage Supply for Bias (V_{DD})

Set the low input voltage supply to 0 V and make sure that it is turned off before connecting the positive terminal (+) to Jumper J1 of the evaluation board. Connect the negative terminal (−) to the TP_PGND terminal of the evaluation board.

Output Terminal

The output terminal (TP_VOUT1) of the ADP1872/ADP1873 evaluation board is equipped with a banana terminal plug similar to TP_VIN1 and TP_PGND. The evaluation board is designed to withstand load immediately upon power-up, but may be damaged if the load is not properly connected to TP_VOUT1. Ensure that the electronic load is turned off prior to connecting the positive terminal (+) and negative terminal (−) to the V_{OUT} and TP_PGND terminals of the evaluation board, respectively. If a power resistor is used, connect this device across the TP_VOUT1 and TP_PGND terminals of the evaluation board.

Ensure that proper current values for your application are programmed on the electronic load prior to activation and, if applicable, that the correct power resistor value for your application is in place before powering up the evaluation board.

DC Voltmeter on V_{IN}, V_{DD}, and V_{OUT}

For more accurate dc measurements of V_{IN}, V_{DD}, and V_{OUT}, add a dedicated voltmeter for each of these voltage nodes (resources permitting) to continually monitor V_{IN}, V_{OUT}, and V_{DD}. This can be done by placing an SMB jack on VIN1, VOUT2, VREG1 (see Figure 35).

Placeholders for SMB jacks are integrated into each evaluation board to facilitate such connections. Therefore, to accurately measure V_{IN}, connect the voltmeter's positive terminal (+) to the node where the positive terminal of the high voltage input capacitors (C3 to C8) and the drain of Q1/Q2 meet, and connect the voltmeter's negative terminal (−) to the node where the negative terminal of the input capacitors and the source terminal of Q3 meet. These SMB terminals are optimally placed to minimize unnecessary voltage drops that may otherwise produce inaccurate VIN dc measurements.

Similarly, for output voltage (V_{OUT}) dc measurements, a placeholder for an SMB terminal is positioned directly across the positive and negative terminals of the output capacitor that is farthest from the inductor terminal and source of Q3. For accurate low input voltage (V_{DD}) dc measurements, an SMB terminal footprint is positioned as close as possible across C1, which is laid out near the VDD pin (Pin 5) and the PGND pin (Pin 7) of the ADP1872/ADP1873.

POWERING UP AND POWERING DOWN THE EVALUATION BOARD

After completing the procedure described in the Setting Up the Evaluation Board section, power up the evaluation board as follows:

1. Apply power to the VDD pin.
2. Apply power to the VIN pin.
3. Slowly increase the V_{DD} supply while monitoring the current meter until V_{DD} is equal to 5 V.
   Because V_{IN} is 0 V, I_{DD} should jump between 120 µA (when approaching the UVLO threshold of 2.65 V) to less than 1 mA until V_{DD} is equal to 5 V. Do not exceed 5.5 V on V_{DD}. No output (V_{OUT}) regulation is expected yet because V_{IN} is 0 V.
4. Slowly increase V_{IN} up to 12 V.
   When V_{IN} is increased, V_{OUT} begins regulating to the desired voltage setpoint (via the V_{OUT} dedicated voltmeter). Continue to increase V_{IN} up to 12 V. Do not exceed 20 V on V_{IN}. Output voltage regulation should occur regardless of whether there is a load connected at the output.
5. After the output voltage is in regulation with the desired input voltage, increase the electronic load to the desired value.

To power down the evaluation board,

1. Power down V_{IN}.
2. Power down V_{DD}.

ENABLING AND DISABLING THE ADP1872/ADP1873

The ADP1872/ADP1873 evaluation board has a placeholder for a switch (normally open) for the COMP/EN pin to allow you to enable (open) and disable (closed) the ADP1872/ADP1873 on the evaluation board. When closed, the switch shorts this pin to ground, disabling the ADP1872/ADP1873. When the switch is subsequently opened (released), the error amplifier brings the voltage on this pin above the enable threshold of 285 mV, thus enabling the IC, which causes the output voltage to regulate.

EVALUATING THE PERFORMANCE OF THE ADP1872/ADP1873

Verifying the Switching Waveform

To verify the switching waveform,

1. Ensure that the oscilloscope, probe tips, and ground loop clip are in good working condition; that the probe tips have been calibrated per the manufacturer's instructions and are clear of debris and dirt; and that the ground loops do not have any breaks or peels.
2. Set the operating mode of the respective oscilloscope to **DC Coupling** in the oscilloscope's **Channel** menu.
3. Set the bandwidth to its maximum value (≥150 MHz).
4. Set the vertical scale to 5 V per division and the timescale (x-axis) to $1/(2 \times f_{SW})$ per division, where f_{SW} is the switching frequency of the evaluation board.
5. Securely attach the ground loop clip onto the TP_PGND terminal of the evaluation board. Ideally, the loop should be as close as possible to the negative terminal of the high input voltage capacitors (C3 to C8) and to the source of MOSFET Q1.
6. Land or securely attach the probe tip to the drain of Q1.
7. Observe the subsequent switching waveform and jitter.

The resultant switching waveform should be between 0 V and the value of V_{IN} (that is, 12 V), and the jitter should be less than or equal to 100 ns.

Observing the Output Voltage Ripple

To observe the output voltage ripple,

1. Set the operating mode of the respective oscilloscope to **AC Coupling** in the oscilloscope's **Channel** menu.
2. Set the vertical scale to 100 mV per division and the timescale to $1/(2 \times f_{SW})$.
3. Securely attach the ground loop clip onto the TP_PGND terminal of the evaluation board. Ideally, the loop should be as close as possible to the negative terminal (−) of the farthest output capacitor from the inductor terminal, and the probe tip should touch the positive terminal (+) of the same output capacitor.
4. Observe the output voltage ripple.

Evaluating the Inductor Current Waveform

To evaluate the inductor current waveform,

1. Calibrate the current probe per the manufacturer's instructions.
2. Power up the system (see the Powering Up and Powering Down the Evaluation Board section).
3. Solder a 3 inch wire loop (from 10 gauge to 14 gauge) between the source of Q1 and the inductor terminal. The current probe has a clamping mechanism and can clamp onto this wire to measure the current traveling through the wire.

4. Ensure that the current direction is toward the output voltage (TP_VOUT1) and that the clamp of the current probe is in the closed, or locked, position.
5. Set the vertical scale to one-third of the total load current that the converter is designed to deliver.
6. Set the timescale similar to how the switching and output ripple waveforms were set.
7. Observe the inductor current waveform.

Obtaining Efficiency Measurements

To obtain more accurate efficiency measurements,

1. Power down the device.
2. Remove the 3 inch wire loop between the source of Q1 and the inductor terminal.
3. Power up the device.
4. Record the current and voltage readings.

Efficiency is calculated based on the measurements made between the output and the input of the converter:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$$

where:
V_{OUT} is the dc voltage readout by the voltmeter that is connected to the SMB terminal of the evaluation board or by the voltmeter that is connected across the output capacitor that is located farthest from the inductor terminal.
I_{OUT} is the digital readout produced by the electronic load equipment.
V_{IN} is the dc voltage readout by the voltmeter.
I_{IN} is the current readout from the current meter in series between the high input voltage supply equipment and the TP_VIN1 terminal of the evaluation board.

Assessing Line Regulation

To assess the line regulation,

1. Vary the high input voltage.
2. Record the resultant changes on the dc level of the output voltage (V_{OUT}).

Examining Load Regulation

To examine the load regulation,

1. Vary the load current through electronic load adjustments.
2. Record the resultant changes on the dc level of the output voltage (V_{OUT}).

Observing Transient Response

To observe the transient response,

1. Power up the system (see the Powering Up and Powering Down the Evaluation Board section).
2. Solder a 3 inch wire loop (from 10 gauge to 14 gauge) between the source of Q1 and the inductor terminal.
3. Record instances where the output transient is out of phase with the load. Such occurrences are caused by sudden changes in the output load current and can be recorded by capturing the inductor ripple current waveform and the output voltage ac transient using the single acquisition feature of the oscilloscope.

Evaluating Short-Circuit Protection

To evaluate the self-protection scheme of the ADP1872/ADP1873 during output short-circuit events,

1. Achieve steady state regulation.
2. Short the voltage output (TP_VOUT1) to TP_PGND.

The system then enters hiccup mode and remains in this mode until the violation disappears (see the ADP1872/ADP1873 data sheet for more details).

MODIFYING THE EVALUATION BOARD

For any given ADP1872/ADP1873 evaluation board, an ADP1872 or ADP1873 IC can be used interchangeably as long as the pre-trimmed frequency setpoint is the same for both ICs.

To maintain system stability throughout the entire load current range, one component (passive or active) cannot be modified without modifying the rest. Refer to the ADP1872/ADP1873 data sheet for information about how each of the following elements can be adjusted, keeping in mind that any change affects the entire system:

- Feedback resistor divider
- Inductor
- Output capacitor
- Compensation network
  - Output filter impedance (Z_{FILT})
  - Error amplifier output impedance (Z_{COMP})
  - Error amplifier gain (G_M)
  - Current-sense loop gain (G_{CS})
  - Programmable current-sense gain (A_{CS})
  - Valley current limit setting
  - Crossover frequency

TYPICAL PERFORMANCE CHARACTERISTICS

For the most up-to-date typical performance characteristics, see the ADP1872/ADP1873 data sheet.

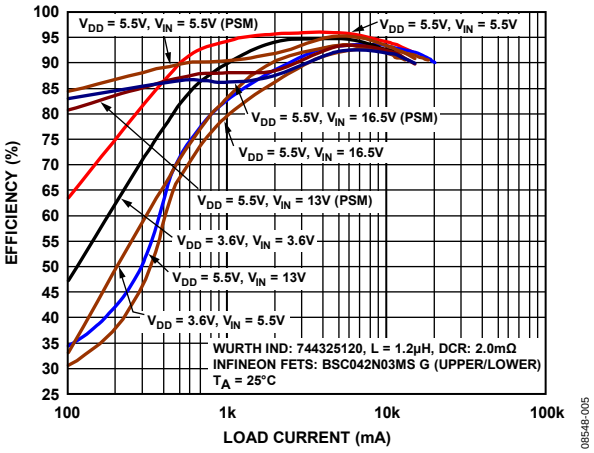

Figure 3. Efficiency—300 kHz, V_{OUT} = 1.8 V

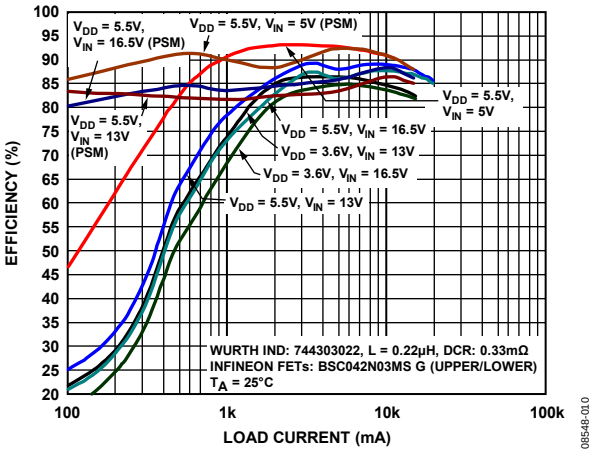

Figure 4. Efficiency—1 MHz, V_{OUT} = 1.8 V

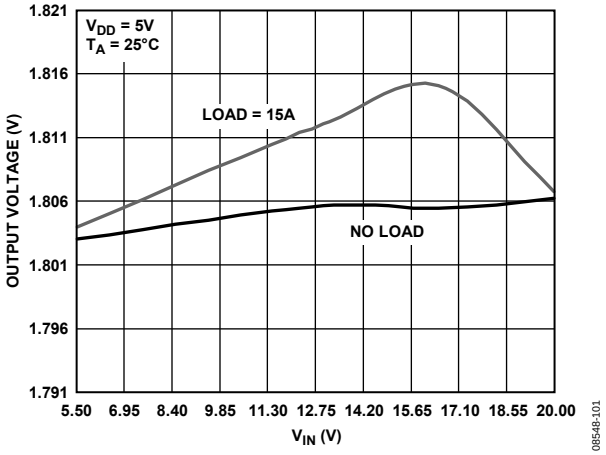

Figure 5. Line Regulation Plot for f_{SW} = 300 kHz, V_{OUT} = 1.8 V

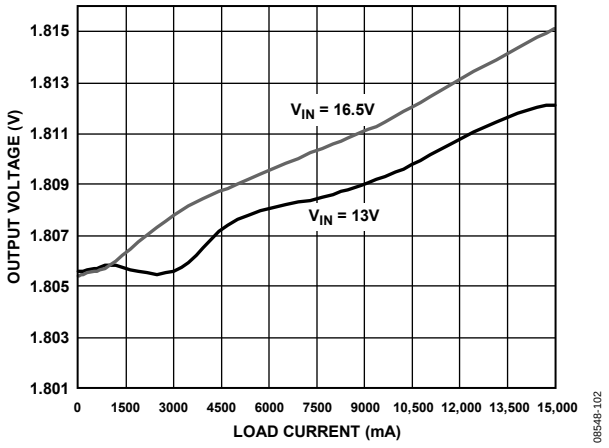

Figure 6. Load Regulation Plot for f_{SW} = 300 kHz, V_{OUT} = 1.8 V

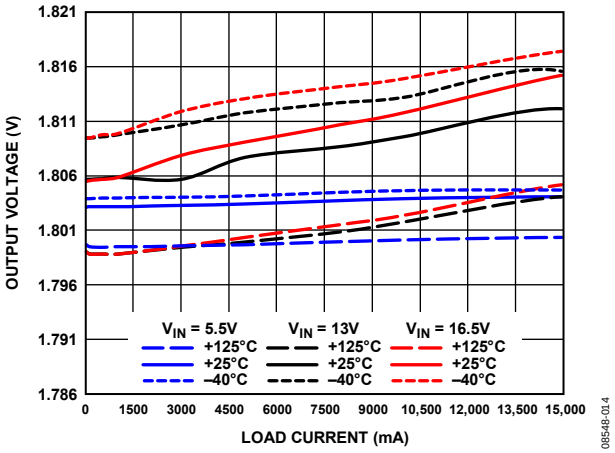

Figure 7. Output Voltage Accuracy—300 kHz, V_{OUT} = 1.8 V

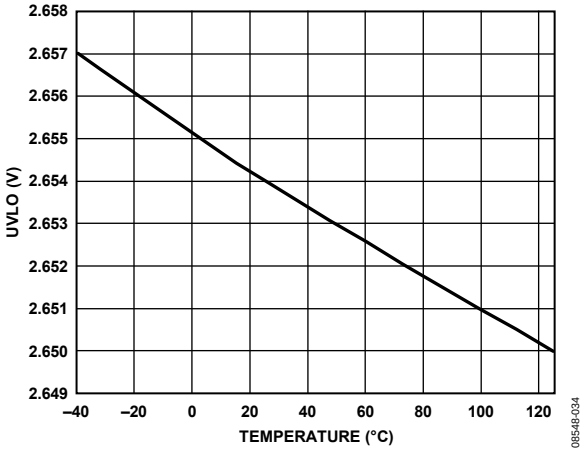

Figure 8. UVLO vs. Temperature

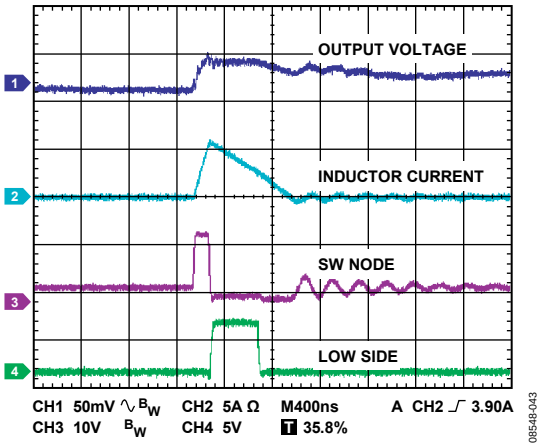

Figure 9. Power Saving Mode (PSM) Operational Waveform, 100 mA

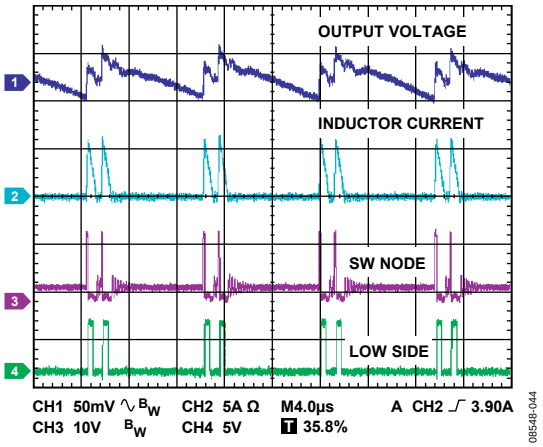

Figure 10. PSM Waveform at Light Load, 500 mA

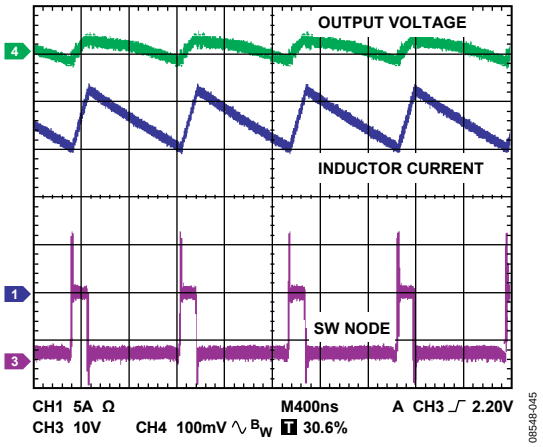

Figure 11. CCM Operation at Heavy Load, 18 A
(See Figure 28 for Application Circuit)

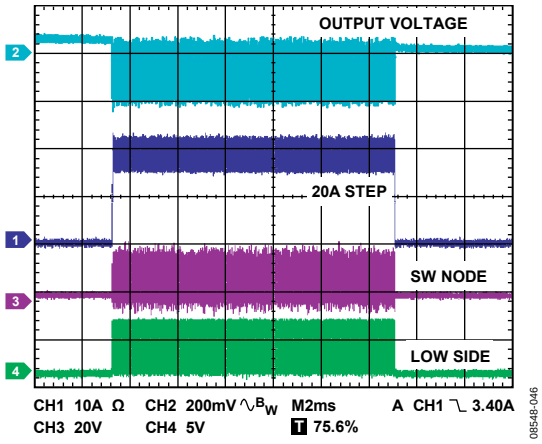

Figure 12. Load Transient Step—PSM Enabled, 20 A
(See Figure 28 for Application Circuit)

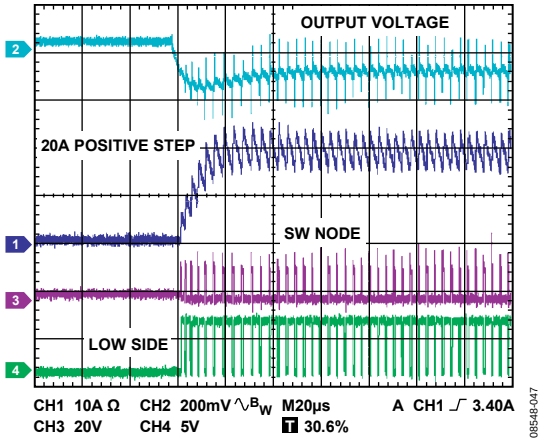

Figure 13. Positive Step During Heavy Load Transient Behavior—PSM Enabled, 20 A, V_{OUT} = 1.8 V (See Figure 28 for Application Circuit)

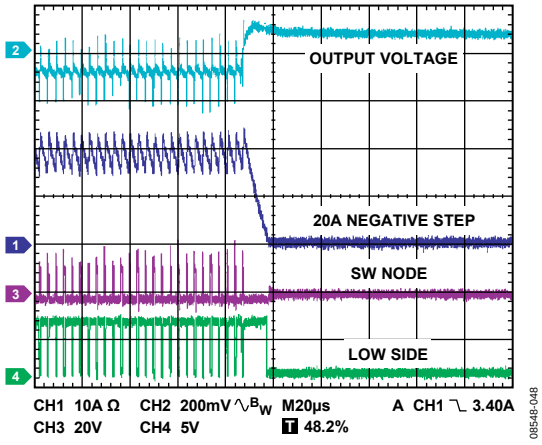

Figure 14. Negative Step During Heavy Load Transient Behavior—PSM Enabled, 20 A (See Figure 28 for Application Circuit)

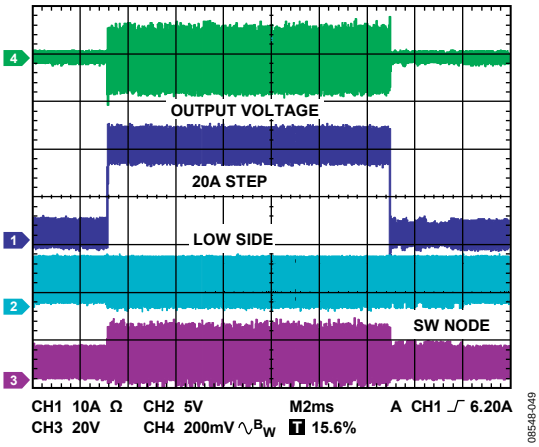

Figure 15. Load Transient Step—Forced PWM at Light Load, 20 A (See Figure 28 for Application Circuit)

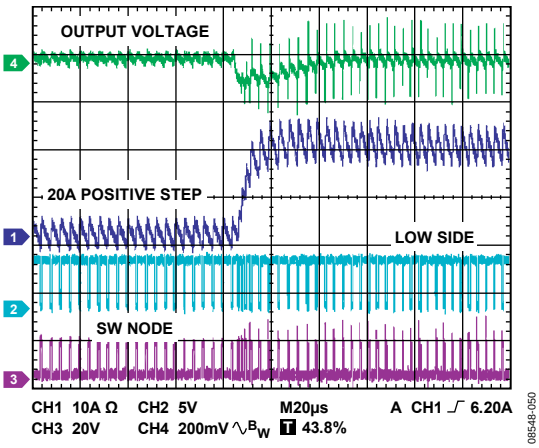

Figure 16. Positive Step During Heavy Load Transient Behavior—Forced PWM at Light Load, 20 A, V_{OUT} = 1.8 V (See Figure 28 for Application Circuit)

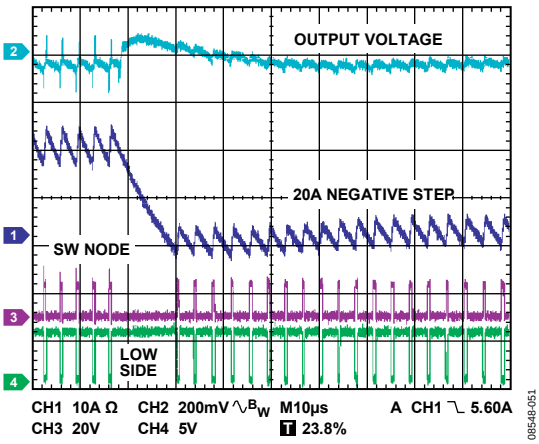

Figure 17. Negative Step During Heavy Load Transient Behavior—Forced PWM at Light Load, 20 A (See Figure 28 for Application Circuit)

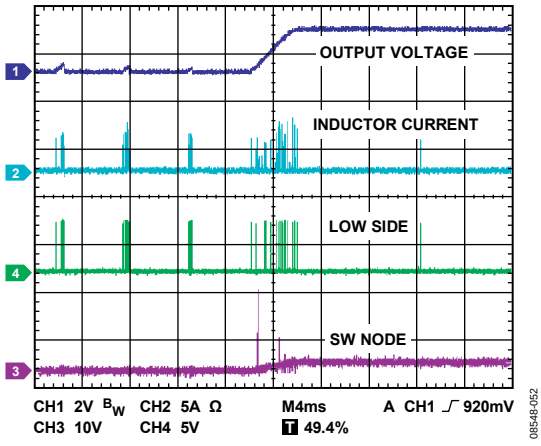

Figure 18. Output Short-Circuit Behavior Leading to Hiccup Mode

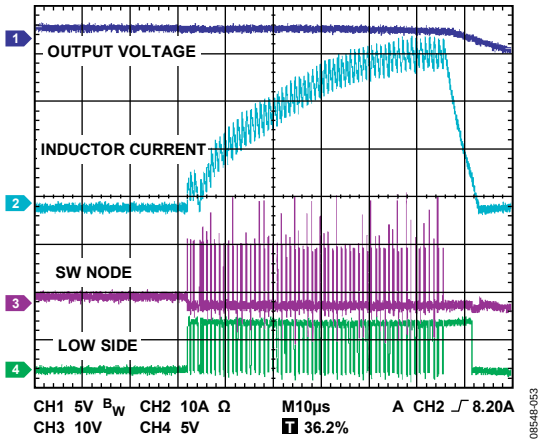

Figure 19. Magnified Waveform During Hiccup Mode

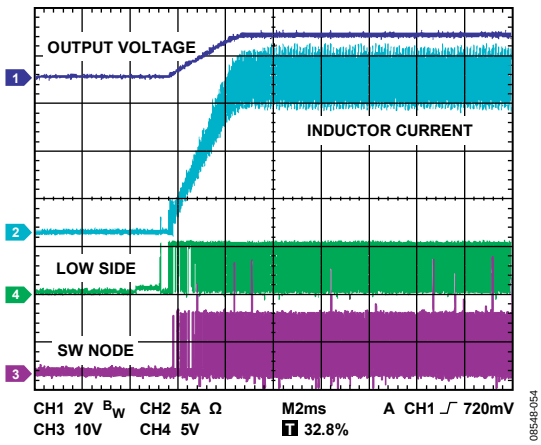

Figure 20. Start-Up Behavior at Heavy Load, 18 A, 300 kHz (See Figure 28 for Application Circuit)

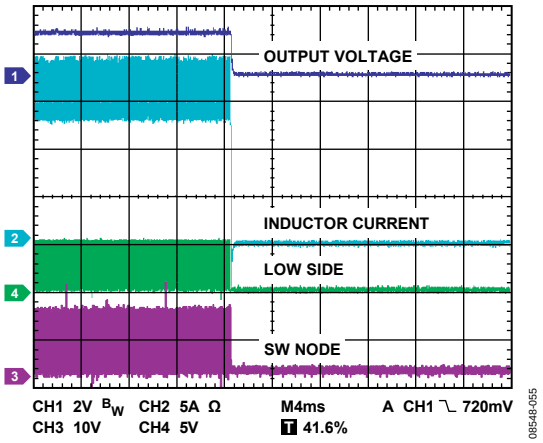

Figure 21. Power-Down Waveform During Heavy Load

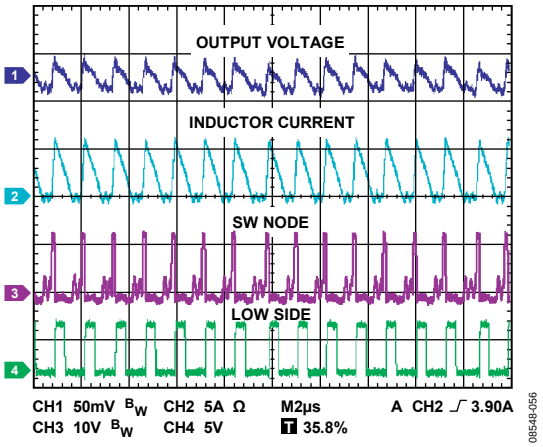

Figure 22. Output Voltage Ripple Waveform During PSM Operation at Light Load, 2 A

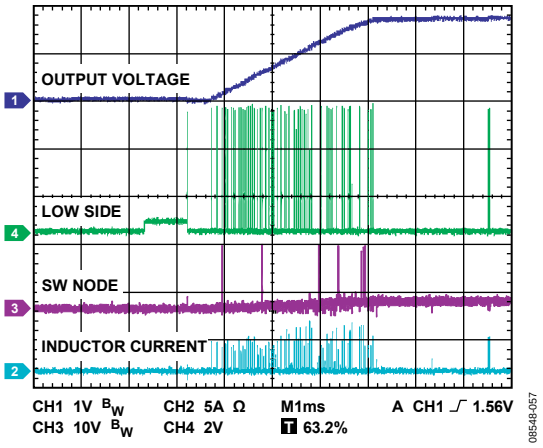

Figure 23. Soft Start and RES Detect Waveform

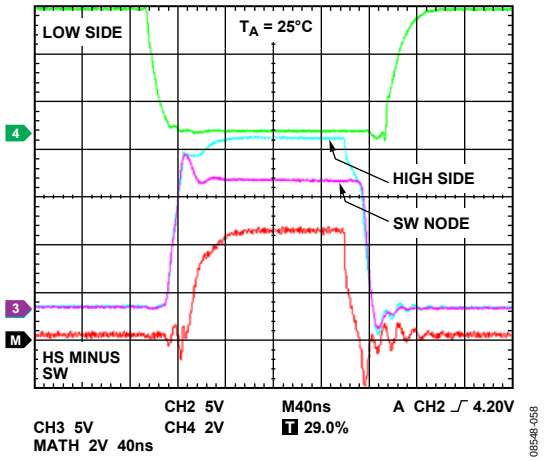

Figure 24. Output Drivers and SW Node Waveforms

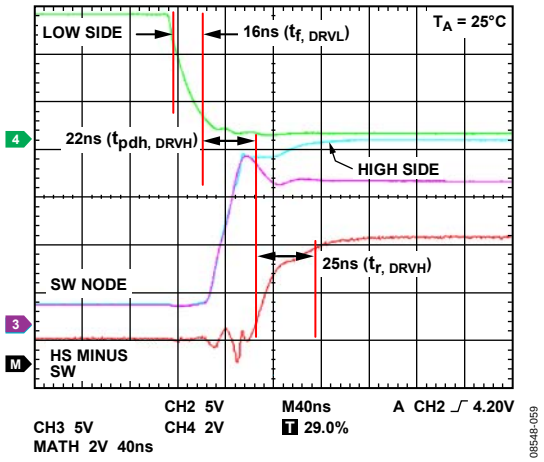

Figure 25. Upper-Side Driver Rising and Lower-Side Falling Edge Waveforms, C_{IN} = 4.3 nF (Upper-/Lower-Side MOSFET), Q_{TOTAL} = 27 nC (V_{GS} = 4.4 V (Q1), V_{GS} = 5 V (Q3)

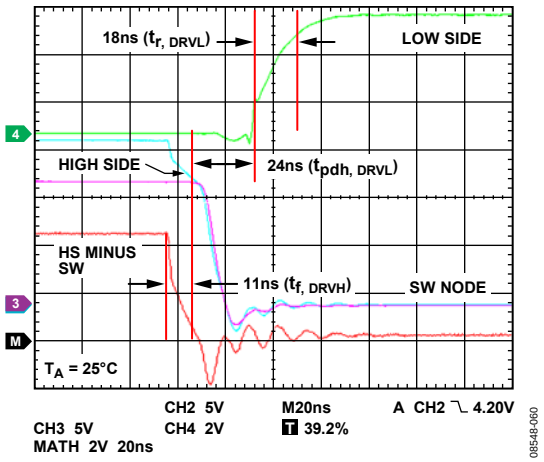

Figure 26. Upper-Side Driver Falling and Lower-Side Rising Edge Waveforms, C_{IN} = 4.3 nF (Upper-/Lower-Side MOSFET), Q_{TOTAL} = 27 nC (V_{GS} = 4.4 V (Q1), V_{GS} = 5 V (Q3)

TYPICAL APPLICATION CIRCUITS

DUAL-INPUT, 300 kHz HIGH CURRENT APPLICATION CIRCUIT

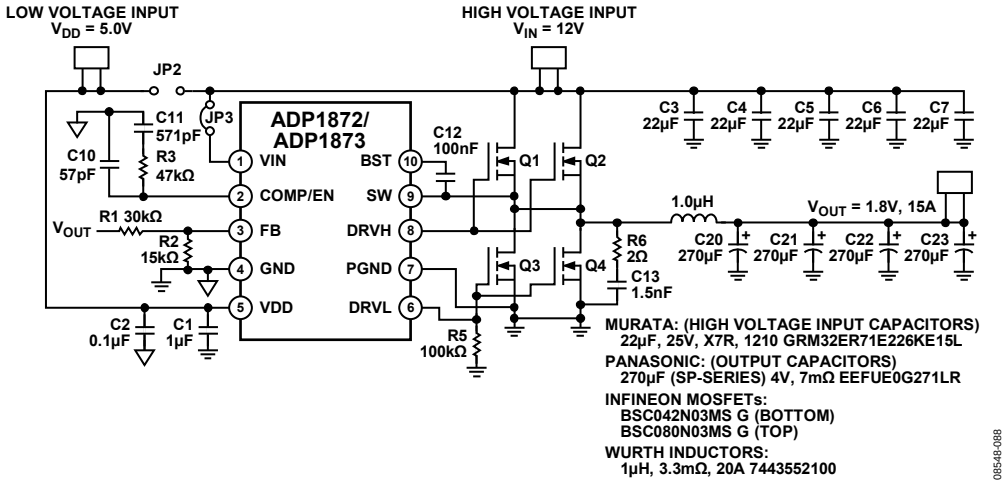

Figure 27. Application Circuit for 12 V Input, 1.8 V Output, 15 A, 300 kHz (Q2/Q4 No Connect)

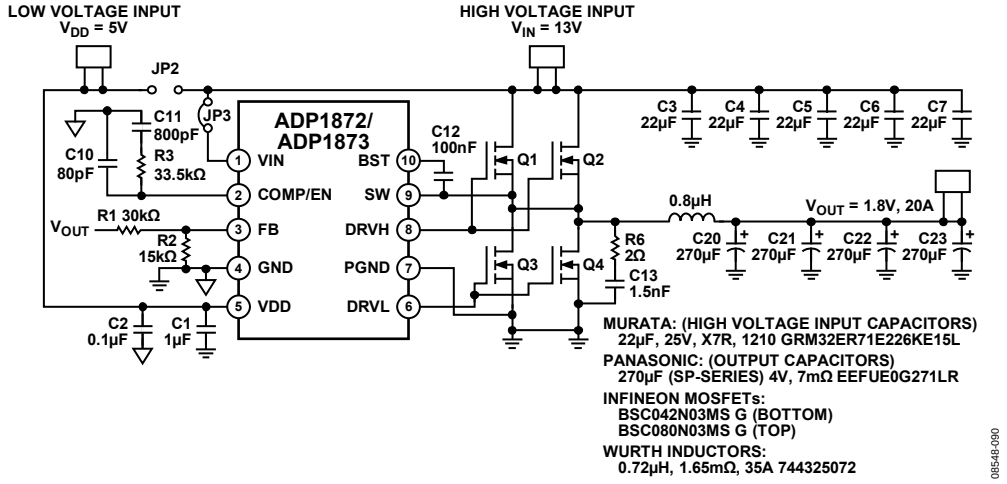

Figure 28. Application Circuit for 13 V Input, 1.8 V Output, 20 A, 300 kHz (Q2/Q4 No Connect)

SINGLE-INPUT, 600 kHz APPLICATION CIRCUIT

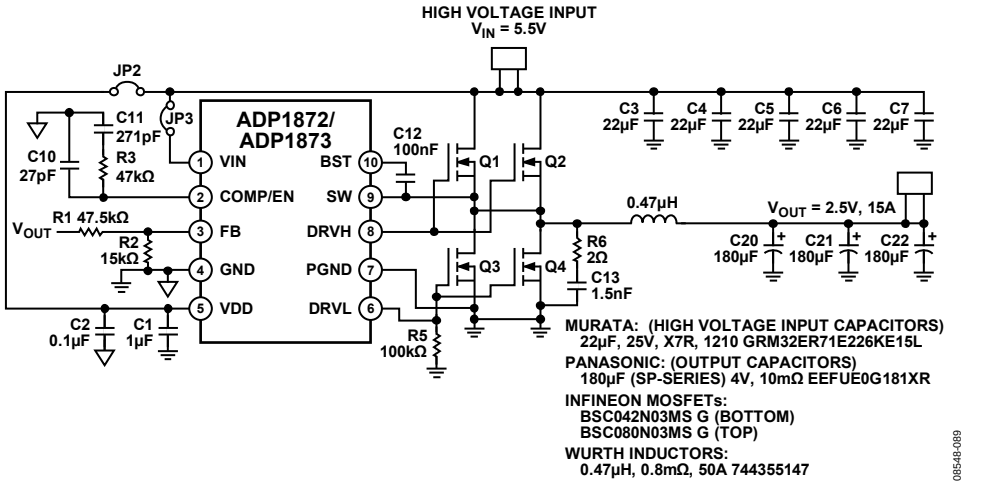

Figure 29. Application Circuit for 5.5 V Input, 2.5 V Output, 15 A, 600 kHz (Q2/Q4 No Connect)

EVALUATION BOARD SCHEMATICS AND LAYOUT

This section provides the schematics for the 1.8 V output, 300 kHz, 14 A application circuit and the 3.3 V output, 300 kHz, 14 A application circuit. For other application circuits, see the ADP1872/ADP1873 data sheet for the recommended values for the external components.

1.8 V OUTPUT, 300 kHz, 14 A APPLICATION CIRCUIT

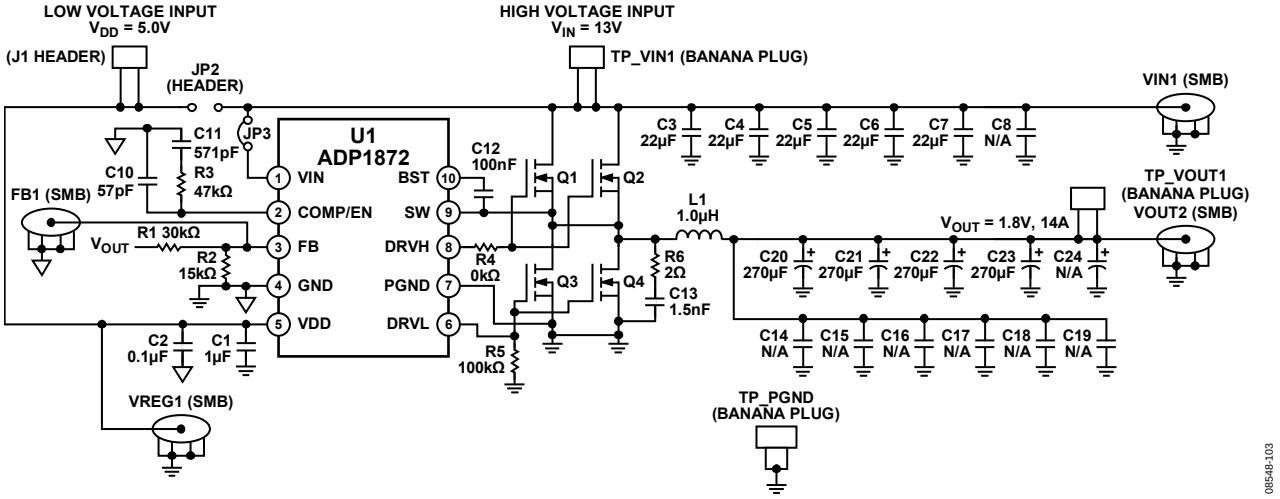

Figure 30. 1.8 V Output, 300 kHz, 14 A Application Circuit

3.3 V OUTPUT, 300 kHz, 14 A APPLICATION CIRCUIT

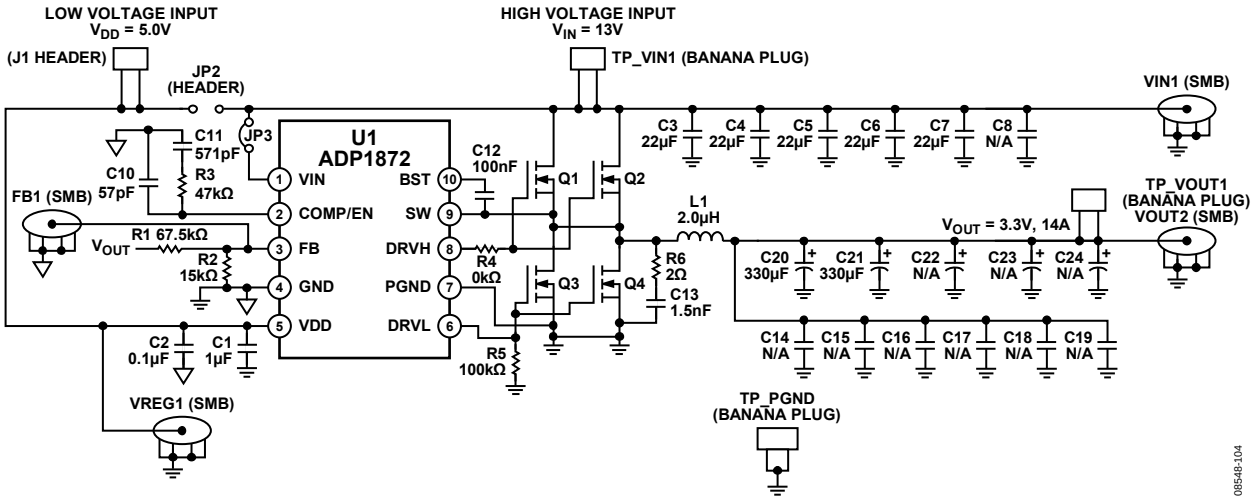

Figure 31. 3.3 V Output, 300 kHz, 14 A Application Circuit

LAYER 1

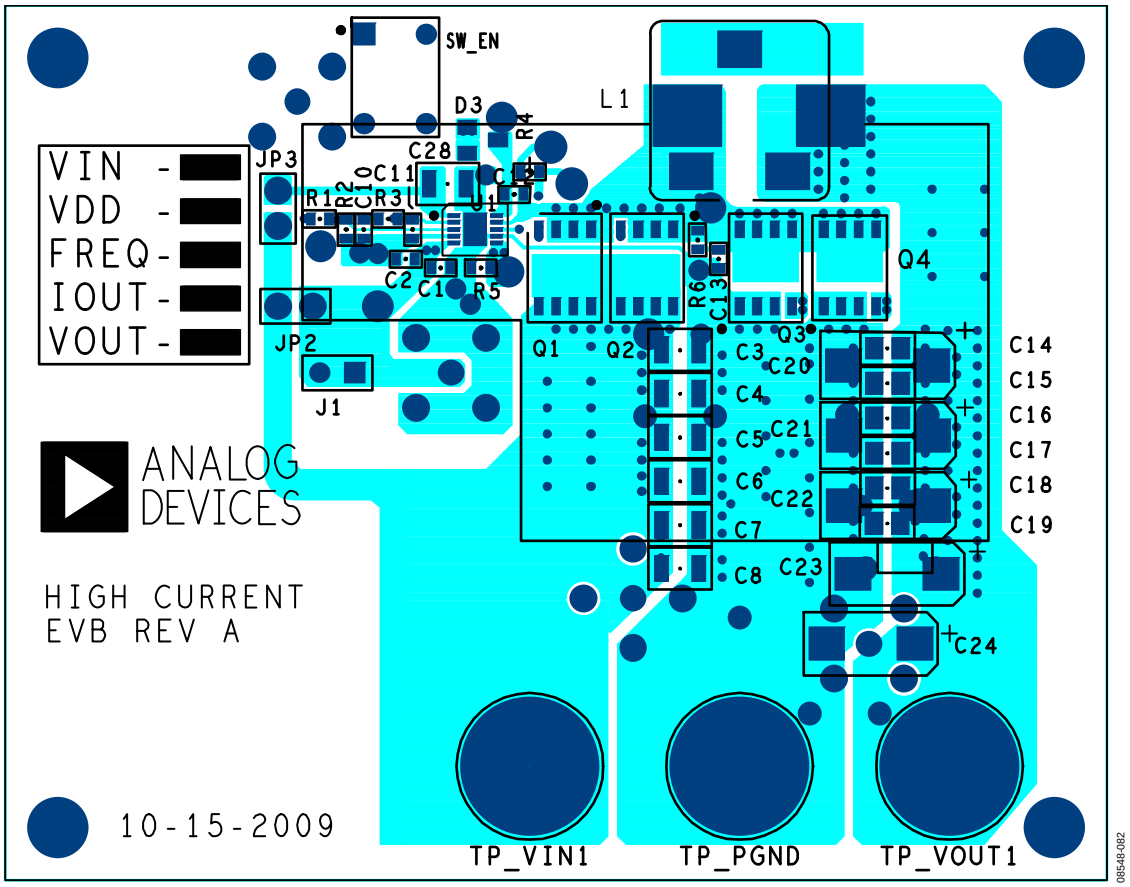

Figure 32. Layer 1

LAYER 2

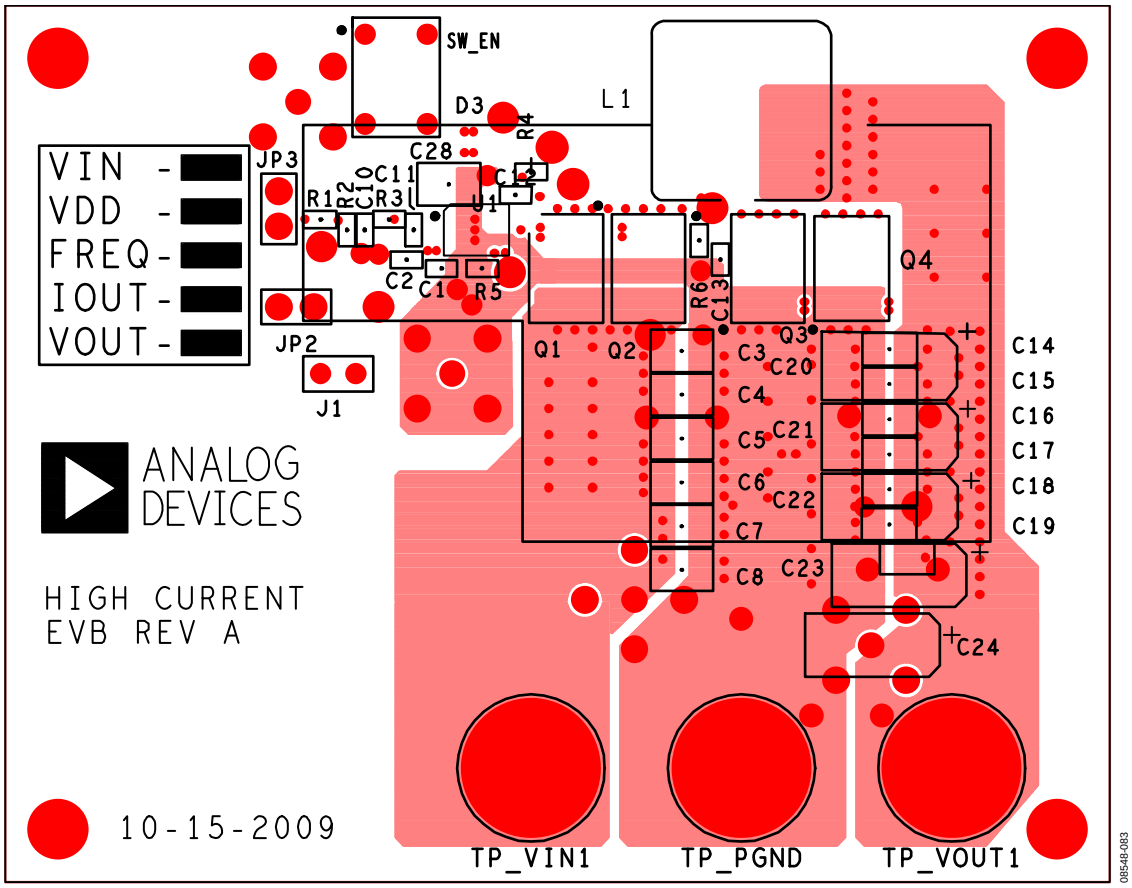

Figure 33. Layer 2

LAYER 3

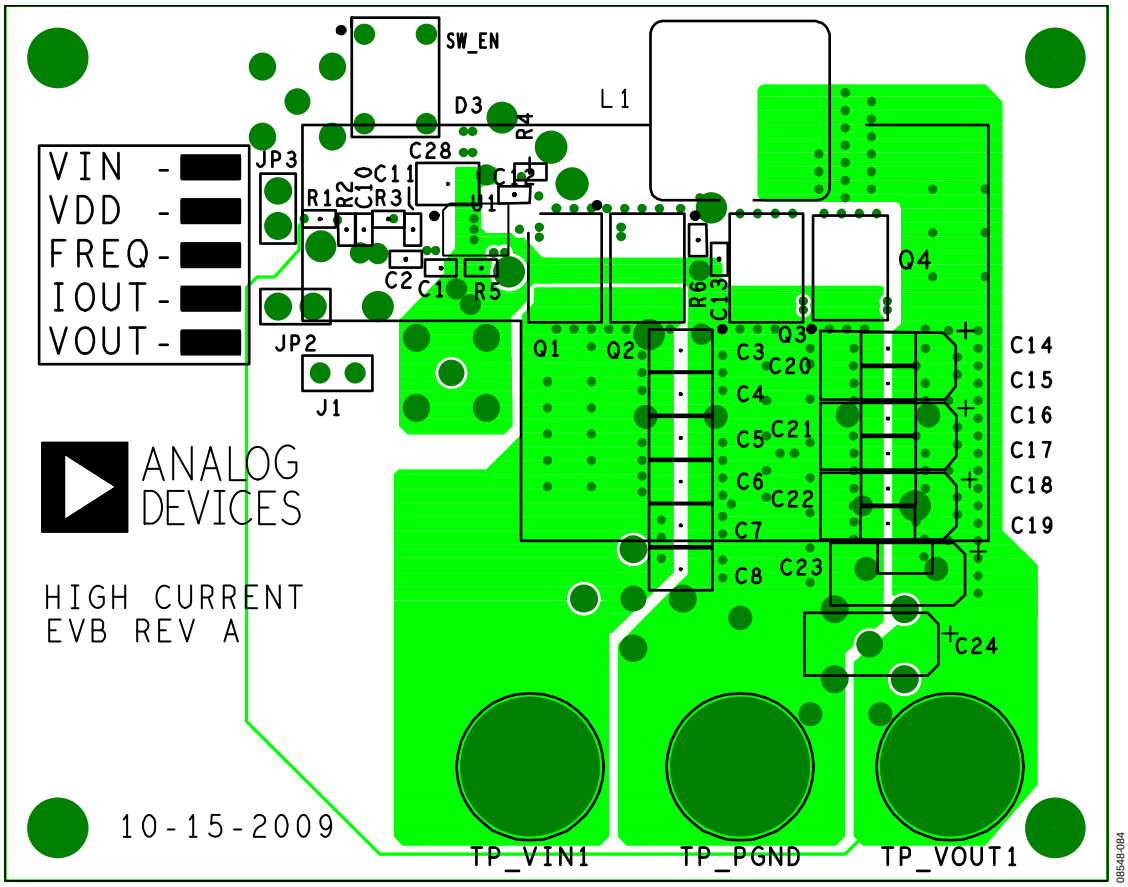

Figure 34. Layer 3

LAYER 4

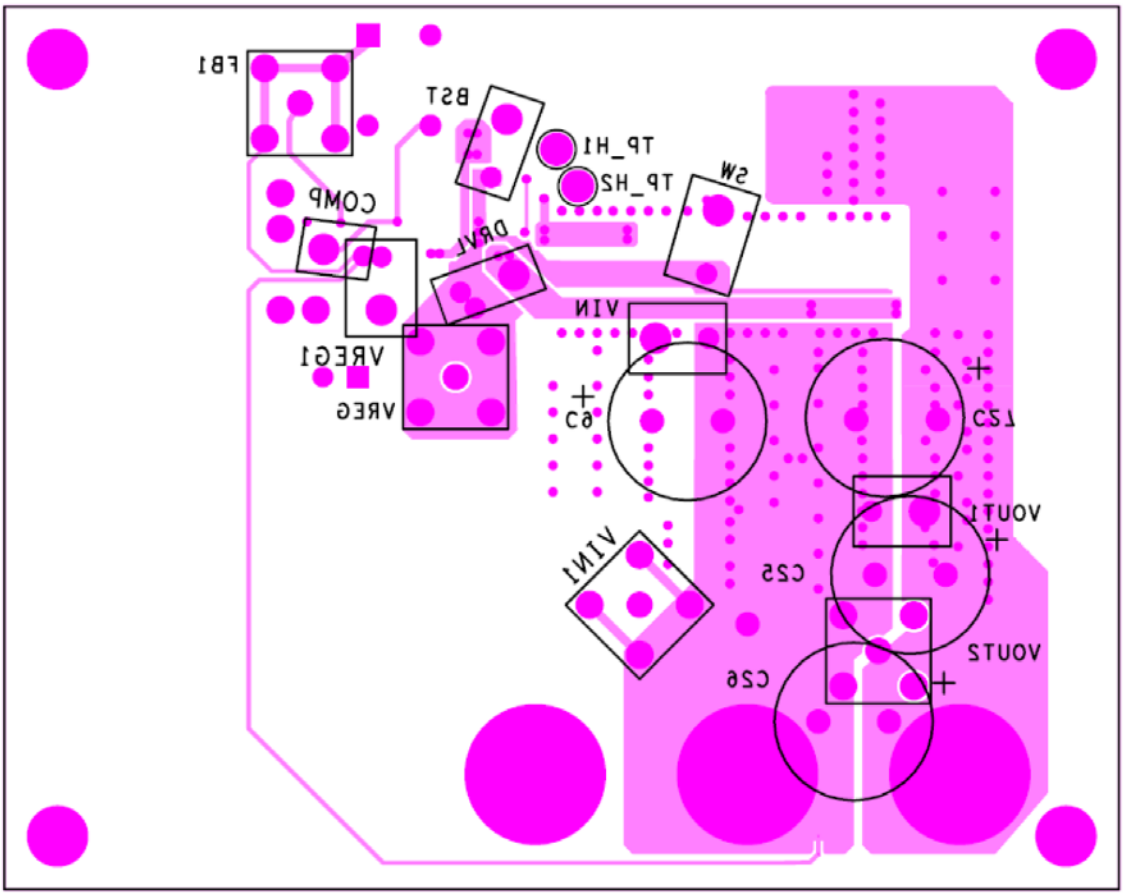

Figure 35. Layer 4

BILL OF MATERIALS

1.8 V OUTPUT, 300 kHz, 14 A APPLICATION CIRCUIT

Table 2.

Name	Reference Designator	Value	Unit	Manufacturer	Description/Model
C_{VDD}	C1	1.0	µF	Taiyo Yuden	1.0 µF, 6.3 V, X5R ceramic capacitor (0402), JMK105BJ105KV-F
C_{VDD}	C2	0.1	µF	TDK	0.1 µF, 25 V, X5R ceramic capacitor (0402), C1005X5R1E104K
C_{IN}	C3	22	µF	Murata	25 V, X7R, 1210 (3.2 mm × 2.5 mm × 2.5 mm) GRM32ER71E226KE15L
C_{IN}	C4	22	µF	Murata	25 V, X7R, 1210 (3.2 mm × 2.5 mm × 2.5 mm) GRM32ER71E226KE15L
C_{IN}	C5	22	µF	Murata	25 V, X7R, 1210 (3.2 mm × 2.5 mm × 2.5 mm) GRM32ER71E226KE15L
C_{IN}	C6	22	µF	Murata	25 V, X7R, 1210 (3.2 mm × 2.5 mm × 2.5 mm) GRM32ER71E226KE15L
C_{IN}	C7	22	µF	Murata	25 V, X7R, 1210 (3.2 mm × 2.5 mm × 2.5 mm) GRM32ER71E226KE15L
C_{IN}	C8	N/A	N/A		
C_{PAR}	C10	57	pF	Taiyo Yuden[1]	±10%, 50 V, X7R ceramic capacitor (0402)
C_C	C11	571	pF	Taiyo Yuden[1]	±5%, 50 V, C0H ceramic capacitor (0402)
C_{BST}	C12	100	nF	Taiyo Yuden[1]	±10%, 50 V, X7R ceramic capacitors (0603)
$C_{SNUBBER}$	C13	1.5	nF	Taiyo Yuden[1]	±10%, 50 V, X7R ceramic capacitors (0603)
C_{OUT}	C14	N/A	N/A		
C_{OUT}	C15	N/A	N/A		
C_{OUT}	C16	N/A	N/A		
C_{OUT}	C17	N/A	N/A		
C_{OUT}	C18	N/A	N/A		
C_{OUT}	C19	N/A	N/A		
C_{OUT}	C20	270	µF	Panasonic	SP-series, 4 V, 7 mΩ, 3.7 A EEFUE0G271LR (4.3 mm × 7.3 mm × 4.2 mm)
C_{OUT}	C21	270	µF	Panasonic	SP-series, 4 V, 7 mΩ, 3.7 A EEFUE0G271LR (4.3 mm × 7.3 mm × 4.2 mm)
C_{OUT}	C22	270	µF	Panasonic	SP-series, 4 V, 7 mΩ, 3.7 A EEFUE0G271LR (4.3 mm × 7.3 mm × 4.2 mm)
C_{OUT}	C23	270	µF	Panasonic	SP-series, 4 V, 7 mΩ, 3.7 A EEFUE0G271LR (4.3 mm × 7.3 mm × 4.2 mm)
C_{OUT}	C24	N/A	N/A		
R_{TOP}	R1	30	kΩ	Vishay[1]	±1% resistors (0603)
R_{BOT}	R2	15	kΩ	Vishay[1]	±1% resistors (0603)
R_C	R3	47	kΩ	Vishay[1]	±1% resistors (0603)
R_{GATE}	R4	0	kΩ	Vishay[1]	±1% resistors (0603)
R_{RES}	R5	100	kΩ	Vishay[1]	±1% resistors (0603)
$R_{SNUBBER}$	R6	2	Ω	Vishay[1]	±1% resistors (0603)
Top MOSFET	Q1	N/A	N/A	Infineon	BSC080N03MS G
Top MOSFET	Q2	N/A	N/A	Infineon	BSC080N03MS G
Bottom MOSFET	Q3	N/A	N/A	Infineon	BSC080N03MS G
Bottom MOSFET	Q4	N/A	N/A	Infineon	BSC080N03MS G
Inductor	L1	1.0	µH	Würth Elek	7443251200
Header	J1	N/A	N/A		
Header	JP2	N/A	N/A		
Header	JP3	N/A	N/A		
Banana Plugs	TP_VIN1	N/A	N/A		
Banana Plugs	TP_PGND	N/A	N/A		
Banana Plugs	TP_VOUT1	N/A	N/A		
Controller/Driver	U1	N/A	N/A	Analog Devices	ADP1872ARMZ-0.3-R7[2] (LDT) or ADP1873ARMZ-0.3-R7[2] (LDF)
Diode	D3	N/A	N/A		

[1] Components from other manufacturers can also be used, as long as the characteristics listed in the corresponding description are met.
[2] Z = RoHS Compliant Part.

3.3 V OUTPUT, 300 kHz, 14 A APPLICATION CIRCUIT

Table 3.

Name	Reference Designator	Value	Unit	Manufacturer	Description/Model
C_{VDD}	C1	1.0	µF	Taiyo Yuden[1]	±10%, 50 V, X7R ceramic capacitors (0603)
C_{VDD}	C2	0.1	µF	Taiyo Yuden[1]	±10%, 50 V, X7R ceramic capacitors (0603)
C_{IN}	C3	22	µF	Murata	25 V, X7R, 1210 (3.2 mm × 2.5 mm × 2.5 mm) GRM32ER71E226KE15L
C_{IN}	C4	22	µF	Murata	25 V, X7R, 1210 (3.2 mm × 2.5 mm × 2.5 mm) GRM32ER71E226KE15L
C_{IN}	C5	22	µF	Murata	25 V, X7R, 1210 (3.2 mm × 2.5 mm × 2.5 mm) GRM32ER71E226KE15L
C_{IN}	C6	22	µF	Murata	25 V, X7R, 1210 (3.2 mm × 2.5 mm × 2.5 mm) GRM32ER71E226KE15L
C_{IN}	C7	22	µF	Murata	25 V, X7R, 1210 (3.2 mm × 2.5 mm × 2.5 mm) GRM32ER71E226KE15L
C_{IN}	C8	N/A	N/A		
C_{PAR}	C10	57	pF	Taiyo Yuden[1]	±10%, 50 V, X7R ceramic capacitor (0402)
C_C	C11	571	pF	Taiyo Yuden[1]	±5%, 50 V, C0H ceramic capacitor (0402)
C_{BST}	C12	100	nF	Taiyo Yuden[1]	±10%, 50 V, X7R ceramic capacitors (0603)
$C_{SNUBBER}$	C13	1.5	nF	Taiyo Yuden[1]	±10%, 50 V, X7R ceramic capacitors (0603)
C_{OUT}	C14	N/A	N/A		
C_{OUT}	C15	N/A	N/A		
C_{OUT}	C16	N/A	N/A		
C_{OUT}	C17	N/A	N/A		
C_{OUT}	C18	N/A	N/A		
C_{OUT}	C19	N/A	N/A		
C_{OUT}	C20	330	µF	Panasonic	SP-series, 4 V, 7 mΩ, 3.7 A EEFUE0G331ER (4.3 mm × 7.3 mm × 4.2 mm)
C_{OUT}	C21	330	µF	Panasonic	SP-series, 4 V, 7 mΩ, 3.7 A EEFUE0G331ER (4.3 mm × 7.3 mm × 4.2 mm)
C_{OUT}	C22	N/A	N/A		
C_{OUT}	C23	N/A	N/A		
C_{OUT}	C24	N/A	N/A		
R_{TOP}	R1	67.5	kΩ	Vishay[1]	±1% resistors (0603)
R_{BOT}	R2	15	kΩ	Vishay[1]	±1% resistors (0603)
R_C	R3	47	kΩ	Vishay[1]	±1% resistors (0603)
R_{GATE}	R4	0	kΩ	Vishay[1]	±1% resistors (0603)
R_{RES}	R5	100	kΩ	Vishay[1]	±1% resistors (0603)
$R_{SNUBBER}$	R6	2	Ω	Vishay[1]	±1% resistors (0603)
Top MOSFET	Q1	N/A	N/A	Infineon	BSC080N03MS G
Top MOSFET	Q2	N/A	N/A	Infineon	BSC080N03MS G
Bottom MOSFET	Q3	N/A	N/A	Infineon	BSC080N03MS G
Bottom MOSFET	Q4	N/A	N/A	Infineon	BSC080N03MS G
Inductor	L1	2.0	µH	Würth Elek	7443551200
Header	J1	N/A	N/A		
Header	JP2	N/A	N/A		
Header	JP3	N/A	N/A		
Banana Plugs	TP_VIN1	N/A	N/A		
Banana Plugs	TP_PGND	N/A	N/A		
Banana Plugs	TP_VOUT1	N/A	N/A		
Controller/Driver	U1	N/A	N/A	Analog Devices	ADP1872ARMZ-0.3-R7[2] (LDT) or ADP1873ARMZ-0.3-R7[2] (LDF)
Diode	D3	N/A	N/A		

[1] Components from other manufacturers can also be used, as long as the characteristics listed in the corresponding description are met.
[2] Z = RoHS Compliant Part.

NOTES

NOTES

NOTES

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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