DS1831C/D/E

3.3V/2.5V Multi-Supply MicroMonitor

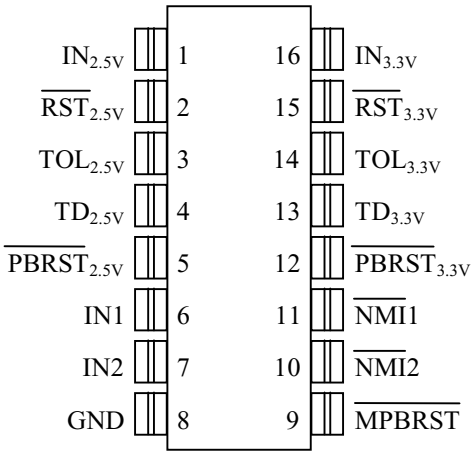
www.dalsemi.com

FEATURES

- 2.5V power-on reset
- 3.3 (or 3V) power-on reset
- 2 referenced comparators with separate outputs for monitoring additional supplies
- Internal power is drawn from higher of either the $IN_{2.5V}$ input or the $IN_{3.3V}$ input
- Excellent for systems designed to operate with multiple power supplies
- Asserts resets during power transients
- Pushbutton reset input for system override
- Maintains reset for user configurable times of 10 ms, 100 ms, or 1 sec
- Watchdog timer for software monitoring (DS1831D)
- Precision temperature-compensated voltage reference and voltage sensor
- 16 pin DIP & 16 pin 150 mil SOIC available
- Operating Temperature of -40°C to +85°C

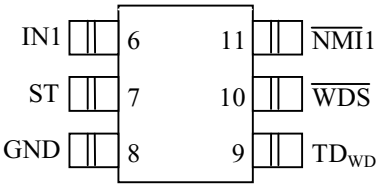
PIN ASSIGNMENT

DS1831C

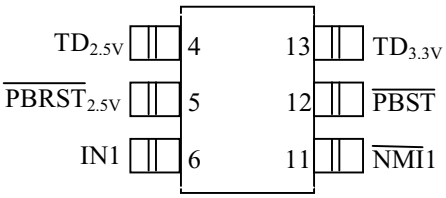


16-Pin (300 mil) DIP
&
16-Pin (150 mil) SOIC

DS1831D



DS1831E



DESCRIPTION

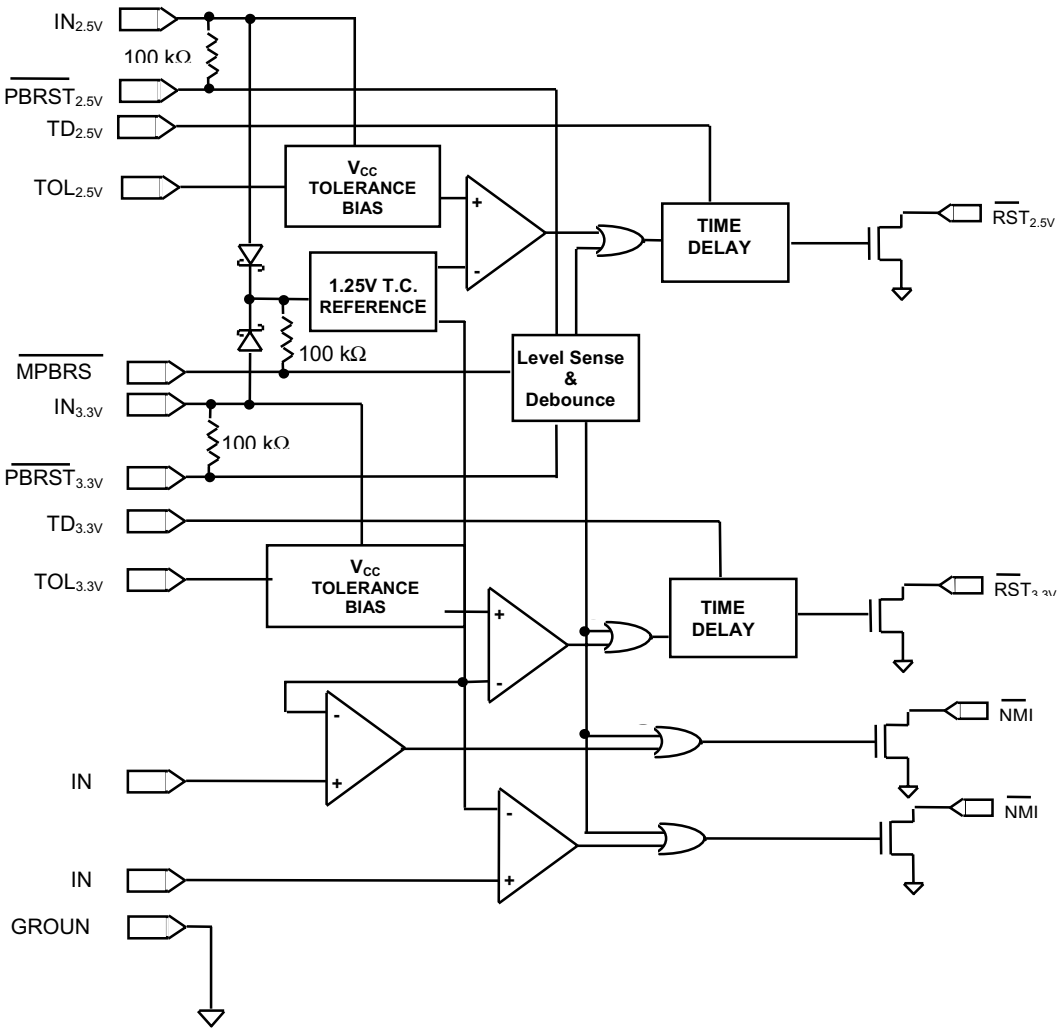
The DS1831C Multi-Supply Monitor & Reset monitors up to 4 system voltages: 2.5 volt supply, 3.3 (or 3) volt supply, and 2 additional user configurable voltage monitors. DS1831 power for internal operation comes from the higher voltage level of the 3.3 volt input or the 2.5 volt input. One of these inputs must be greater than 1 volt for device operation. Pushbutton (manual reset) functionality is provided for the 2.5 volt reset, the 3.3 volt reset or for all reset outputs by the master pushbutton. The DS1831D replaces one reference comparator and the master pushbutton with watchdog and the DS1831E replaces the 3.3-volt PBRST with a last reset status output.

TOL and TD inputs allow user configuration of the DS1831 for multiple applications. The TOL inputs configure the tolerance for the specified output and the TD inputs configure the reset time delays.

PIN CONFIGURATION

1	$IN_{2.5V}$	2.5V Power Supply Input	9	$\overline{MPBRST}$ TD_{WD}	Master Pushbutton (DS1831C/E) Watchdog Time Delay Select (DS1831D)
2	$\overline{RST}_{2.5V}$	2.5V Reset Open Drain Output	10	$\overline{NM12}$ $\overline{WDS}$	Non Maskable Interrupt 2 (DS1831C/E) Watchdog Status Output (DS1831D)
3	$TOL_{2.5V}$	Selects 2.5V Input Tolerance	11	$\overline{NM11}$	Non Maskable Interrupt 1
4	$TD_{2.5V}$	Selects 2.5V Reset Time Delay	12	$\overline{PBRST}_{3.3V}$ $\overline{PBST}$	3.3V Reset Pushbutton (DS1831C/E) Pushbutton Status Output (DS1831E)
5	$\overline{PBRST}_{2.5V}$	2.5V Reset Pushbutton	13	$TD_{3.3V}$	Select 3.3V Reset Time Delay
6	IN1	Sense Input 1	14	$TOL_{3.3V}$	Selects 3.3V Input Tolerance
7	IN2 ST	Sense Input 2 (DS1831C/E) Watchdog Strobe Inputs (DS1831D)	15	$\overline{RST}_{3.3V}$	3.3V Reset Open Drain Output
8	GND	Ground	16	$IN_{3.3V}$	3.3V Power Supply Input

BLOCK DIAGRAM Figure 1



OPERATION – POWER MONITOR

The DS1831 provides the functions of detecting out-of-tolerance conditions on a 3.3 (or 3) volt and 2.5 volt power supply and warning a processor based system of impending power failure. When an input is detected as out-of-tolerance on either voltage input the $\overline{RST}$ for that supply will be forced active low. When that input returns to a valid state the associated $\overline{RST}$ will remain active for the time delay selected with the associated TD input and then return to an inactive state until the next input out-of-tolerance condition.

On power-up both resets are kept active for the selected reset time after the associated power supply input has reached the selected tolerance. This allows the power supply and system power to stabilize before $\overline{RST}$ is released.

All internal operating current for the DS1831 will be supplied by either the $IN_{3.3V}$ or $IN_{2.5V}$ input which ever has the highest voltage level.

OPERATION - TOLERANCE SELECT

The DS1831 provides 2 TOL inputs for individual customization of the DS1831 to specific application requirements. If the TOL for the 2.5 volt supply is tied to the 2.5 volt input a 5% tolerance is selected. If the TOL is connected to ground a 10% tolerance is selected or if it is left unconnected a 15% tolerance is selected. If the TOL for the 3.3 volt supply is tied to the 3.3 volt input a 5% tolerance is selected, a 10% tolerance is selected if it is connected to ground, and a 20% tolerance is selected if the input is left unconnected. These tolerance conditions are set at power up and can only be changed by power cycling the device.

OPERATION - RESET TIME-DELAY SELECT

The DS1831 provides 2 TD inputs for individual customization of reset time delays and an additional one for the DS1831D watchdog. TD inputs select time delays for the $IN_{2.5V}$ and $IN_{3.3V}$ resets outputs and the Watchdog on the DS1831D. The reset time delays are shown in table 1. These allow the selection of minimum delays of 10 ms, 100 ms, and 1000 ms.

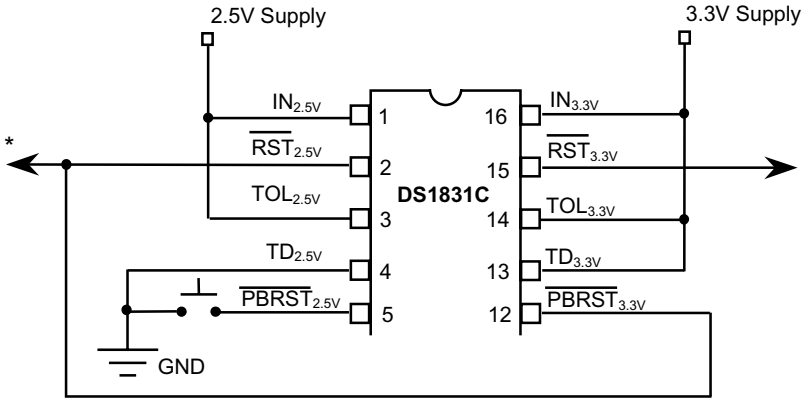
Wiring an individual reset output to the push-button input of the other voltage reset allows custom reset timings or allows for the sequencing of the reset outputs. See figure 2.

These time delays are set at power-up and cannot be changed after the device reaches an in-tolerance condition.

TD INPUTS/RESET AND WATCHDOG TIME-DELAYS Table 1

	RESET TIME-DELAY		
TD	**MIN**	**TYP**	**MAX**
GND	10 ms	16 ms	20 ms
Float	100 ms	160 ms	200 ms
V_{CC}	1000 ms	1600 ms	2000 ms

PUSHBUTTON RESET SEQUENCING Figure 2



*NOTE:

The $\overline{RST}_{2.5}$ volt output is connected to the $IN_{3.3V}$ via a 100 kΩ resistor in the push-button input and therefore does not require a pull-up resistor (an addition pull up can be used to accelerate responses.) If an external pull-up is used in this example it must be connected to the 3.3 volt power supply.

OPERATION - PUSHBUTTON RESET

The DS1831 provides 3 pushbutton inputs for manual reset of the device. Pushbutton inputs for the 3.3 volt reset, 2.5 volt reset, and a master pushbutton reset (DS1831C & DS1831D only) input; provide multiple options for system control. The 3.3 volt pushbutton reset and 2.5 volt pushbutton resets provide a simple manual reset for the associated reset output; while the master pushbutton reset forces all resets and NMI outputs active low.

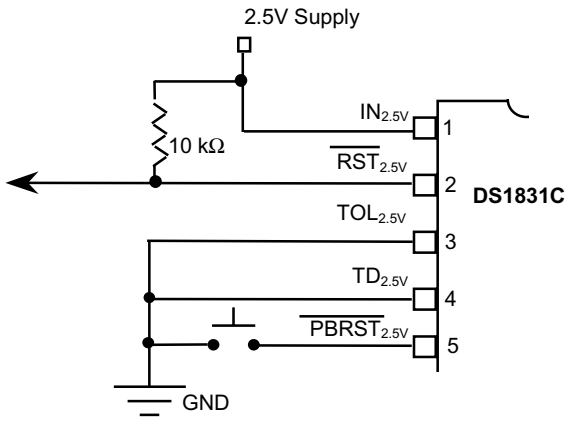
The 2.5 volt reset pushbutton input and the 3.3 volt reset pushbutton input provide manual reset control for each associated reset output. When the output associated with a pushbutton input is not active, a pushbutton reset can be generated by pulling the associated $\overline{PBRST}$ pin low for at least 20 µs. When the pushbutton is held low the reset will be forced active and will remain active for a reset cycle after the pushbutton is released. See figure 2 for an application example that allows a user to sequence the reset outputs.

A master pushbutton reset cycle can be started if at least one voltage input ($IN_{2.5V}$, $IN_{3.3V}$, IN1, or IN2) is in tolerance and at least 1 output is active. A master pushbutton reset is generated by pulling the $\overline{MPBRST}$ pin low for at least 20 µs. When the pushbutton is held low all outputs are forced active and will remain active for a reset or NMI time delay after the pushbutton is released. The Master Pushbutton input is pulled high through an internal 100 kΩ pull up resistor and debounced via internal circuitry. See figure 3 for an application example. Figures 4 and 5 for the timing diagram.

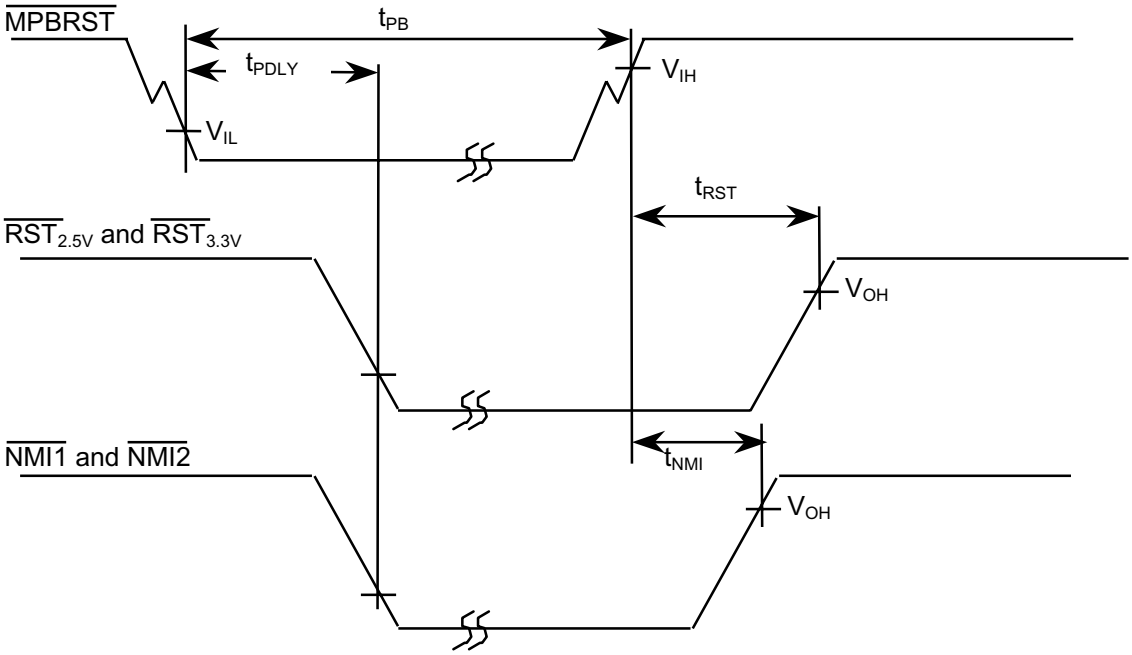
The 2.5 volt and 3.3 volt pushbutton reset inputs are pulled high through an internal 100 kΩ pull up resistor to the voltage input, which is associated with that pushbutton. The master pushbutton is pulled to the greater of the "$IN_{2.5V}$" and "$IN_{3.3V}$" inputs.

*Caution should be exercised to avoid pulling the pushbutton inputs above associated supply inputs. Generally all pushbutton inputs should be driven low with open drain inputs.

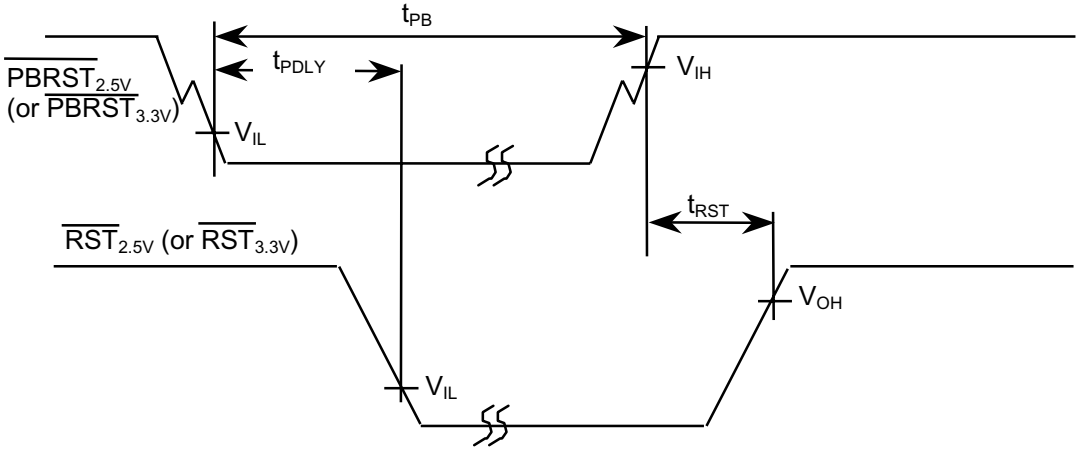
PUSHBUTTON RESET Figure 3



TIMING DIAGRAM – MASTER PUSHBUTTON RESET Figure 4



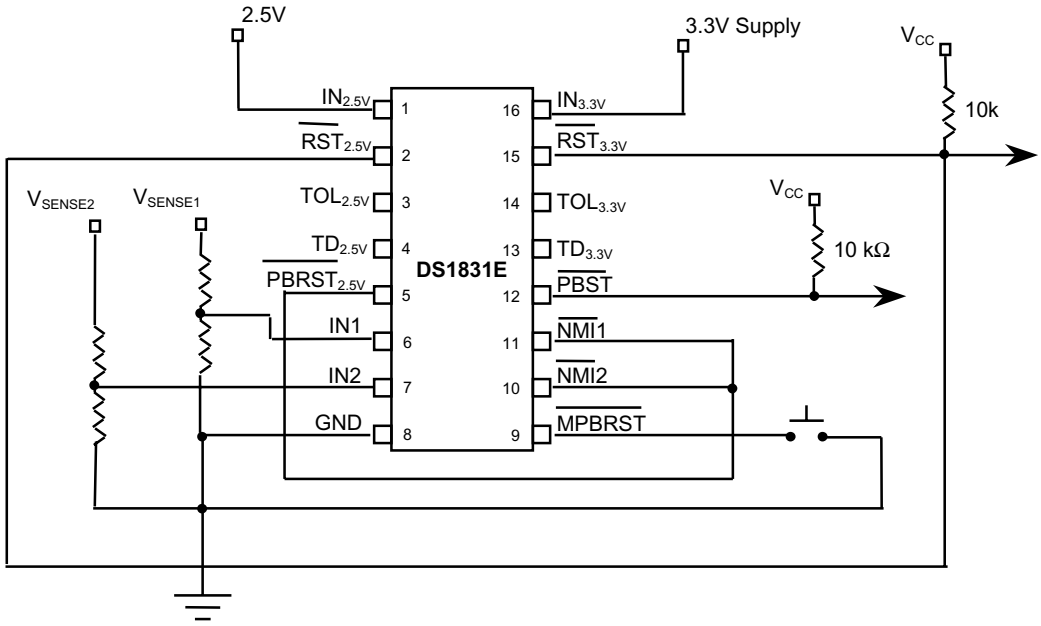
TIMING DIAGRAM – 2.5V OR 3.3V PUSHBUTTON RESET Figure 5



OPERATION – PUSHBUTTON STATUS

The DS1831E provides a master pushbutton status open drain output. The $\overline{PBST}$ output indicates the status of the most recent reset condition. If the last reset was generated by the master pushbutton input it would maintain a low condition until cleared by another event (except the master pushbutton) generating a reset. Once cleared it will remain high until the master pushbutton is pulled low generating a reset condition. The $\overline{PBST}$ output is open drain and will require a pull-up resistor on the output to maintain a valid condition. The value of the pull up resistor is not critical in most cases but must be set low enough to pull the output to a high state. A common value used is 10 kΩs (See Figure 6).

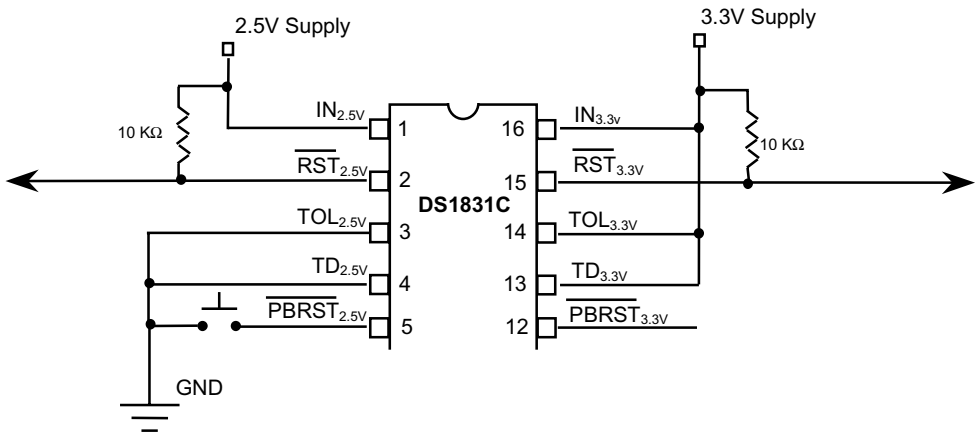
DS1831E APPLICATION EXAMPLE Figure 6



OUTPUT VALID CONDITIONS

The DS1831 can maintain valid outputs as long as one input remains above 1.0 volt. Accurate voltage monitoring additionally requires that either the 3.3 volt IN or 2.5 volt IN input be above 1.5 volts. If this condition is not met and at least one of the supply inputs are at or above 1.0 volt all outputs are maintained in the active condition. The DS1831 requires pull-up resistors on the outputs to maintain a valid output. The value of the pull up resistor is not critical in most cases but must be set low enough to pull the output to a high state. A common pull-up resistor value used is 10 kΩs (See Figure 7).

APPLICATION DIAGRAM - OPEN DRAIN OUTPUTS Figure 7



NOTE:

If outputs are at different voltages the outputs can not be connected to form a wired AND.

OPERATION - NON-MASKABLE INTERRUPT

The DS1831 has 2 referenced comparator (DS1831D has only 1 referenced comparator) that can be used to monitor upstream voltages or other system specific voltages. Each comparator is referenced to the 1.25 volt internal band gap reference and controls an open drain output. When a voltage being monitored decays to the voltage sense point, the DS1831 pulses the $\overline{\text{NMI}}$ output to the active state for a minimum 10 µs. The comparator detection circuitry also has built-in hysteresis of 100 µV. The supply must be below the voltage sense point for approximately 2 µs before a low $\overline{\text{NMI}}$ will be generated. In this way, power supply noise is minimized in the monitoring function, reducing false interrupts. See Figure 8 for the non-maskable timing diagram.

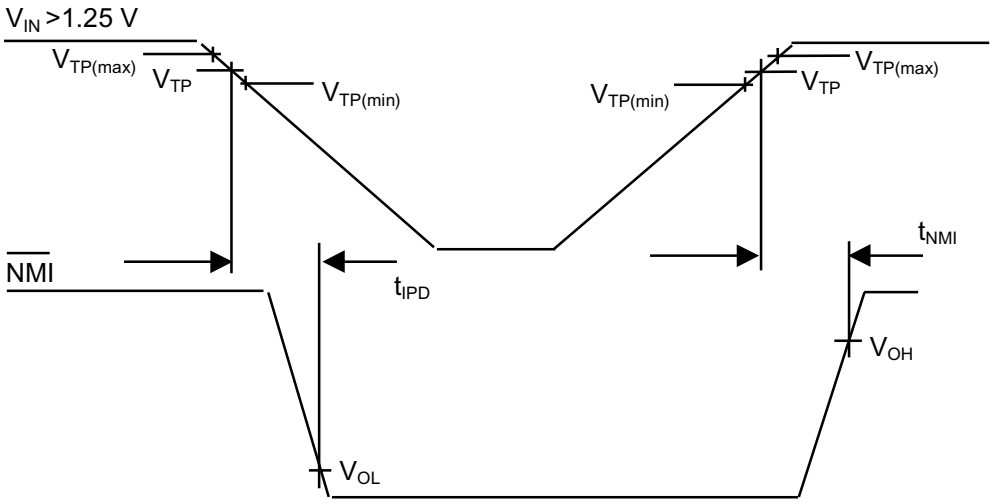
Versatile trip voltages can be configured by the use of an external resistor divider to divide the voltage at a sense point to the 1.25 volt trip levels of the referenced comparators. See figure 9 for an example circuit diagram and sample equations. The equations demonstrate a design process to determine the resistor values to use.

Connecting one or both $\overline{\text{NMI}}$ outputs to one of the reset specific $\overline{\text{PBRST}}$'s allows the non-maskable interrupt to generate an automatic reset for the reset time period when an out-of-tolerance condition occurs in a monitored supply. An example is shown in Figure 9.

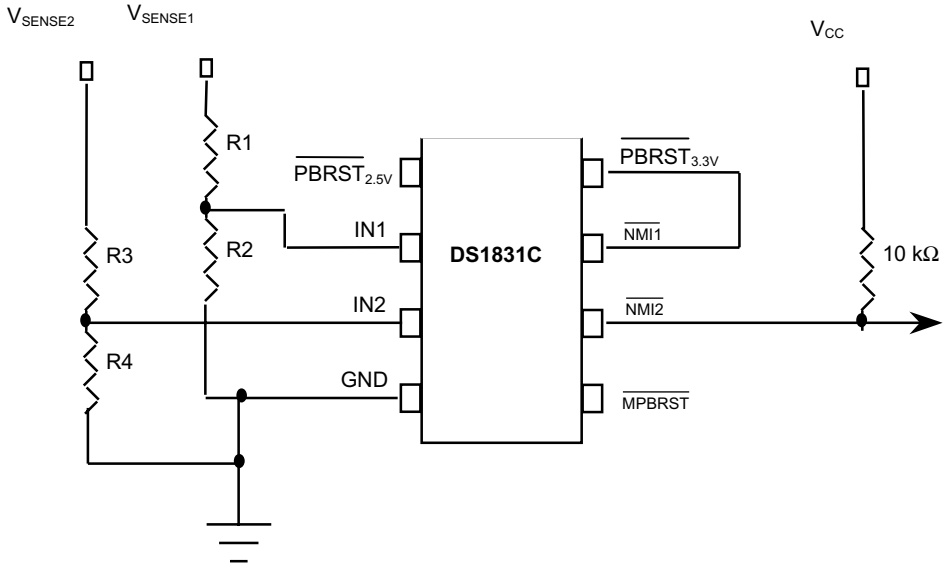
The output associated with the specific input will be held low if the voltage on the input pin is less than 1.25 volts. If the voltage is above 1.25 volts the output will not sink current and will be pulled up by the required pull up resistor. The value of the resistors is not critical in most cases but must be set low enough to pull the output to a high state. A common value used is 10 kΩs. If a $\overline{\text{NMI}}$ output is connected to a pushbutton input an additional pull-up resistor can be used (to improve speed of transitions) but is not required.

During a power-up, any detected IN pin levels above V_{TP} by the comparator are disabled from generating an inactive (high) interrupt until at least 1 supply on the V_{IN} inputs rises above 1.5 volts. All NMI outputs will be held active (low) until at least one V_{IN} reaches 1.5 volts at which point the $\overline{\text{NMI}}$ outputs will be based on the value of the associated IN input.

TIMING DIAGRAM - NON MASKABLE INTERRUPT Figure 8



NON MASKABLE INTERRUPT CIRCUIT EXAMPLE Figure 9



Example: V_{SENSE1} = 11.50 volts trip point $V_{SENSE1} = \frac{R1 + R2}{R2}$ X 1.25V

Therefore: $11.50V = \frac{R1 + 100\,k\Omega}{100\,k\Omega}$ X 1.25V

Resulting In: R1 = 820 kΩ

Repeat the same steps to solve for R3 and R4 with V_{SENSE2}.

OPERATION - WATCHDOG TIMER

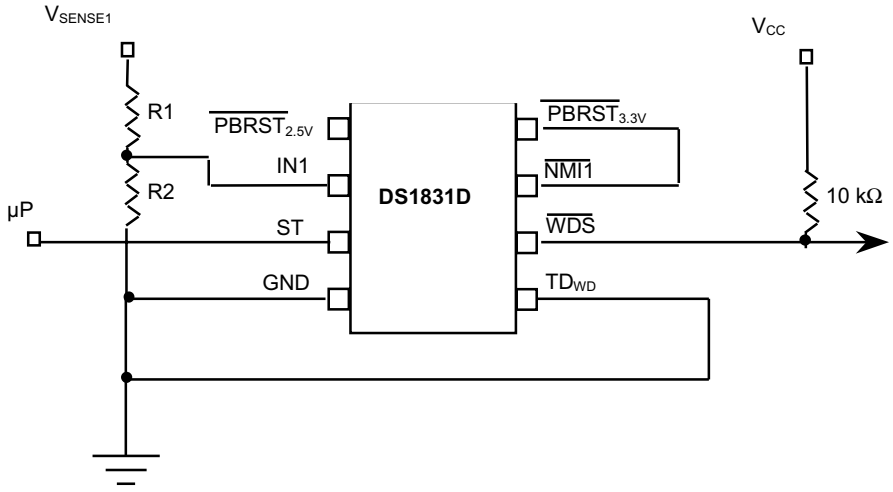
The watchdog timer function (DS1831D only) forces the $\overline{WDS}$ signal active (low) when the $\overline{ST}$ input does not have a transition (high-to-low or low-to-high) within the predetermined time period. The time-out period is determined by the condition of the TD_{WD} pin. If TD_{WD} is connected to ground the minimum watchdog time-out would be 10 ms, TD floating would yield a minimum time-out of 100 ms, and TD_{WD} connected to V_{CC} would provide a time-out of 1000 ms minimum. Time-out of the watchdog starts when at least one of the $\overline{RST}$ outputs becomes inactive (high). If a transition occurs on the ST input pin prior to time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the $\overline{WDS}$ output is pulsed active for a minimum of 100 µs.

The $\overline{WDS}$ output is an open-drain output and must be pulled up externally. In most applications this output would be connected to one of the Pushbutton inputs and would not require an external pull-up resistor. The value of the resistors is not critical in most cases but must be set low enough to pull the output to a high state. A common value used is 10 kΩs. If a $\overline{WDS}$ output is connected to a pushbutton input an additional pull-up resistor can be used (to improve speed of transitions) but is not required.

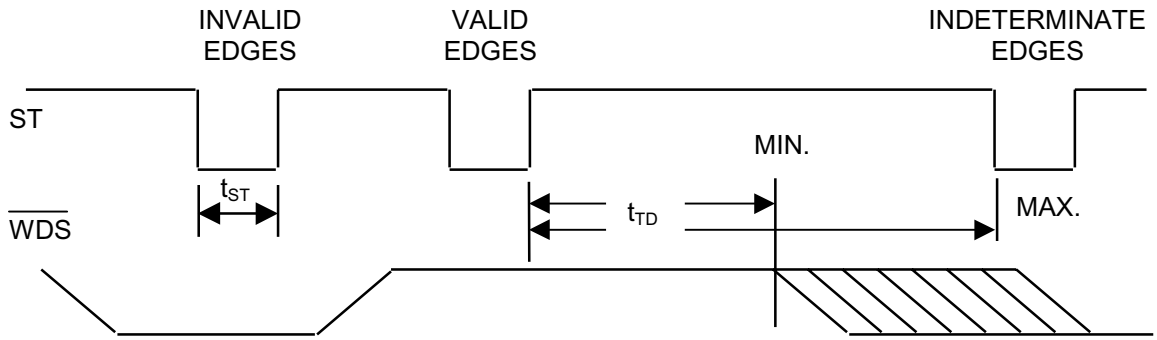
The $\overline{ST}$ input can be derived from many microprocessor outputs. The most typical signals used are the microprocessor address signals, data signals, or control signals. When the microprocessor functions normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time-out. To guarantee that the watchdog timer does not time-out, a transition must occur at or less than the minimum times shown in Table 1. A typical circuit example is shown in Figure 10. The watchdog timing is shown in Figure 11.

The DS1831A watchdog function cannot be disabled. The watchdog strobe input must be strobed to avoid a watchdog time-out however the watchdog status output can be disconnected yielding the same result.

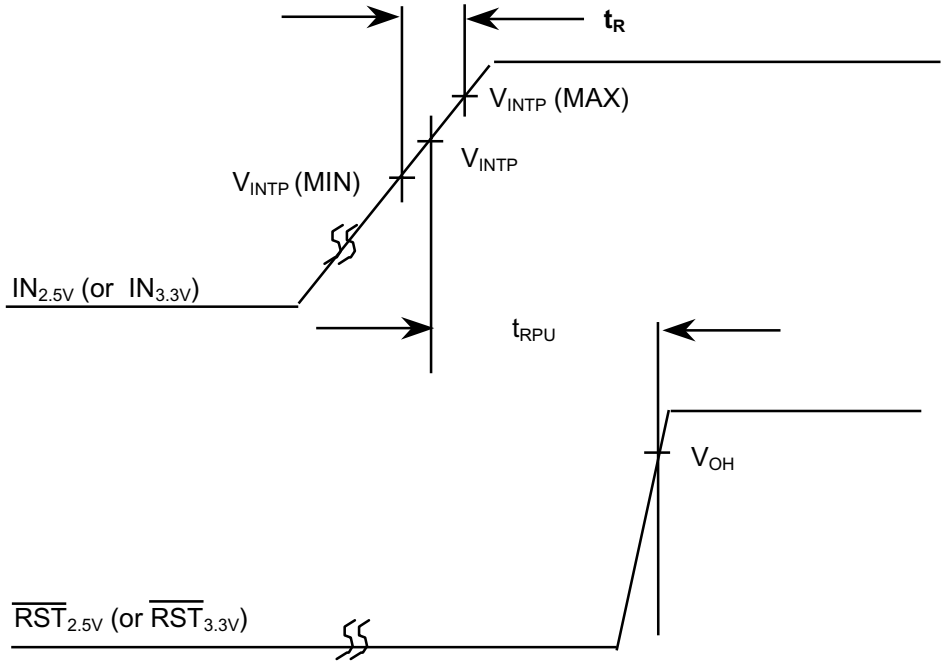
WATCHDOG CIRCUIT EXAMPLE Figure 10



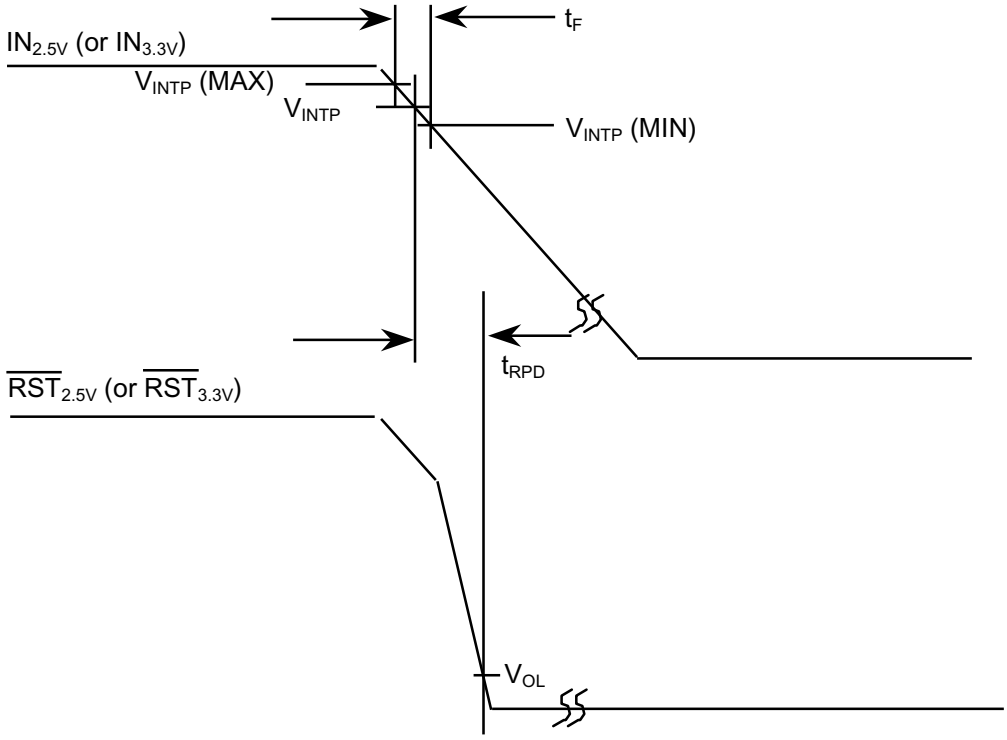
TIMING DIAGRAM-STROBE INPUT Figure 11



RESET TIMING DIAGRAM - POWER UP Figure 12



RESET TIMING DIAGRAM - POWER DOWN Figure 13



ABSOLUTE MAXIMUM RATINGS*

Voltage on $IN_{2.5V}$ or $IN_{3.3V}$ Pins Relative to Ground	-0.5V to +7.0V
Voltage on either $\overline{RST}$ Relative to Ground	-0.5V to the greater of $IN_{2.5V}$ + 0.5V or $IN_{3.3V}$ + 0.5V
Voltage on $\overline{PBRST}_{3.3V}$ Relative to Ground	-0.5V to $IN_{3.3V}$ + 0.5V
Voltage on $\overline{PBRST}_{2.5V}$ Relative to Ground	-0.5V to $IN_{2.5V}$ + 0.5V
Voltage on $\overline{MPBRST}$ Relative to Ground	-0.5V to the greater of $IN_{2.5V}$ + 0.5V or $IN_{3.3V}$ + 0.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

** The voltage input on IN and ST inputs can be exceeded if the input current is less than 10 mA.

RECOMMENDED DC OPERATING CONDITIONS (-40° to 85°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
$IN_{2.5V}$ (Supply Voltage)	V_{IN}	1.0	5.5	V	1
$IN_{3.3V}$ (Supply Voltage)	V_{IN}	1.0	5.5	V	1
ST and $\overline{MPBRST}$ input High Level	V_{IH}	2	V_{INT} + 0.3	V	1,2*
		V_{INT}-0.4		V	1,3*
$\overline{PBRST}_{3.3V}$ input High Level	V_{IH}	2	$IN_{3.3V}$ + 0.3	V	1
$\overline{PBRST}_{2.5V}$ input High Level	V_{IH}	2	$IN_{2.5V}$ +0.3	V	1
ST, $\overline{PBRST}_{3.3V}$, $\overline{PBRST}_{2.5V}$ and $\overline{MPBRST}$ input Low Level	V_{IL}	-0.3	.5	V	1

* V_{INT} is the greater voltage level of the $IN_{2.5V}$ or $IN_{3.3V}$.

DC ELECTRICAL CHARACTERISTICS (-40° to 85°C, VCC = 1.0V TO 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	µA	4
Output Current @ 2.4V	I_{OH}					5
Output Current @ 0.4V	I_{OL}	+10			mA	6
Operating Current @ ⇐5.5V	I_{CC}		80	100	µA	7
Operating Current @ ⇐3.6V	I_{CC}		60	80	µA	8
$IN_{3.3V}$ Trip Point ($TOL_{3.3V}$ = $IN_{3.3V}$)	V_{INTP}	2.98	3.06	3.15	V	1
$IN_{3.3V}$ Trip Point ($TOL_{3.3V}$ = GND)	V_{INTP}	2.80	2.88	2.97	V	1
$IN_{3.3V}$ Trip Point ($TOL_{3.3V}$ = Float)	V_{INTP}	2.47	2.55	2.64	V	1
$IN_{2.5V}$ Trip Point ($TOL_{2.5V}$ = $IN_{2.5V}$)	V_{INTP}	2.250	2.312	2.375	V	1
$IN_{2.5V}$ Trip Point ($TOL_{2.5V}$ = GND)	V_{INTP}	2.125	2.187	2.250	V	1
$IN_{2.5V}$ Trip Point ($TOL_{2.5V}$ = Float)	V_{INTP}	2.000	2.062	2.125	V	1
IN Input Trip Points	V_{TP}	1.20	1.25	1.30	V	1

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Input Capacitance	C_{OUT}	7	pF	

AC ELECTRICAL CHARACTERISTICS

(-40° to 85°C, VCC = 1.0V TO 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RESET Active Time (TD=Low)	t_{RST}	10	16	20	ms	8
RESET Active Time (TD=Float)	t_{RST}	100	160	200	ms	8
RESET Active Time (TD=High)	t_{RST}	1000	1600	2000	ms	8
V_{CC} Detect to $\overline{RST}$	t_{RPU}	See RESET Active Time			ms	8
V_{CC} Detect to $\overline{RST}$	t_{RPD}		2	10	µs	9
VIN Detect to $\overline{NMI}$	t_{IPD}		2	10	µs	9
NMI Active Time	t_{NMI}	20			µs	
$\overline{PBRST}$ = V_{IL}	t_{PB}	20			µs	
$\overline{PBRST}$ Stable Low to Reset Active	t_{PDLY}			50	µs	
Watchdog Timeout ($TD_{(WD)}$=Low)	t_{TD}	10	16	20	ms	
Watchdog Timeout (TD_{WD}=Float)	t_{TD}	100	160	200	ms	
Watchdog Timeout (TD_{WD}=High)	t_{TD}	1000	1600	2000	ms	
ST Pulse Width	t_{ST}	10			ns	
V_{in} Slew Rate ($V_{INTP(MAX)}$ to $V_{INTP(MIN)}$)	t_F	300			µs	
V_{in} Slew Rate ($V_{INTP(MAX)}$ to $V_{INTP(MIN)}$)	t_R	0			ns	

NOTES:

1. All voltages are referenced to ground.
2. Measured with both $IN_{3.3V}$ & $IN_{2.5V} \geq 2.7V$.
3. Measured with both $IN_{3.3V}$ & $IN_{2.5V} \leq 2.7V$.
4. All Pushbutton inputs are internally pulled to the associated Supply IN input or the greatest Supply IN input for the $\overline{MPBRST}$ with an internal Impedance of 100 kΩ.
5. All outputs are Open Drain and output I_{OH} would be determined by the external pull-up resistor.
6. Measured with outputs open and $IN_{3.3V}$ or $IN_{2.5V} \leq$ 5.5V.
7. Measured with outputs open and $IN_{3.3V}$ or $IN_{2.5V} \leq$ 3.6V.
8. Measured using t_R = 5 µs.
9. Noise immunity - pulses <2 µs at a trip level will not cause a $\overline{RST}$ or $\overline{NMI}$.

Ordering Information

Ordering Part Number	Package Type	Description
DS1831C	16 Pin DIP 300 mil	2.5V/3.3V MultiSupply Monitor
DS1831CS	16 Pin SO 150 mil	2.5V/3.3V MultiSupply Monitor
DS1831D	16 Pin DIP 300 mil	2.5V/3.3V MultiSupply Monitor w/Watchdog
DS1831DS	16 Pin SO 150 mil	2.5V/3.3V MultiSupply Monitor w/Watchdog
DS1831E	16 Pin DIP 300 mil	2.5V/3.3V MultiSupply Monitor w/Pushbutton Status
DS1831ES	16 Pin SO 150 mil	2.5V/3.3V MultiSupply Monitor w/Pushbutton Status

* Add “/T&R” for tape and reeling of surface mount packages.