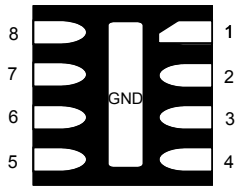
EMIF03-SIM02M8

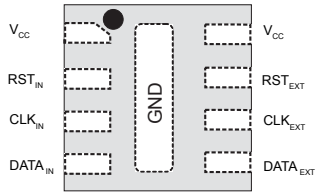
Datasheet

3 line IPAD, EMI filter for SIM card applications

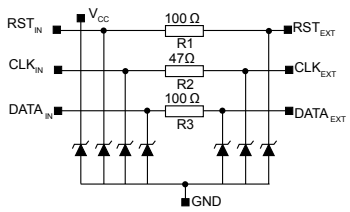


Micro QFN 1.7 mm x 1.5 mm
(bottom view)

Pin configuration (top view)



Device configuration



Maximum line capacitance = 20 pF

Product status
EMIF03-SIM02M8

Features

- SIM card EMI low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consuming: 1.7 mm x 1.5 mm
- Very thin package: 0.6 mm max.
- High efficiency in ESD suppression on external pins (IEC 61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging
- Lead free package
- Easy layout and flexibility thanks to I/O topology
- Low clamping voltage
- Complies with following standards:
  - IEC 61000-4-2 level 4 externals pins
    - 15 kV (air discharge)
    - 8 kV (contact discharge)
  - IEC 61000-4-2 level 2 internal pins
    - 2 kV (air discharge)
    - 2 kV (contact discharge)
- MIL STD 883G - Method 3015-7 Class 3A (all pins)

Applications

Where EMI filtering in ESD sensitive equipment is required:

- Keyboard for mobile phones
- Computers and printers
- Communication systems
- MCU boards

Description

The EMIF03-SIM02M8 is a 3 line highly integrated device designed to suppress EMI/RFI noise in all systems exposed to electromagnetic interference.

This filter includes ESD protection circuitry, which prevents damage to the application when subjected to ESD surges up to 15 kV on the external pins.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
V_{PP}	Internal pins:		kV
	ESD discharge IEC 61000-4-2 air discharge	2	
	ESD discharge IEC 61000-4-2 contact discharge	2	
	External pins and V_{CC}:		
	ESD discharge IEC 61000-4-2 air discharge	15	
	ESD discharge IEC 61000-4-2 contact discharge	8	
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Figure 1. Electrical characteristics (definitions)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current at VRM
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic resistance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input and Output
C_{line}	Input capacitance per line

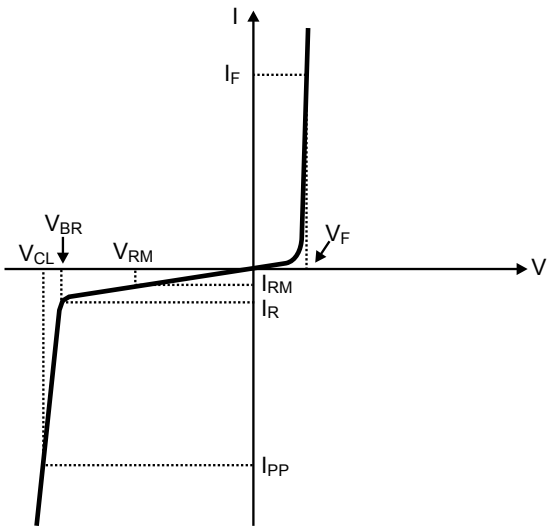


Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6		7.9	V
I_{RM}	V_{RM} = 3 V per line			0.2	µA
R1, R3	Tolerance ±20%		100		Ω
R13	Tolerance ±20%		47		Ω
C_{line}	V_R = 0 V, V_{OSC} = 30 mV, F = 1 MHz		17	20	pF

1.1 Characteristics (curves)

Figure 2. S21(db) attenuation (RST line)

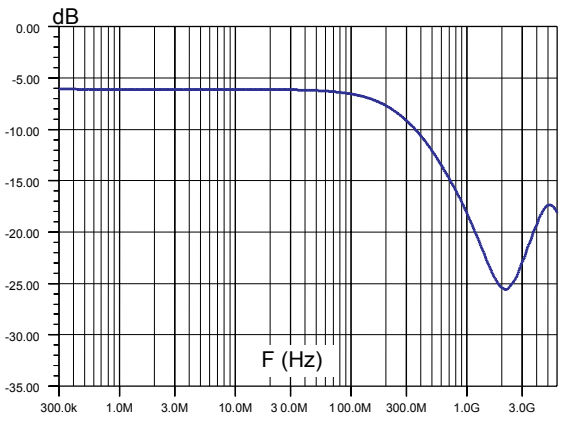


Figure 3. S21(db) attenuation (CLK line)

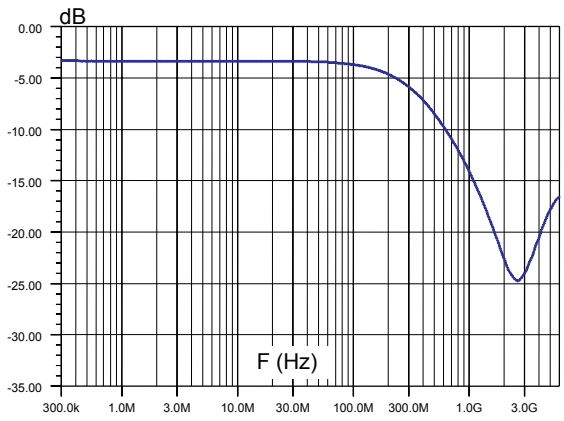


Figure 4. S21(db) attenuation (DATA line)

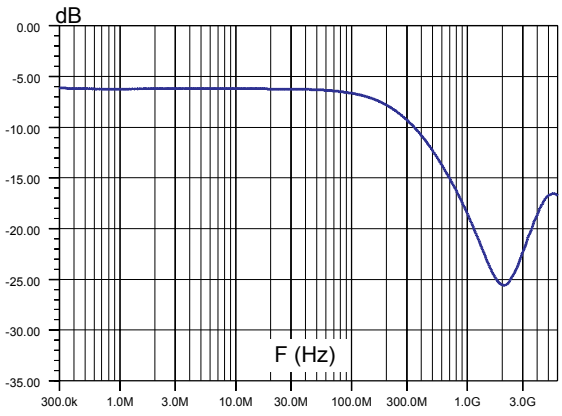


Figure 5. Analog cross talk measurements

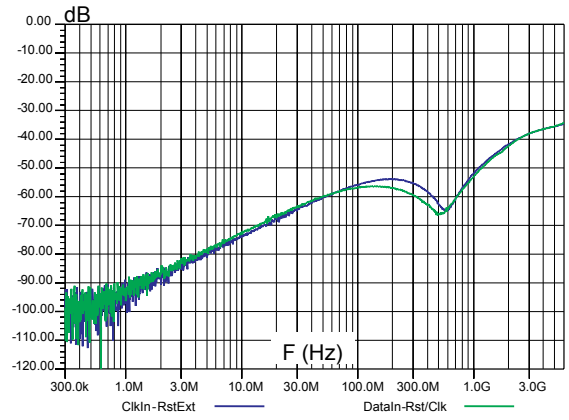


Figure 6. ESD response to IEC 61000-4-2 (+15 kV air discharge) applied to external pin

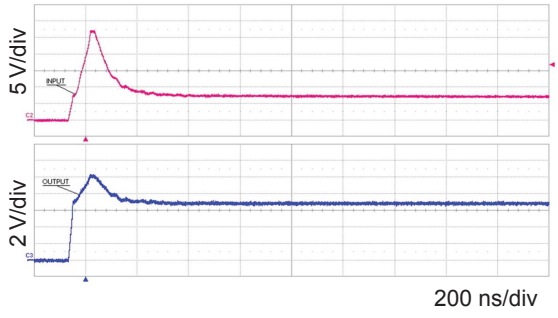


Figure 7. ESD response to IEC 61000-4-2 (-15 kV air discharge) applied to external pin

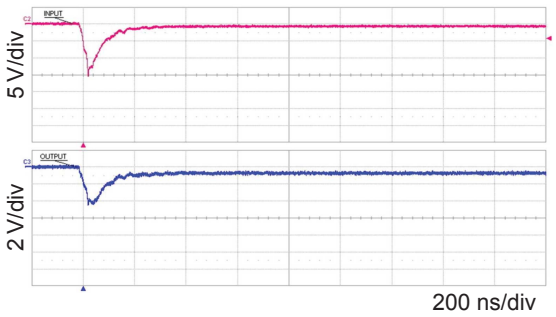


Figure 8. ESD response to IEC 61000-4-2 (+2 kV air discharge) applied to internal pin

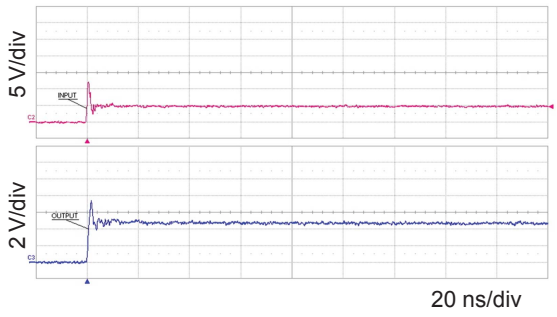
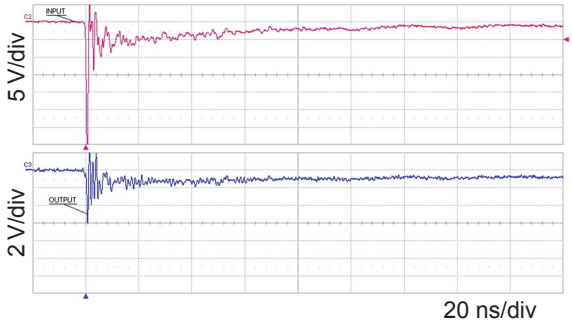
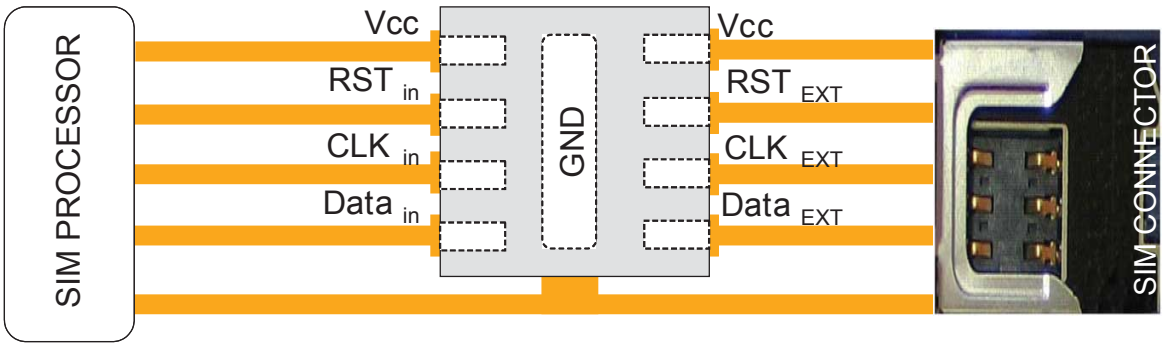


Figure 9. ESD response to IEC 61000-4-2 (-2 kV air discharge) applied to internal pin



2 Application information

Figure 10. **Application schematic**



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 Micro QFN 1.7x1.5-8L package information

- Epoxy meets UL94, V0

Figure 11. Micro QFN 1.7x1.5-8L package outline

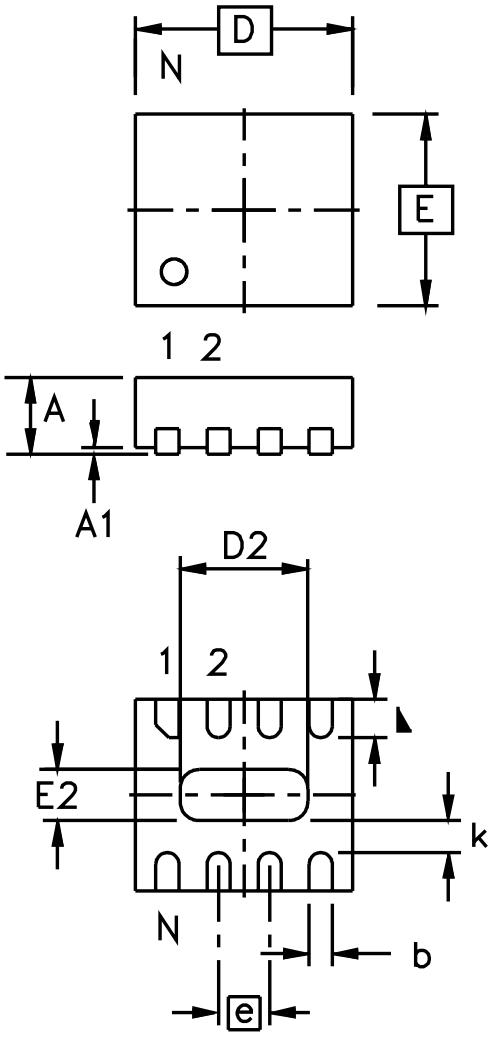


Table 3. Micro QFN 1.7x1.5-8L package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D	1.65	1.70	1.75
D2	0.85	1.00	1.10
E	1.45	1.50	1.55
E2	0.25	0.40	0.50
e	0.35	0.40	0.45
k	0.20		
L	0.25	0.30	0.35

Figure 12. Micro QFN 1.7x1.5-8L footprint (dimensions in mm)

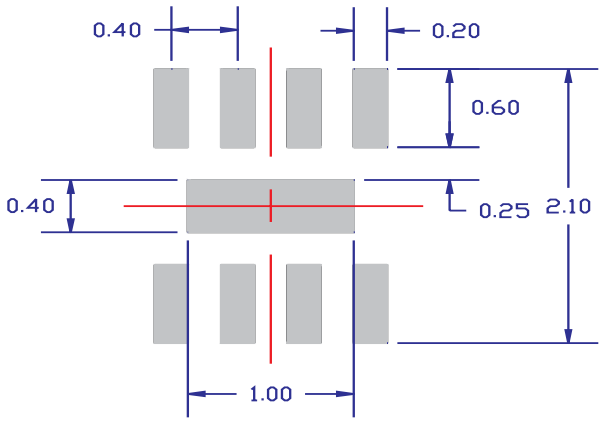
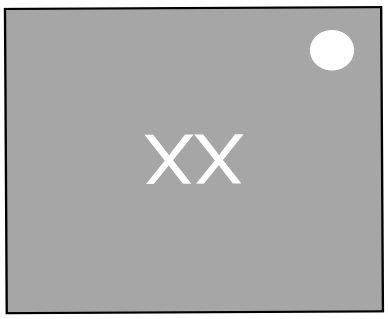
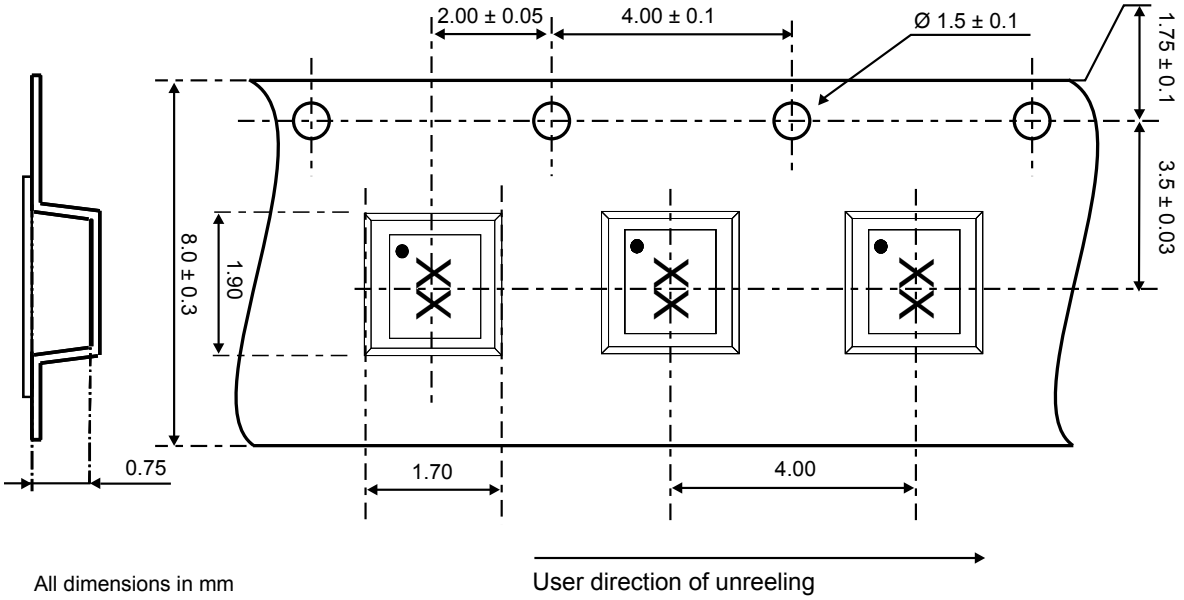


Figure 13. Marking



Dot : Pin 1 identification
XX : Marking code (cf Table 4: Ordering information)
The marking can be rotated by multiples of 90° to differentiate assembly locations

Figure 14. Tape and reel outline



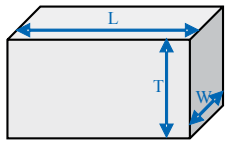
Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a. Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 15. Stencil opening dimensions



2. General design rule
   a. Stencil thickness (T) = 75 ~ 125 µm
   b. Aspect ratio = $\frac{W}{T} \geq 1.5$
   c. Aspect area = $\frac{L \times W}{2T(L + W)} \geq 0.66$
3. Reference design
   a. Stencil opening thickness: 100 µm
   b. Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c. Stencil opening for leads: Opening to footprint ratio is 90%

4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

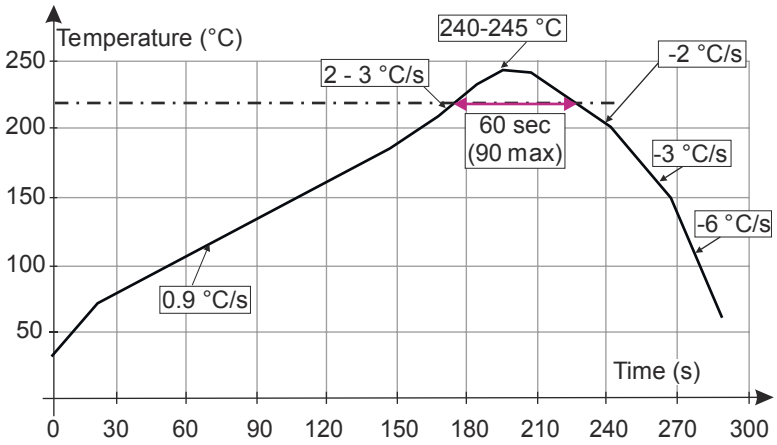
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

4.5 Reflow profile

Figure 16. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

5 Ordering information

Figure 17. **Ordering information scheme**

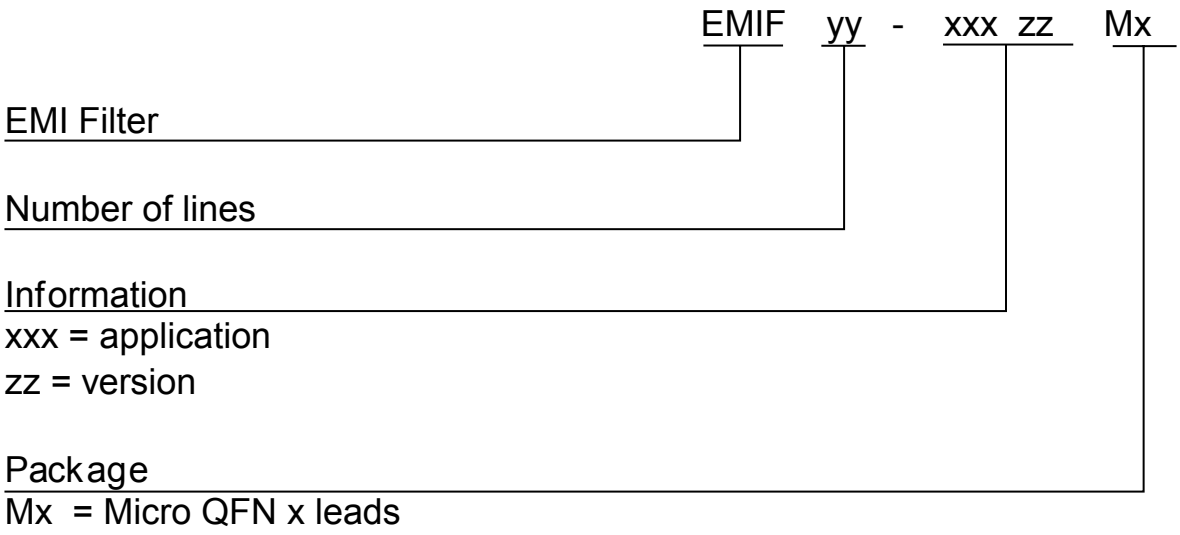


Table 4. **Ordering information**

Part number	Marking	Package	Weight	Base qty.	Delivery mode
EMIF03-SIM02M8	HA(1)	Micro QFN	4 mg	3000	Tape and reel (7”)

1. *The marking can be rotated by multiples of 90° to differentiate assembly locations.*

Revision history

Table 5. Document revision history

Date	Version	Changes
07-Oct-2007	1	Initial release.
31-Jan-2022	2	Updated Table 3. Micro QFN 1.7x1.5-8L package mechanical data and Figure 13. Marking. Minor text changes.