FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11467-1E

MEMORY Consumer FCRAM™
CMOS

256M Bit (4 bank x 2M word x 32 bit)
Consumer Applications Specific Memory for SiP

MB81ES253245

■ DESCRIPTION

The Fujitsu MB81ES253245 is a CMOS Fast Cycle Random Access Memory (FCRAM*) with Low Power SDRAM Interface containing 268,435,456 storages accessible in a 32-bit format.
MB81ES253245 is suited for consumer application requiring high data band width with low power consumption.

* : FCRAM is a trademark of Fujitsu Semiconductor Limited, Japan

■ FEATURES

- 2 M word × 32 bit × 4 banks organization
- Burst Read/Write Access Capability
  -t_{CK} = 6 ns Min / 166 MHz Max (Tj ≤ + 105 °C)
- Low Voltage Power Supply: $V_{DD} = V_{DDQ}$ = + 1.7 V to + 1.95 V
- Junction Temperature: T_J = − 25 °C to + 125 °C
- 1.8 V-CMOS compatible inputs
- Burst Length:1, 2, 4, 8, Full Column
- CAS latency: 2, 3, 4
- Auto Precharge option for each burst access
- Configurable Driver Strength and Pre Driver Strength
- Auto Refresh and Self Refresh Modes
- Deep Power Down Mode
- Low Power Consumption
  -I_{DDA1} = 75 mA Max (Tj ≤ + 105 °C)
- 4 K refresh cycles / 16 ms (Tj ≤ +105 °C)

2010.5

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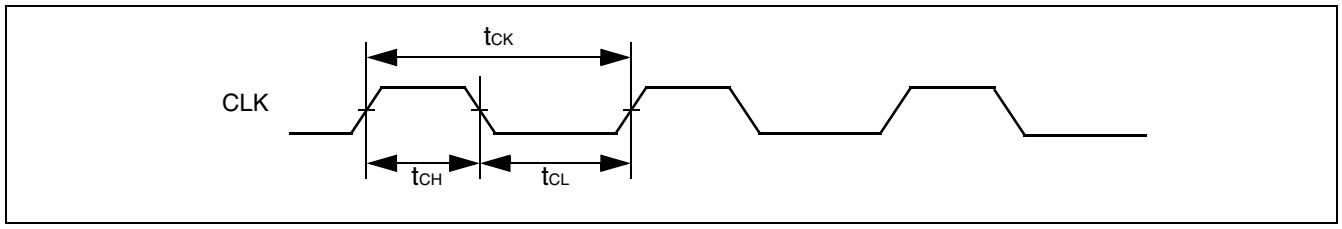
■ PIN DESCRIPTIONS

Symbol	Type	Function		
CLK	Input	Clock		
CKE	Input	Clock Enable		
$\overline{CS}$	Input	Chip Select		
$\overline{RAS}$	Input	Row Address Strobe		
$\overline{CAS}$	Input	Column Address Strobe		
$\overline{WE}$	Input	Write Enable		
BA[1:0]	Input	Bank Address Inputs		
A[11:0]	Input	Address Inputs	Row	A0 to A11
			Column	A0 to A8
AP(A10)	Input	Auto Precharge Enable		
DQM[3:0] *	Input	Input / Output Data Mask		
DQ[31:0] *	I/O	Data Bus Input / Output		
V_{DDQ}, V_{DD}	Supply	Power Supply		
V_{SSQ}, V_{SS}	Supply	Ground		

* : DQM0, DQM1, DQM2 and DQM3 correspond to DQ[7:0], DQ[15:8], DQ[23:16] and DQ[31:24].

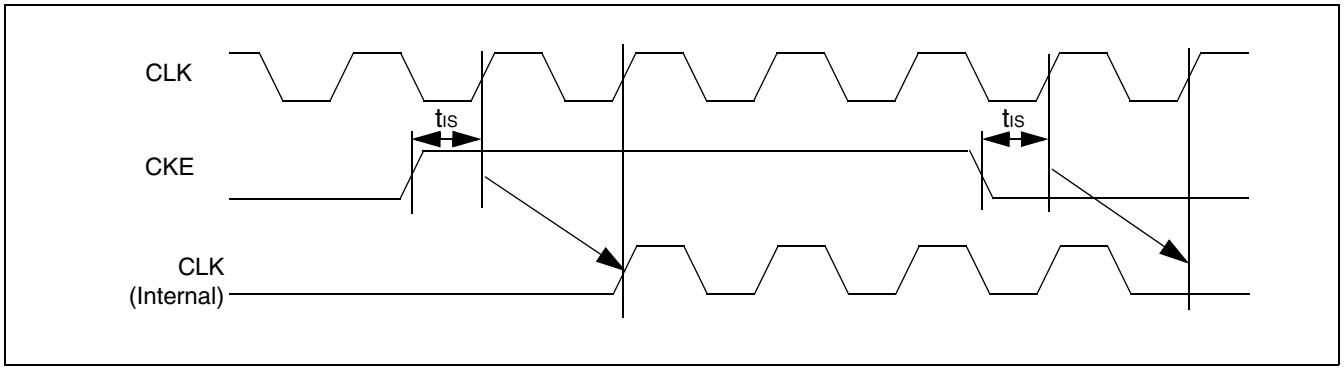
1. Clock Inputs (CLK)

CLK is a system clock input. All address and control input signals are sampled on the rising edge of CLK. And the rising edge of CLK increments device internal address counter and drives output data.



2. Clock Enable (CKE)

CKE is a high active clock enable signal. When CKE = Low is latched at the rising edge of CLK, the next CLK rising edge will be invalid. CKE controls power down mode and self refresh mode.



3. Chip Select ($\overline{CS}$)

$\overline{CS}$ enables all commands inputs, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$, and address inputs. $\overline{CS}$ = High disable command input but internal operation such as burst cycle will not be suspended.

4. Command Inputs ($\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$)

The combinations of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ input in conjunction with $\overline{CS}$ at a rising edge of the CLK define the command for device operation. Refer to the "■COMMAND TRUTH TABLE".

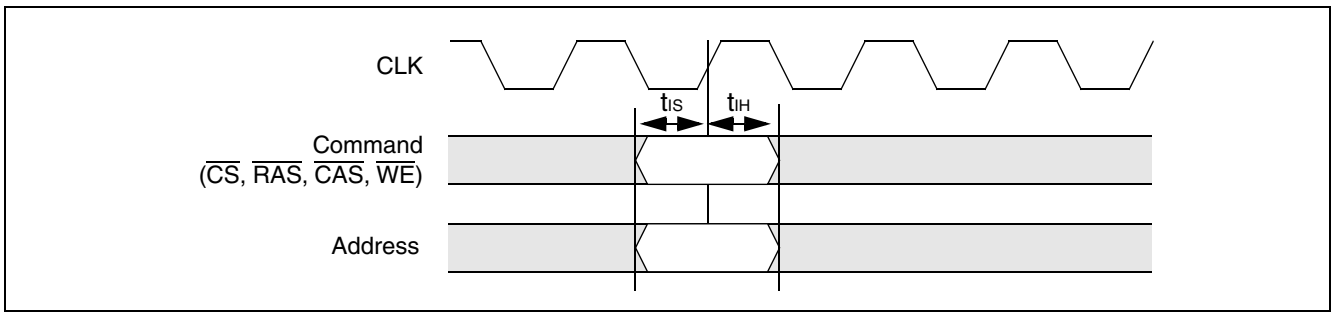
5. Bank Address Inputs (BA0, BA1)

BA0 and BA1 define to which bank an ACTIVE (ACT), READ (READ, READA), WRITE (WRIT, WRITA) or PRECHARGE (PRE, PALL) command is being applied.

6. Address Inputs (A0 to A11)

Address input selects an arbitrary location of a total of 2,097,152 words of each memory cell matrix. Total 21 address input signals are required to decode such a matrix. Row Address (RA) is input from A0 to A11 and Column Address (CA) is input from A0 to A8. Row addresses are latched with ACTIVE(ACT) command, and Column addresses and Auto Precharge (AP) bit are latched with Read (READ or READA) or Write command (WRIT or WRITA).

• Command and address inputs setup and hold time



7. Input/Output Data Mask (DQM0 to DQM3)

DQM is an input mask signal for write data and output enable signal for read data. Input data is masked when DQM is sampled High on the rising edge of CLK along with input data. Output buffer is disable after 2 clocks from DQM is sampled High on the rising edge of CLK. DQM0, DQM1, DQM2 and DQM3 correspond to DQ[7:0], DQ[15:8], DQ[23:16] and DQ[31:24] respectively. Refer to the “DQ/DQM Correspondence Table”.

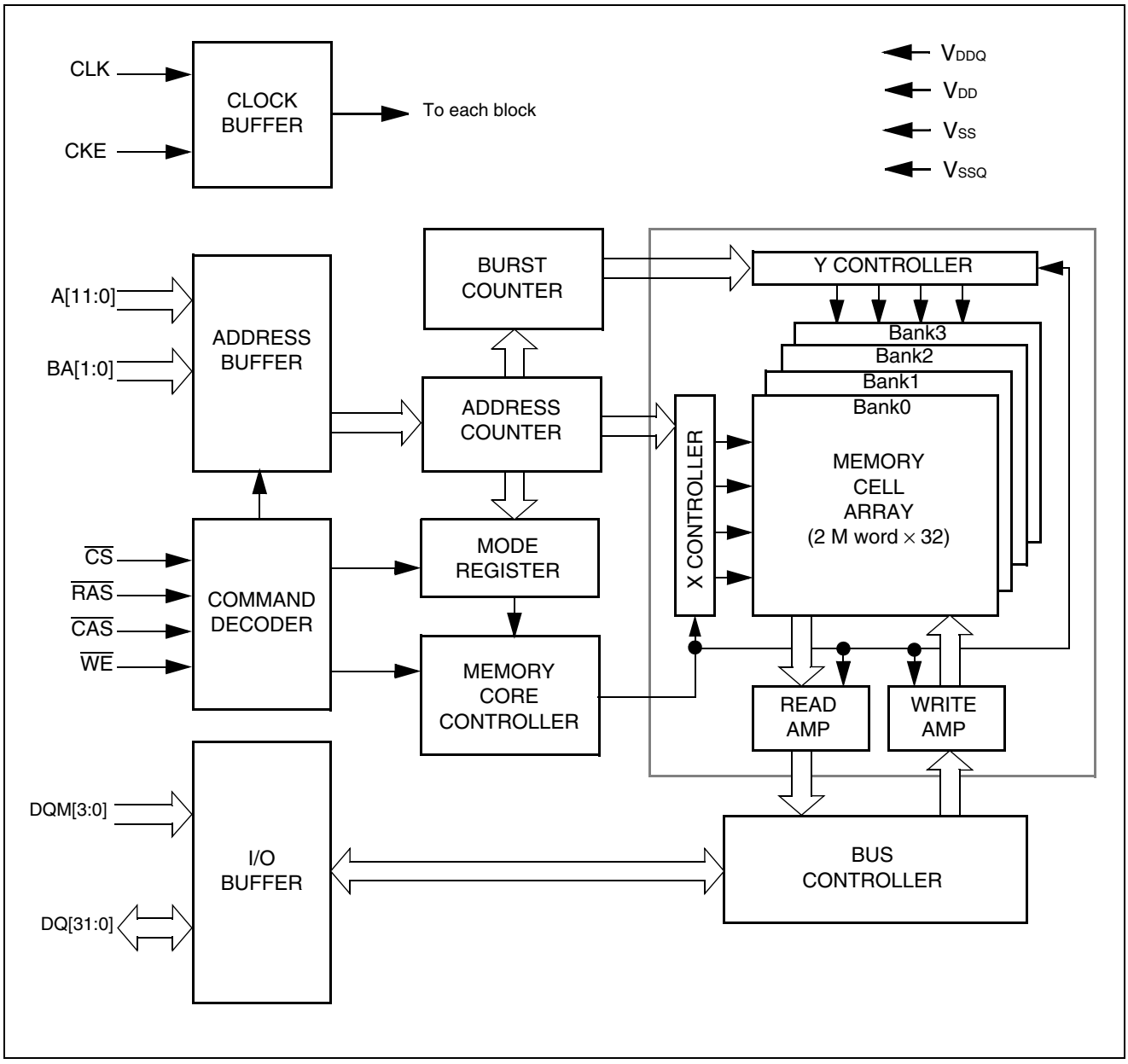
8. Data Bus Input / Output (DQ0 to DQ31)

DQ is data bus input / output signal.

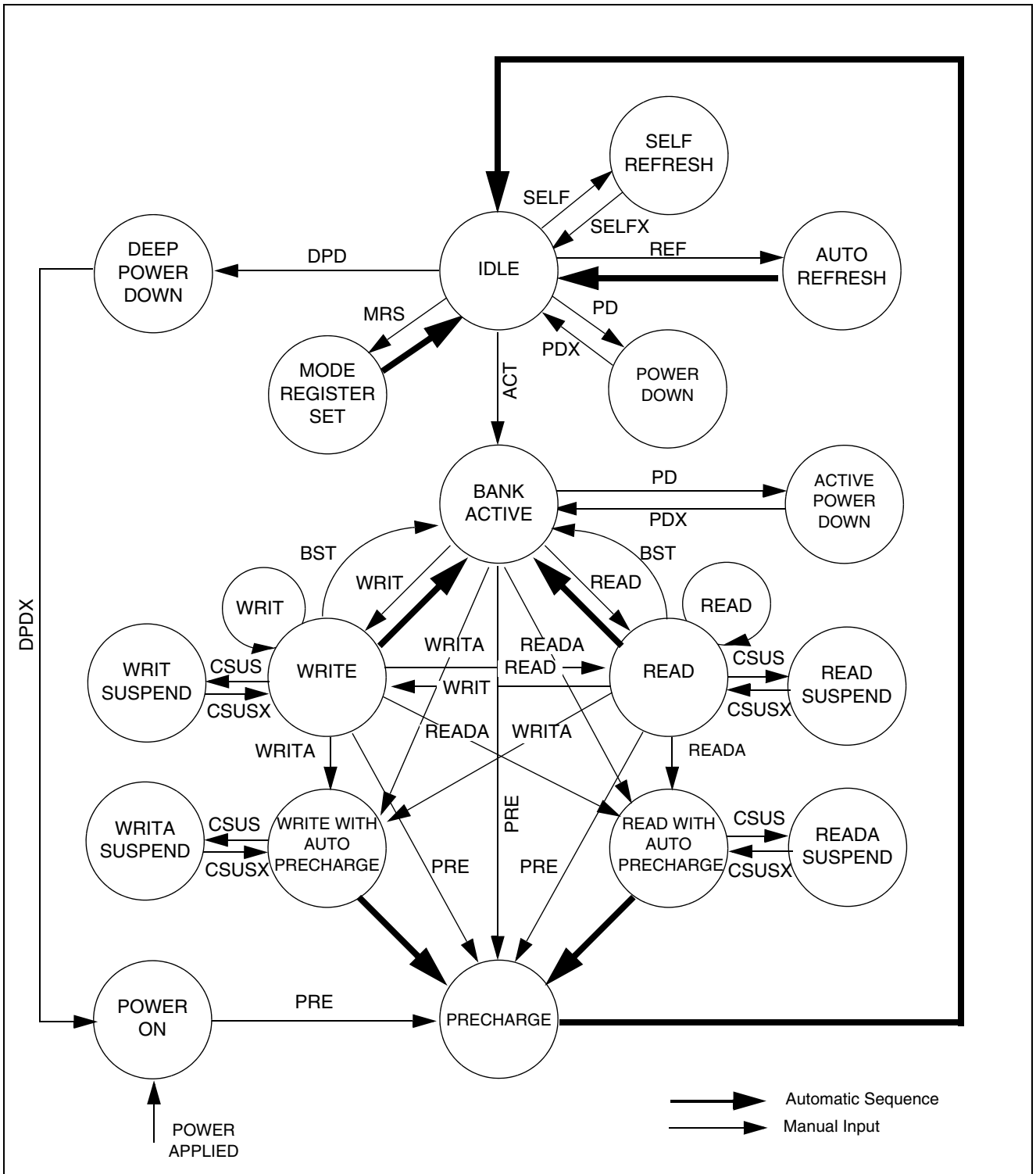
• DQ/DQM Correspondence Table

DQ	DQM
DQ[7:0]	DQM0
DQ[15:8]	DQM1
DQ[23:16]	DQM2
DQ[31:24]	DQM3

■ BLOCK DIAGRAM



■ SIMPLIFIED STATE DIAGRAM



Note: "■SIMPLIFIED STATE DIAGRAM" is based on the single bank operation.
State transition of multi bank operation are not described in all detail.

■ FUNCTIONAL DESCRIPTION

1. Power Up Initialization

This device internal condition after power-up will be undefined. The following Power up initialization sequence must be performed to start proper device operation.

1. Apply power (V_{DD} should be applied before or in parallel with V_{DDQ}) and start clock. Attempt to maintain either NOP or DESL command at the input.
2. Maintain stable power, stable clock, and NOP or DESL condition for a minimum of 300 µs.
3. Precharge all banks by PRECHARGE (PRE) or PRECHARGE ALL (PALL) command.
4. Assert minimum of 2 AUTO REFRESH (REF) commands.
5. Program the Mode Register by MODE REGISTER SET (MRS) command.
6. Program the Extended Mode Register by MODE REGISTER SET (MRS) command.

In addition, CKE must be High to ensure that output is High-Z state. The Mode Register and Extended Mode Register can be set before 2 Auto refresh commands (REF).

2. Mode Register

The Mode Register is used to configure the type of device function among optional features. This device has 2 Mode Registers, Mode Register and Extended Mode Register. Mode Registers can be programmed by MODE REGISER SET (MRS) command. Refer to the “Mode Register Table” in “■FUNCTIONAL DESCRIPTION”.

Mode Register Table

Mode Register

BA_1	BA_0	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	ADDRESS
0	0	0	0	0	0	0	CL			0	BL			Mode Register

A_6	A_5	A_4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A_2	A_1	A_0	Burst Length
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Full Column

Extended Mode Register

BA_1	BA_0	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	ADDRESS
0	1	0	0	0	0	0	PDS	DS	0	0	0	0	0	Extended Mode Register

A_6	Pre Driver Strength
0	Fast
1	Slow

A_5	Driver Strength
0	Normal
1	Weak

3. Burst Length (BL)

Burst Length (BL) is the number of word to be read or write as the result of a single READ or WRITE command. It can be set on 1, 2, 4, 8, Full Column words boundary through Mode Register. The burst type is sequential that is incremental decoding scheme within a boundary address to be determined by burst length. Device internal address counter assigns + 1 to the previous address until reaching the end of boundary address and then wrap round to least significant address (= 0). When BL = Full Column is set, burst read or write operation will continue until interrupted by new READ or WRIT or PRE or BST commands. Therefore Auto precharge option is illegal when the BL = Full Column is selected.

Burst Length	Starting Column Address				Burst Address Sequence (Hexadecimal)
	A_3	A_2	A_1	A_0	
2	X	X	X	0	0 - 1
	X	X	X	1	1 - 0
4	X	X	0	0	0 - 1 - 2 - 3
	X	X	0	1	1 - 2 - 3 - 0
	X	X	1	0	2 - 3 - 0 - 1
	X	X	1	1	3 - 0 - 1 - 2
8	X	0	0	0	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
	X	0	0	1	1 - 2 - 3 - 4 - 5 - 6 - 7 - 0
	X	0	1	0	2 - 3 - 4 - 5 - 6 - 7 - 0 - 1
	X	0	1	1	3 - 4 - 5 - 6 - 7 - 0 - 1 - 2
	X	1	0	0	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3
	X	1	0	1	5 - 6 - 7 - 0 - 1 - 2 - 3 - 4
	X	1	1	0	6 - 7 - 0 - 1 - 2 - 3 - 4 - 5
	X	1	1	1	7 - 0 - 1 - 2 - 3 - 4 - 5 - 6

4. CAS Latency (CL)

CAS Latency (CL) is the delay between READ command being registered and first read data becoming available during read operation. First read data will be valid after (CL-1) $\times t_{CK} + t_{AC}$ from the CLK rising edge where READ command being latched.

5. Driver Strength (DS)

Driver Strength (DS) is to adjust the driver strength of data output.

6. Pre Driver Strength (PDS)

Pre Driver Strength (PDS) is to adjust the transition time of the data output without changing the output driver impedance.

■ COMMAND TRUTH TABLE

1) Basic Command Truth Table

Command	Symbol	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10 (AP)	A[9:0], A11
DESELECT *1	DESL	H	X	X	X	X	X	X
NO OPERATION *1	NOP	L	H	H	H	X	X	X
BURST TERMINATE *2, *3	BST	L	H	H	L	X	X	X
READ *3, *4	READ	L	H	L	H	V	L	CA
READ with Auto Precharge *3, *4	READA	L	H	L	H	V	H	CA
WRITE *3, *4	WRIT	L	H	L	L	V	L	CA
WRITE with Auto Precharge *3, *4	WRITA	L	H	L	L	V	H	CA
BANK ACTIVE *4, *5	ACT	L	L	H	H	V	RA	
PRECHARGE SINGLE BANK *5, *6	PRE	L	L	H	L	V	L	X
PRECHARGE ALL BANKS *5, *6	PALL	L	L	H	L	X	H	X
AUTO REFRESH *6	REF	L	L	L	H	X	X	X
MODE REGISTER SET *7	MRS	L	L	L	L	V	V	V

Note: V = Valid, L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, RA = Row Address, CA = Column Address
All commands are assumed to be valid state transitions and latched on the rising edge of CLK. CKE assumes to be kept High.

*1: NOP and DESL commands have the same functionality. Unless specifically noted, NOP will represent both NOP and DESL command in later description.

*2: When the current state is IDLE and CKE=L, BST command will represent DPD command. Refer to the “2) CKE Command Truth Table” in the “■ COMMAND TRUTH TABLE”.

*3: BST command can be applied to READ or WRIT. READA and WRITA must not be terminated by BST command.

*4: READ, READA, WRIT and WRITA commands can be issued after the corresponding bank has been activated. Refer to the “■ SIMPLIFIED STATE DIAGRAM”.

*5: ACT command can be issued after corresponding bank has been precharged by PRE or PALL command. Refer to the “■ SIMPLIFIED STATE DIAGRAM”.

*6: REF command can be issued after all banks have been precharged by PRE or PALL command. Refer to the “■SIMPLIFIED STATE DIAGRAM”.

*7: MRS command can be issued after all banks have been precharged and all DQ are in High-Z. Mode Register and Extended Mode Register are selected through BA input. Mode Register and Extended Mode Register must be set by MRS command after power up.

2) CKE Command Truth Table

Current State	Command	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA, A[11:0]
			n-1	n					
READ (READA) or WRIT (WRITA)	CLOCK SUSPEND ENTRY	CSUS	H	L	X	X	X	X	X
CLOCK SUSPEND	CLOCK SUSPEND EXIT	CSUSX	L	H	X	X	X	X	X
IDLE	SELF REFRESH ENTRY *1	SELF	H	L	L	L	L	H	X
SELF REFRESH	SELF REFRESH EXIT *2	SELFX	L	H	L	H	H	H	X
					H	X	X	X	X
IDLE or BANK ACTIVE	POWER DOWN ENTRY *1	PD	H	L	L	H	H	H	X
					H	X	X	X	X
POWER DOWN	POWER DOWN EXIT	PDX	L	H	L	H	H	H	X
					H	X	X	X	X
IDLE	DEEP POWER DOWN ENTRY *1	DPD	H	L	L	H	H	L	X
DEEP POWER DOWN	DEEP POWER DOWN EXIT	DPDX	L	H	L	H	H	H	X
					H	X	X	X	X

Note: V = Valid, L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}

*1: SELF and DPD commands can be issued after all banks have been precharged and all DQ are in High-Z.

*2: CKE should be held High more than t_{REFC} period after SELFX.

3) Single Bank Operation

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function
IDLE	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *1
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACT	Bank Active
	L	L	H	L	BA, AP	PRE/PALL	NOP *2
	L	L	L	H	X	REF	Auto Refresh *3
	L	L	L	L	MODE	MRS	Mode Register Set *3, *4
BANK ACTIVE	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	
	L	H	L	H	BA, CA, AP	READ/READA	Start Read; Determine AP
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Start Write; Determine AP
	L	L	H	H	BA, RA	ACT	Illegal *1
	L	L	H	L	BA, AP	PRE/PALL	Precharge; Determine Precharge Type
	L	L	L	H	X	REF	Illegal
	L	L	L	L	MODE	MRS	

(Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function
READ	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Burst Terminate → BANK ACTIVE
	L	H	L	H	BA, CA, AP	READ/READA	Interrupt burst read by new burst read; Determine AP
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Interrupt burst read by new burst write; Determine AP *5
	L	L	H	H	BA, RA	ACT	Illegal *1
	L	L	H	L	BA, AP	PRE/PALL	Terminate burst read by precharge → IDLE
	L	L	L	H	X	REF	Illegal
	L	L	L	L	MODE	MRS	
WRITE	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Burst terminate → BANK ACTIVE
	L	H	L	H	BA, CA, AP	READ/READA	Interrupt burst read by new burst read; Determine AP *5
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Interrupt burst write by new burst write; Determine AP
	L	L	H	H	BA, RA	ACT	Illegal *1
	L	L	H	L	BA, AP	PRE/PALL	Terminate burst write by precharge → IDLE
	L	L	L	H	X	REF	Illegal
	L	L	L	L	MODE	MRS	

(Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function
READ WITH AUTO PRECHARGE	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *1
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACT	
	L	L	H	L	BA, AP	PRE/PALL	
	L	L	L	H	X	REF	Illegal
	L	L	L	L	MODE	MRS	
WRITE WITH AUTO PRE-CHARGE	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *1
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACT	
	L	L	H	L	BA, AP	PRE/PALL	
	L	L	L	H	X	REF	Illegal
	L	L	L	L	MODE	MRS	
Precharging	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *1
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACT	
	L	L	H	L	BA, AP	PRE/PALL	NOP *2
	L	L	L	H	X	REF	Illegal
	L	L	L	L	MODE	MRS	

(Continued)

(Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function
Bank Activating	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal *2
	L	H	L	H	BA, CA, AP	READ/READA	
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACT	
	L	L	H	L	BA, AP	PRE/PALL	
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	
Refreshing/ Mode Register Setting	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	X	X	READ/READA/ WRIT/WRITA	
	L	L	X	X	X	ACT/PRE/PALL/ REF/SELF/MRS	

RA = Row Address BA = Bank Address
CA = Column Address AP = Auto Precharge

Note: Assuming CKE = H during the previous clock cycle and the current clock cycle. After illegal commands are asserted, following command and stored data should not be guaranteed.

*1: Illegal to bank in the specified state. Command entry may be legal depending on the state of bank selected by BA.

*2: NOP to bank in precharging or in idle state. Bank in active state may be precharged depending on BA.

*3: Illegal if any bank is not idle.

*4: MRS command should be issued on condition that all DQ are in High-Z.

*5: Must avoid the bus contention.

■ BANK OPERATION COMMAND TABLE

Minimum clock latency or delay time for single bank operation

1st Command	2nd Command (same bank)										
	MRS	ACT	READ	READA	WRIT	WRITA	BST	PRE	PALL	REF	SELF
MRS	t_{MRD}	t_{MRD}	—	—	—	—	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}
ACT	—	—	t_{RCD}	*4 t_{RCD}	t_{RCD}	*5 t_{RCD}	—	t_{RAS}	t_{RAS}	—	—
READ	—	—	1	1	*6 1	*6 1	1	*3 1	*3 1	—	—
READA	*1, *2 BL + t_{RP}	BL + t_{RP}	—	—	—	—	—	BL + t_{RP}	BL + t_{RP}	*1 BL + t_{RP}	*1, *2 BL + t_{RP}
WRIT	—	—	*6 1	*6 1	1	1	1	*3 t_{DPL}	*3 t_{DPL}	—	—
WRITA	*1, *2 BL-1 + t_{DAL}	BL-1 + t_{DAL}	—	—	—	—	—	BL-1 + t_{DAL}	BL-1 + t_{DAL}	*1 BL-1 + t_{DAL}	*1, *2 BL-1 + t_{DAL}
PRE	*1, *2 t_{RP}	t_{RP}	—	—	—	—	t_{RP}	1	1	*1 t_{RP}	*1, *2 t_{RP}
PALL	*2 t_{RP}	t_{RP}	—	—	—	—	t_{RP}	1	1	t_{RP}	*2 t_{RP}
REF	t_{REFC}	t_{REFC}	—	—	—	—	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}
SELFX	t_{REFC}	t_{REFC}	—	—	—	—	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}

“—” : illegal

*1: Assume all banks are in IDLE state.

*2: Assume output is in High-Z state.

*3: Assume t_{RAS} (Min.) is satisfied.

*4: ACT to READA interval must be longer than t_{RAS} - BL.

*5: ACT to WRITA interval must be longer than t_{RAS} - (BL - 1 + t_{DPL}).

*6: Assume no I/O conflict.

Minimum clock latency or delay time for multi bank operation

		2nd Command (other bank)										
		MRS	**ACT**	**READ**	**READA**	**WRIT**	**WRITA**	**BST**	**PRE**	**PALL**	**REF**	**SELF**
1st Command	**MRS**	t_{MRD}	t_{MRD}	—	—	—	—	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}
	ACT	—	t_{RRD}	1	1	1	1	1	1	t_{RAS}	—	—
	READ	—	*1, *3 1	1	1	*5 1	*5 1	1	1	1	—	—
	READA	*1, *2 BL+t_{RP}	*1, *3 1	1	1	*5 1	*5 1	—	1	BL+ t_{RP}	*1 BL + t_{RP}	*1 BL+ t_{RP}
	WRIT	—	*1, *3 1	*5 1	*5 1	1	1	1	1	*3 t_{DPL}	—	—
	WRITA	*1 BL-1 + t_{DAL}	*1, *3 1	*5 1	*5 1	1	1	—	1	*3 BL-1 + t_{DAL}	*1 BL-1 + t_{DAL}	*1 BL-1 + t_{DAL}
	PRE	*1, *2 t_{RP}	*1, *3 1	1	1	1	1	1	1	1	*1 t_{RP}	*1, *2 t_{RP}
	PALL	*1 t_{RP}	t_{RP}	—	—	—	—	t_{RP}	1	1	t_{RP}	t_{RP}
	REF	t_{REFC}	t_{REFC}	—	—	—	—	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}
	SELFX	t_{REFC}	t_{REFC}	—	—	—	—	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}

“ — ” : illegal

*1: Assume other bank is in IDLE state.

*2: Assume output is in High-Z state.

*3: Assume t_{RRD} is satisfied.

*4: Assume t_{RAS} is satisfied.

*5: Assume no I/O conflict.

■ COMMAND DESCRIPTION

1. DESELECT (DESL)

When $\overline{CS}$ is High at the CLK rising edge, all input signals are neglected. Internal operation such as burst cycle is held.

2. NO OPERATION (NOP)

NOP disables address and data input and internal operation such as burst cycle is held.

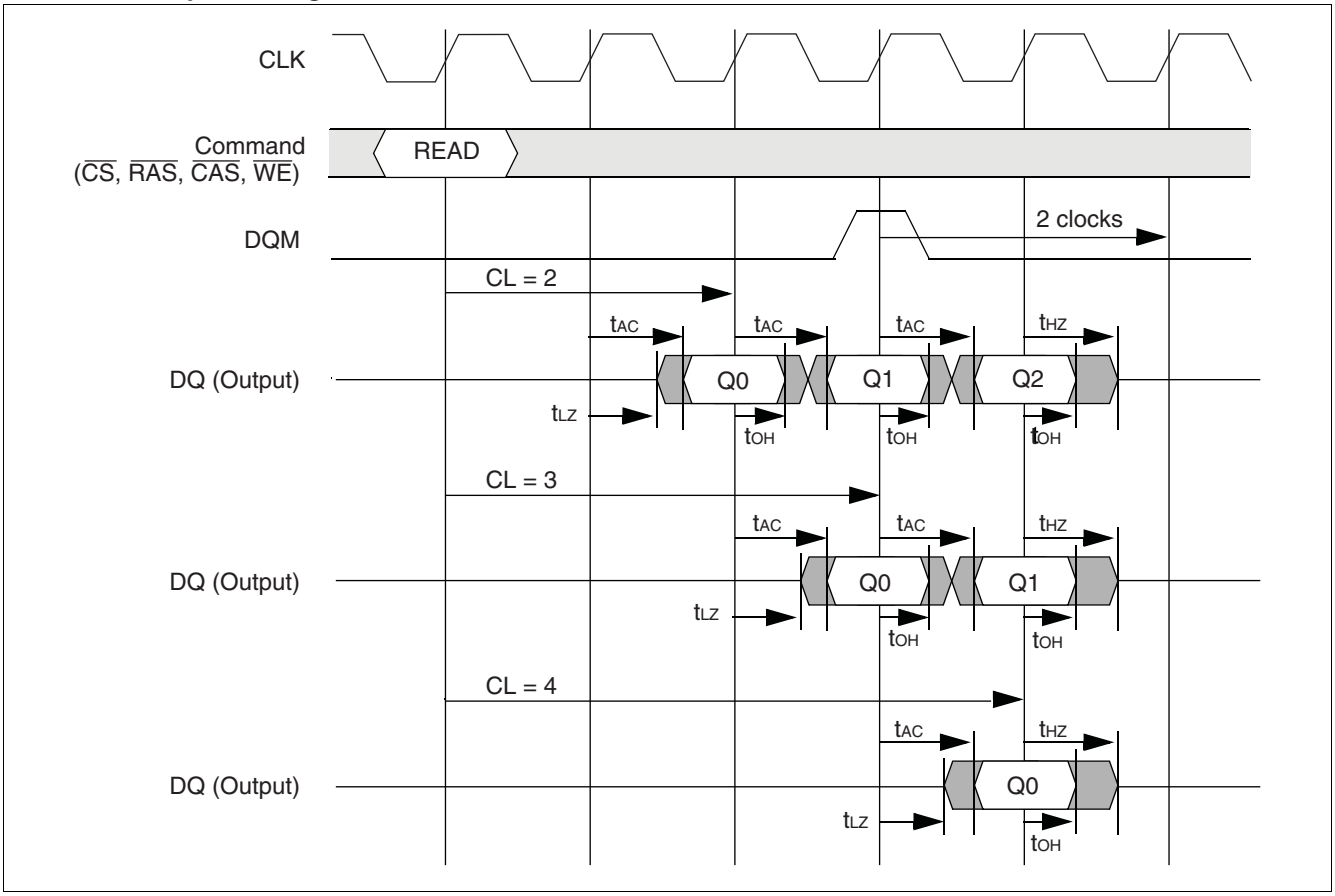
3. BANK ACTIVE (ACT)

ACT activates the bank selected by BA and latch the row address through A0 to A11.

4. READ (READ)

READ initiates burst read operation to an activated row address. Address inputs of A[8:0] determine starting column address and A10 determines whether Auto Precharge is used or not. Read data appears on the DQs subject to DQM input logic level inputs two clocks earlier. If a given signal on DQM is registered Low, the corresponding data will be valid data. And if a given signal on DQM is registered High, the corresponding data will be High-Z two clocks later.

Read Data Output Timing



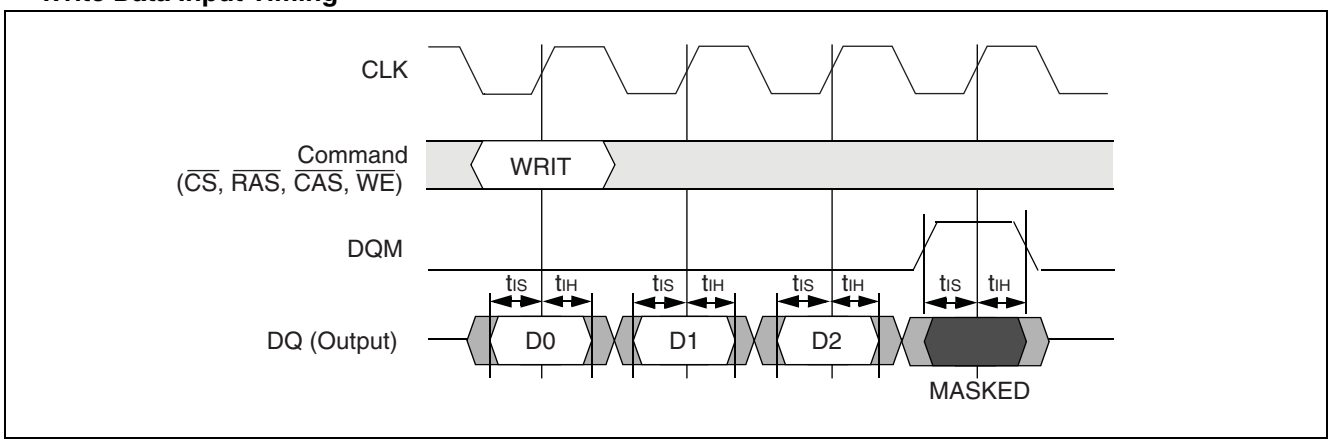
5. READ with Auto Precharge (READA)

READA commands can be issued by READ command with AP (A10) = H. Auto Precharge is a feature which precharge the activated bank after the completion of burst read operation. The t_{RAS} is defined from between ACTIVE (ACT) command to the internal precharge which starts after BL from READA command. READ with Auto Precharge operation should not be interrupted by subsequent READ, READA, WRIT, WRITA commands. Next ACTIVE (ACT) command can be issued after BL + t_{RP} after READA command.

6. WRITE (WRIT)

WRIT initiates burst write operation to an active row address. Address inputs of A[8:0] determine starting column address and AP(A10) determines whether Auto Precharge is used or not. The input data appearing on DQ is written into memory cell array subject to the DQM input logic level appearing coincident with the input data. If a given signal on DQM is registered Low, the corresponding data will be written into the cell array. And if a given signal on DQM is registered High, the corresponding data will be masked and write will not be executed to that byte.

Write Data Input Timing



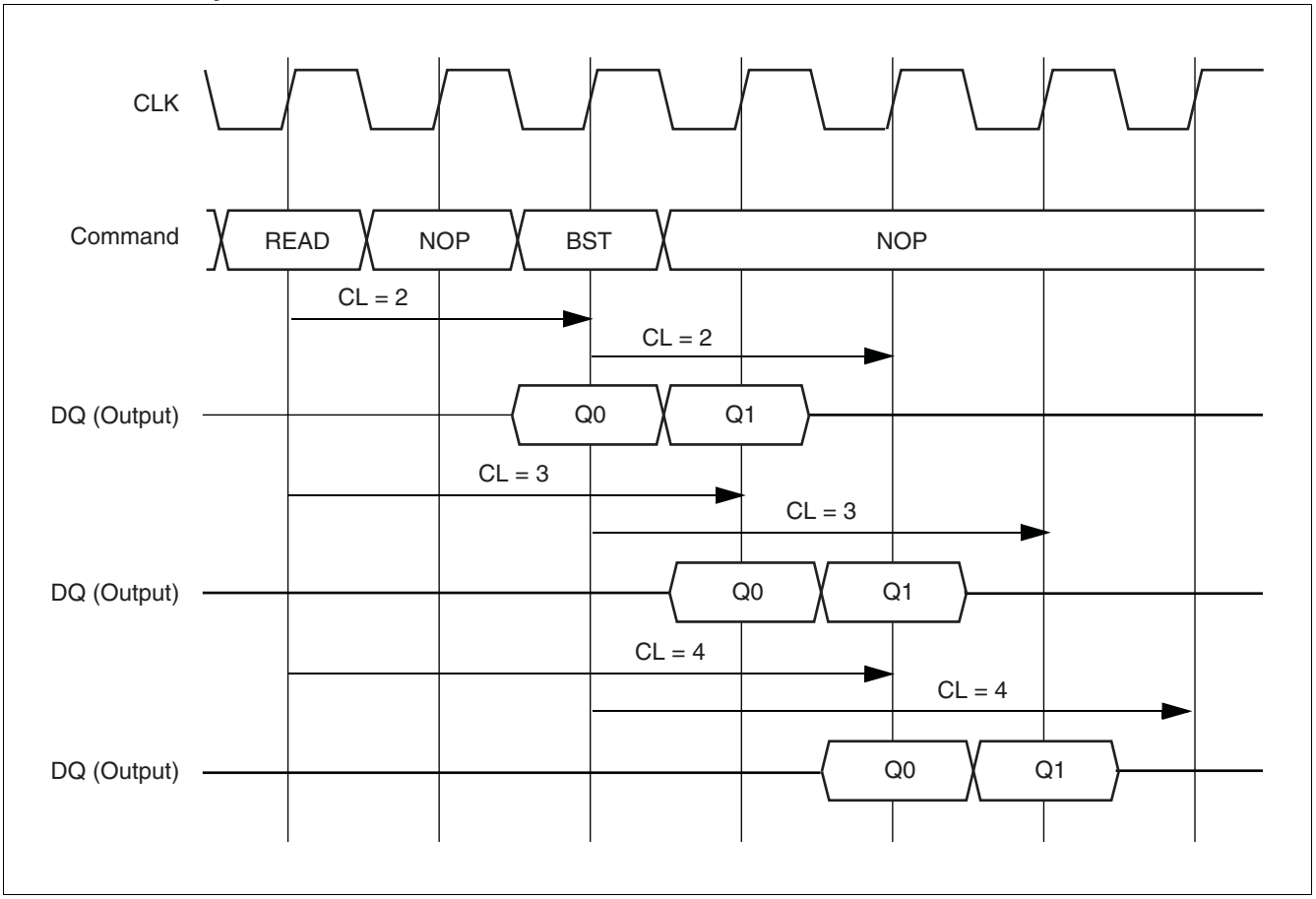
7. WRITE with Auto Precharge (WRITA)

WRITA command can be issued by WRIT command with AP (A10) = H. Auto Precharge is a feature which precharge the activated bank after the completion of burst write operation. The t_{RAS} is defined from between ACTIVE (ACT) command to the internal precharge which starts after BL - 1 + t_{DPL} from WRITA command. WRIT with Auto Precharge operation should not be interrupted by subsequent READ, READA, WRIT, WRITA commands. Next ACTIVE (ACT) command can be issued after BL - 1 + t_{DAL} after WRITA command.

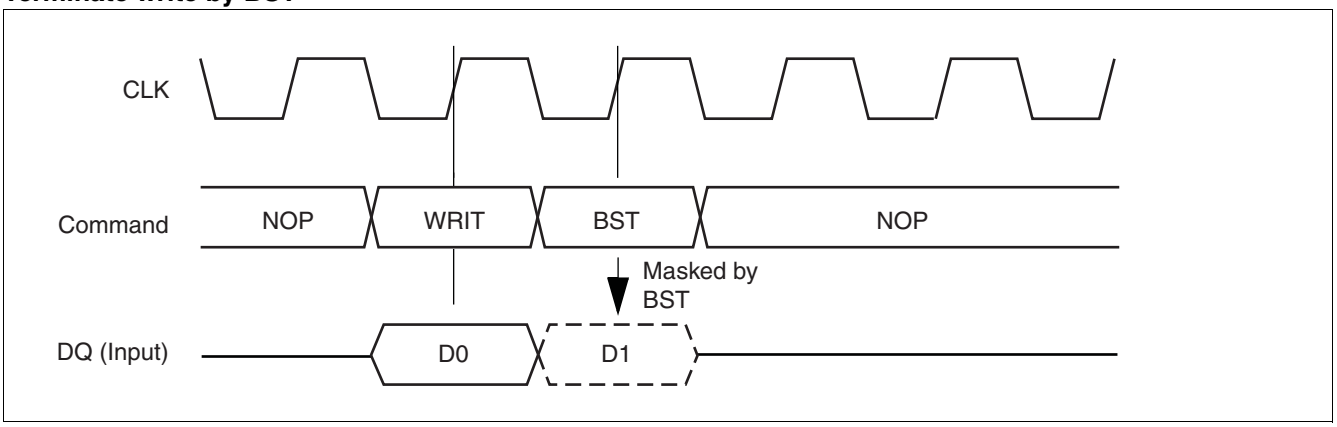
8. BURST TERMINATE (BST)

BST terminates the burst read or write operation. When a burst read is terminated by BST command, the data output will be in High-Z after CAS latency from the BST command. When a burst write is terminated by BST command, the data input coincident with BST command will be masked.

Terminate read by BST



Terminate write by BST



9. PRECHARGE SINGLE BANK (PRE)

PRECHARGE SINGLE BANK (PRE) command starts precharge operation for a bank selected by BA. A selected bank will be in IDLE state after specified time duration of t_{RP} from PRE command. A10 determines whether one or all banks are precharged. If AP(A10) = L, a bank to be selected by BA is precharged.

10. PRECHARGE ALL BANK (PALL)

PRECHARGE ALL BANK (PALL) command starts precharge operation for all banks. All banks will be in IDLE state after specified time duration of t_{RP} from PALL command. A10 determines whether one or all banks are precharged. If AP(A10) = H, all banks are precharged and BA input is a “don't care”.

11. AUTO REFRESH (REF)

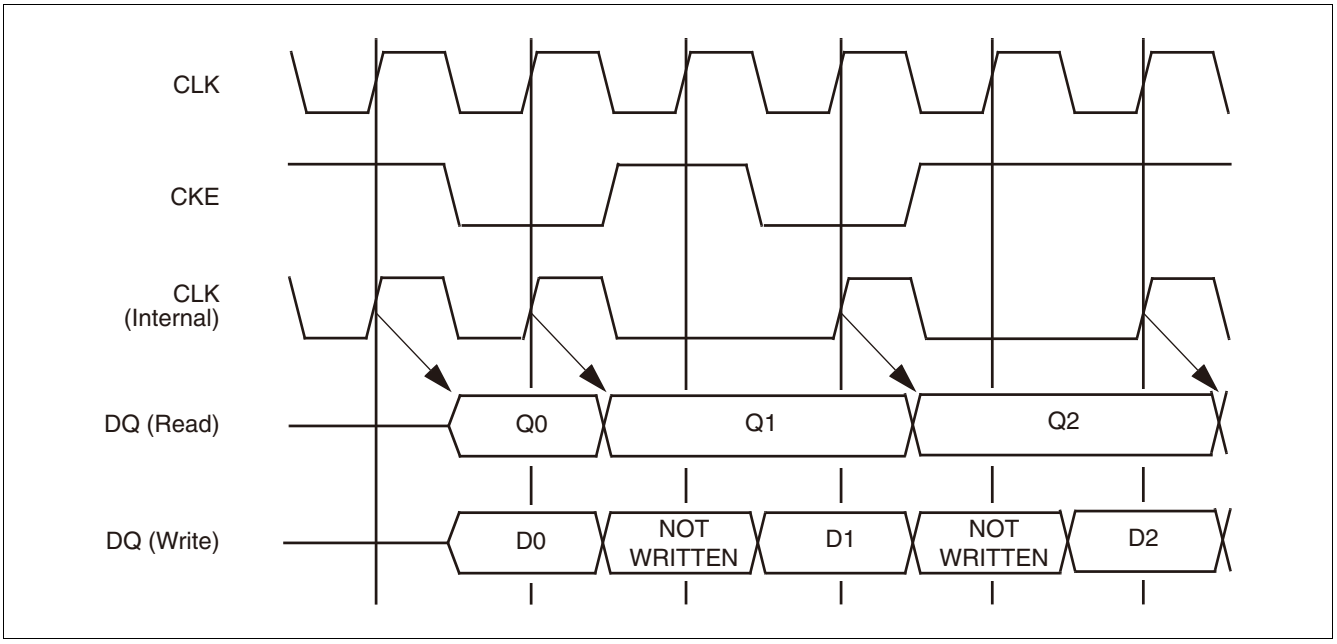
AUTO REFRESH (REF) command starts internal refresh operation which uses the internal refresh address counter. All banks must be precharged prior to the Auto refresh command. Data retention capability depends on the Junction Temperature (Tj). Total 4,096 AUTO REFRESH (REF) commands must be asserted within the following refresh period of t_{REF}.

Tj Max (°C)	t_{REF} (ms)
+ 105	16
+ 125	4

12. CLOCK SUSPEND (CSUS)

CLOCK SUSPEND (CSUS) command is used to suspend the internal burst counter. Clock Suspend mode can be entry by CKE = L during burst read or write operation. When burst read operation is suspended, output data remain the previous data depending on the internal clock. When burst write operation is suspended, input data is not written. Clock suspend mode can be exit by CKE = H.

CLOCK SUSPEND MODE



13. SELF REFRESH ENTRY (SELF)

SELF REFRESH ENTRY (SELF) commands can be issued by AUTO REFRESH (REF) command in conjunction with CKE = Low after last read data has been appeared on DQ. During Self Refresh mode, stored data can be retained without external clocking and all inputs except for CKE will be “don't care”. Self refresh mode can be used when Tj is less than + 85°C. Auto Refresh must be issued to retain data when Tj is greater than + 85 °C.

14. SELF REFRESH EXIT (SELFX)

To exit self refresh mode, apply minimum t_{IS} after CKE brought High, and then the NO OPERATION command (NOP) or the DESELECT command (DESL) should be asserted within one t_{REFC} period. CKE should be held High within one t_{REFC} period after t_{IS}. Refer to the "(15) Self Refresh Entry and Exit" in "■TIMING DIAGRAMS" for the detail. It is recommended to assert an AUTO REFRESH command just after the t_{REFC} period to avoid the violation of refresh period.

15. MODE REGISTER SET (MRS)

MODE REGISTER SET (MRS) commands to program the mode registers. Once a mode register is programmed, the contents of the register will be held until re-programmed by another MRS command. MRS command should only be issued on conditions that all DQs are in High-Z and all banks are in IDLE state. The contents of the mode registers is undefined after the power-up and Deep Power Down Exit. Therefore MRS must be issued to set each content of mode registers after initialization. Refer to the "Power Up Initialization" in "■FUNCTIONAL DESCRIPTION".

16. POWER DOWN ENTRY (PD)

POWER DOWN ENTRY (PD) commands to drive the device in Power Down mode and maintains low power state as long as CKE is kept Low. During Power Down state, all inputs signals are "don't care" except for CKE. Power Down mode must be entered on condition that all DQs are in High-Z and all banks are in IDLE state.

17. POWER DOWN EXIT (PDX)

POWER DOWN EXIT (PDX) commands to resume the device from Power Down mode. Any commands can be detected 1 clock after PDX commands.

18. DEEP POWER DOWN ENTRY (DPD)

DEEP POWER DOWN ENTRY (DPD) commands to drive the device in Deep Power Down mode which is the lowest power consumption but all stored data and the contents of mode registers will be lost. During Deep Power Down state, all inputs signals are "don't care" except for CKE. Deep Power Down mode must be entered on conditions that all DQs are in High-Z and all banks are in IDLE state.

19. DEEP POWER DOWN EXIT (DPDX)

DEEP POWER DOWN EXIT (DPDX) commands to resume the device from Deep Power Down mode. Power up initialization procedure must be performed after DPDX command. Refer to the "Power Up Initialization" in "■ FUNCTIONAL DESCRIPTION".

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage *	V_{DD},V_{DDQ}	− 0.5 to + 2.3	V
Input / Output Voltage *	V_{IN}, V_{OUT}	− 0.5 to + 2.3	V
Short Circuit Output Current	I_{OUT}	± 50	mA
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	− 55 to + 125	°C

* : All voltages are referenced to V_{SS}.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage*1	V_{DD}, V_{DDQ}	1.7	1.8	1.95	V
	V_{SS}, V_{SSQ}	0	0	0	V
Input High Voltage*2	V_{IH}	$V_{DDQ} \times 0.8$	—	V_{DDQ} + 0.3	V
Input Low Voltage*3	V_{IL}	− 0.3	—	0.3	V
Junction Temperature	T_j	− 25	—	+ 125	°C

*1: V_{DDQ} must be less than or equal to V_{DD}.

*2: Maximum DC voltage on input or I/O pins is V_{DDQ} + 0.3 V. During voltage transitions, inputs may positive overshoot to V_{DDQ} + 1.0V for periods of up to 3 ns.

*3: Minimum DC voltage on input or I/O pins is − 0.3 V. During voltage transitions, inputs may negative overshoot to V_{SSQ} − 1.0V for periods of up to 3 ns.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ CAPACITANCE

(T_a = + 25 °C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance, Except for DQM	C_{IN1}	3	—	5	pF
Input Capacitance for DQM	C_{IN2}	5	—	7	pF
I/O Capacitance	$C_{I/O}$	5	—	7	pF

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(Under recommended operating conditions unless otherwise noted)

Parameter	Symbol	Condition		Value		Unit
				Min.	Max.	
Output High Voltage	V_{OH}	I_{OH} = − 0.1 mA		V_{DDQ} − 0.2	—	V
Output Low Voltage	V_{OL}	I_{OL} = 0.1 mA		—	0.2	V
Input Leakage Current	I_{LI}	0 V ≤ V_{IN} ≤ V_{DDQ}, All other pins not under test = 0 V		− 5	5	µA
Output Leakage Current	I_{LO}	0 V ≤ V_{IN} ≤ V_{DDQ}, Data out disabled		− 5	5	µA
Operating Current	I_{DD1}	t_{RC} = t_{RC} min, t_{CK} = t_{CK} min, BL=1, CKE = V_{IH}, $\overline{CS}$ = V_{IH} One bank active, Output pin open, addresses inputs are SWITCHING		—	75	mA
Precharge Standby Current	I_{DD2P}	All banks idle, CKE = V_{IL}, $\overline{CS}$ = V_{IH}, t_{CK} = t_{CK} min, address and control inputs are SWITCHING; data bus inputs are STABLE	Tj ≤ + 105 °C	—	3 *	mA
	I_{DD2N}	All banks idle, CKE = V_{IH}, $\overline{CS}$ = V_{IH}, t_{CK} = t_{CK} min, address and control inputs are SWITCHING; data bus inputs are STABLE		—	15	mA
Operating Burst Current	I_{DD4}	One bank active, BL = 4, t_{CK} = t_{CK} min, Output pin open, Gapless data, address inputs are SWITCHING; 50% data change each burst transfer	Tj ≤ + 105 °C	—	155 *	mA
Auto Refresh Current	I_{DD5}	t_{RC} = t_{RFC} min, t_{CK} = t_{CK} min, CKE = V_{IH}, address and control inputs are SWITCHING; data bus inputs are STABLE		—	120	mA
Self Refresh Current	I_{DD6}	CKE = V_{IL}, $\overline{CS}$ = V_{IL}, address and control inputs are STABLE; data bus inputs are STABLE		—	4	mA
Deep Power Down Current	I_{DD8}	address and control inputs are STABLE; data bus inputs are STABLE		—	20	µA

* : Please contact local Fujitsu representative regarding the maximum value at Tj ≤ + 125 °C.

Notes: • All voltages are referenced to V_{SS}.

- After power on, initialization following power-up timing is required. DC characteristics are guaranteed after the initialization.
- I_{DD} depends on the output termination or load condition, clock cycle rate, signal clocking rate. The specified values are obtained with the output open condition.

2. AC Characteristics

(Under recommended operating conditions unless otherwise noted)*1, *2

Parameter			Symbol	Value		Unit
				Min.	Max.	
DQ Output Access Time from CLK*3, *4			t_{AC}	—	6	ns
DQ Output Hold Time from CLK *3, *4			t_{OH}	2	—	ns
Clock High Level Width *3			t_{CH}	2.5	—	ns
Clock Low Level Width *3			t_{CL}	2.5	—	ns
Clock Cycle Time	CL = 2		t_{CK}	14.8	—	ns
	CL = 3			7.4		
	CL = 4	Tj ≤ + 105 °C		6 *7		
Input Setup Time *3			t_{IS}	2	—	ns
Input Hold Time *3			t_{IH}	1	—	ns
DQ Low-Z Time from CLK *3, *5			t_{LZ}	0	—	ns
DQ High-Z Time from CLK *3, *5			t_{HZ}	—	6	ns
MRS Command Period			t_{MRD}	2	—	t_{CK}
ACT to PRE, PALL Command Period			t_{RAS}	44.4	8000	ns
ACT to ACT Command Period			t_{RC}	66.6	—	ns
REF to ACT, REF Command Period			t_{REFC}	100	—	ns
ACT to READ or WRIT Command Period			t_{RCD}	22.2	—	ns
Precharge Period			t_{RP}	22.2	—	ns
ACT to ACT Command Period			t_{RRD}	14.8	—	ns
Data Input to PRE, PALL Command Period			t_{DPL}	14.8	—	ns
Data Input to ACT, REF Command Period	CL = 2		t_{DAL}	1 CLK + t_{RP}	—	ns
	CL = 3			2 CLK + t_{RP}		
	CL = 4			3 CLK + t_{RP}		
Average Periodic Refresh Interval	Tj ≤ + 105°C		t_{REF}	—	16	ms
	Tj ≤ + 125°C				4	
Transition Time *6			t_T	—	1	ns

* 1: AC characteristics are measured after the Power up initialization procedure.

* 2: $V_{DD} \times 0.5$ is the reference level for 1.8 V I/O for measuring timing of input/output signals.

* 3: If input signal transition time (t_T) is longer than 1 ns; [(t_T/2) – 0.5] ns should be added to t_{AC} (Max), and t_{HZ} (max) spec values, [(t_T/2) – 0.5] ns should be subtracted from t_{LZ} (Min) and t_{OH} (Min) spec values, and (t_T – 1.0) ns should be added to t_{CH} (Min), t_{CL} (Min), t_{IS} (Min) and t_{IH} (Min) spec values.

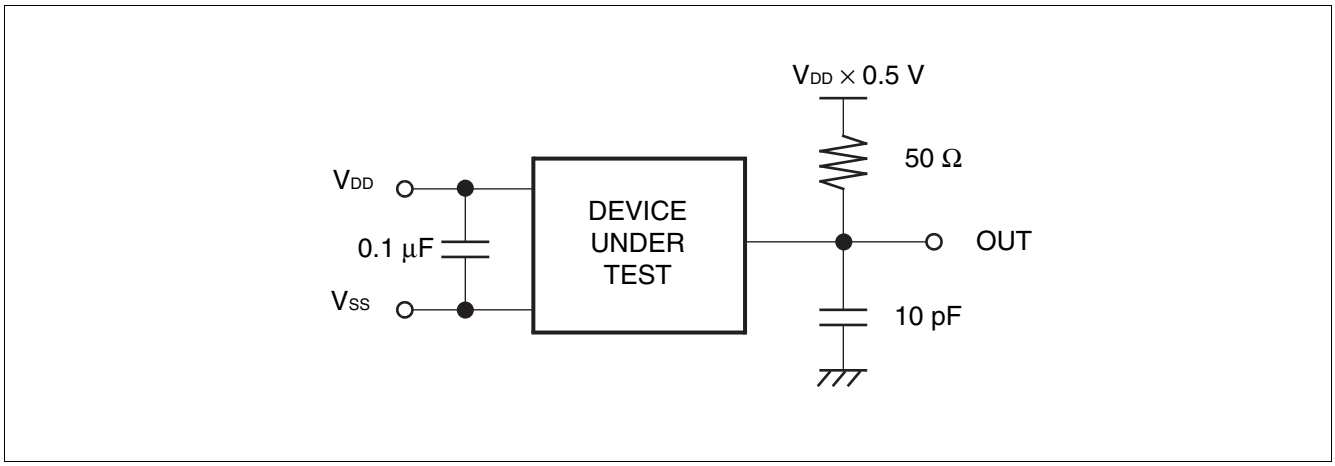
* 4: t_{AC}, t_{LZ} and t_{HZ}, are measured under output load circuit shown in " 3. Measurement Condition of AC Characteristics" in " ■ ELECRTRICAL CHARACTERISTICS" and Driver Strength (DS) = Normal, Pre Driver Strength (PDS) = Fast are assumed.

* 5: Specified where output buffer is no longer driven.

* 6: Transition times are measured between V_{IH} (Min) and V_{IL} (Max).

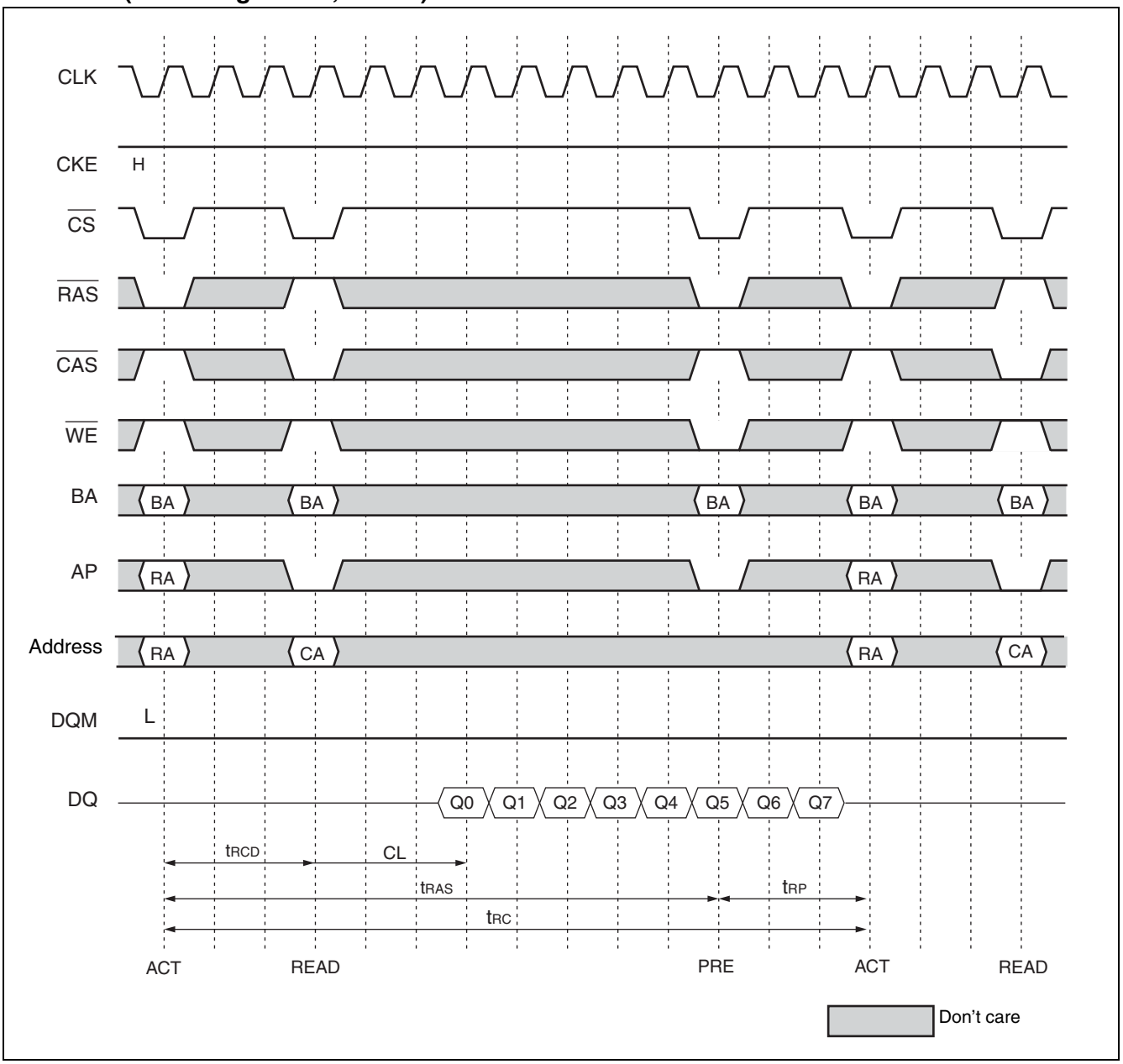
* 7: Please contact local Fujitsu representative regarding minimum value at Tj ≤ + 125 °C.

3. Measurement Condition of AC Characteristics



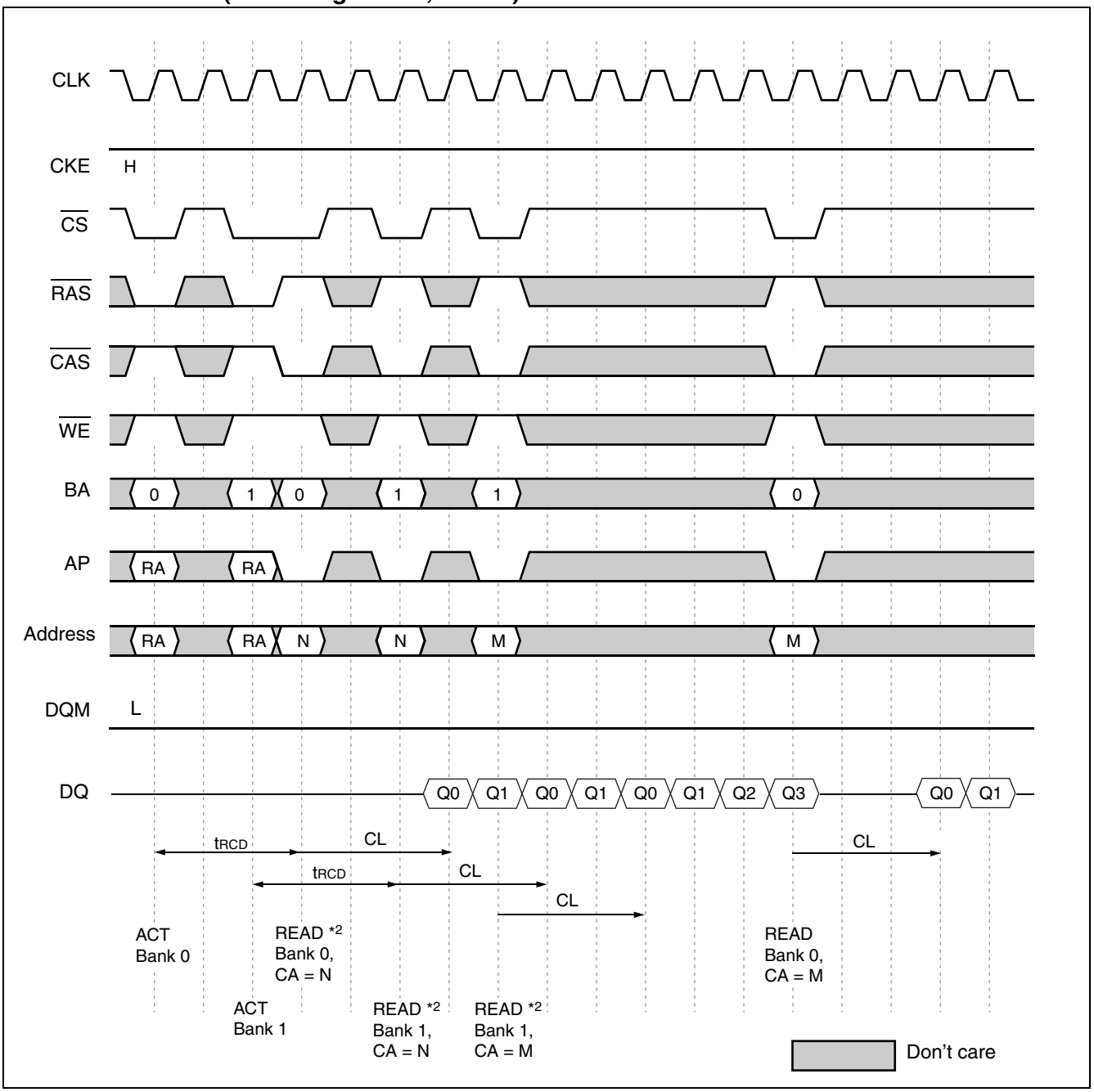
■ TIMING DIAGRAMS

1. Read* (Assuming CL = 3, BL = 8)



* : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

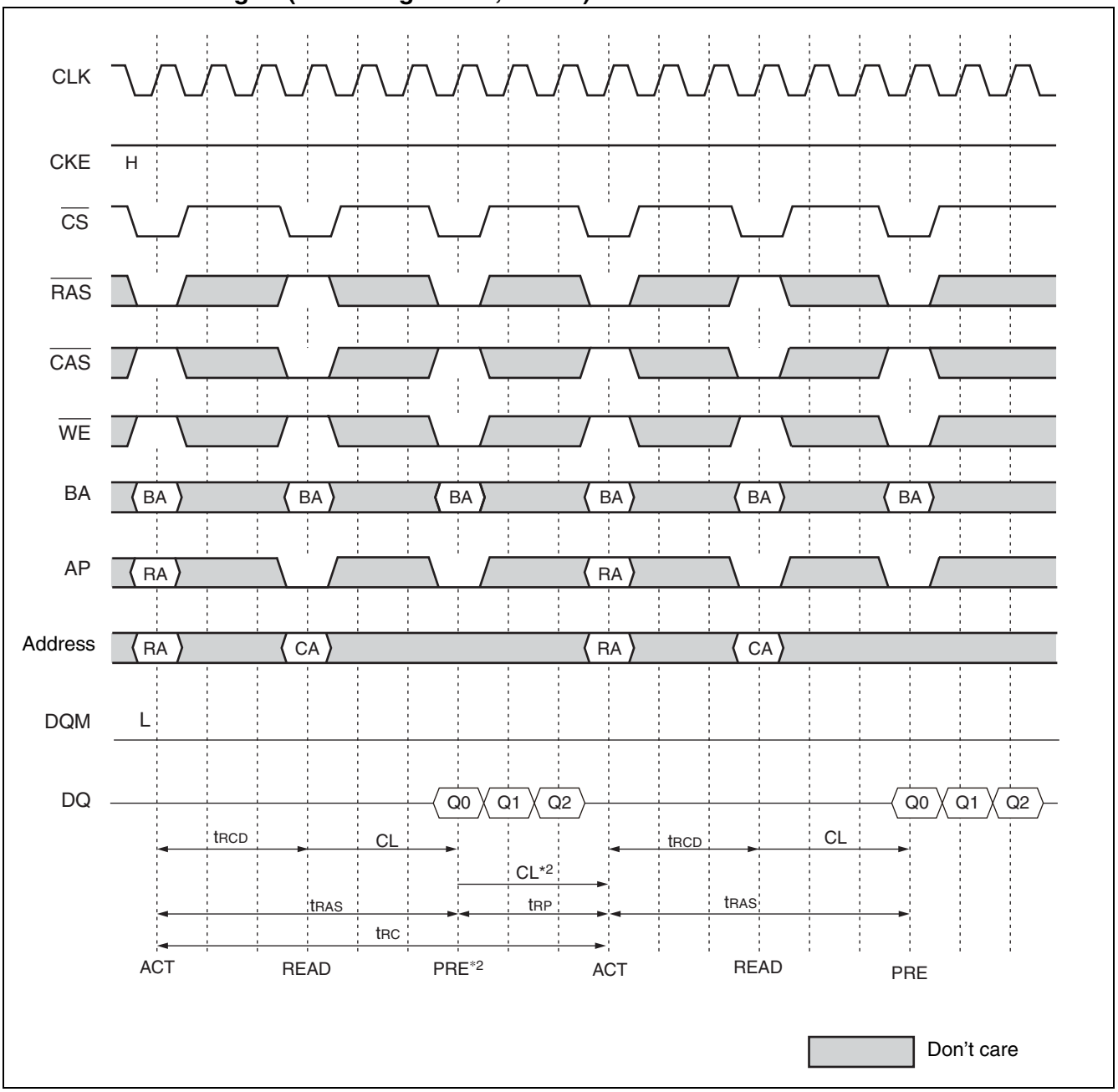
2. Read to Read*1 (Assuming CL = 3, BL = 4)



*1: RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2: Previous burst read can be interrupted by subsequent burst read.

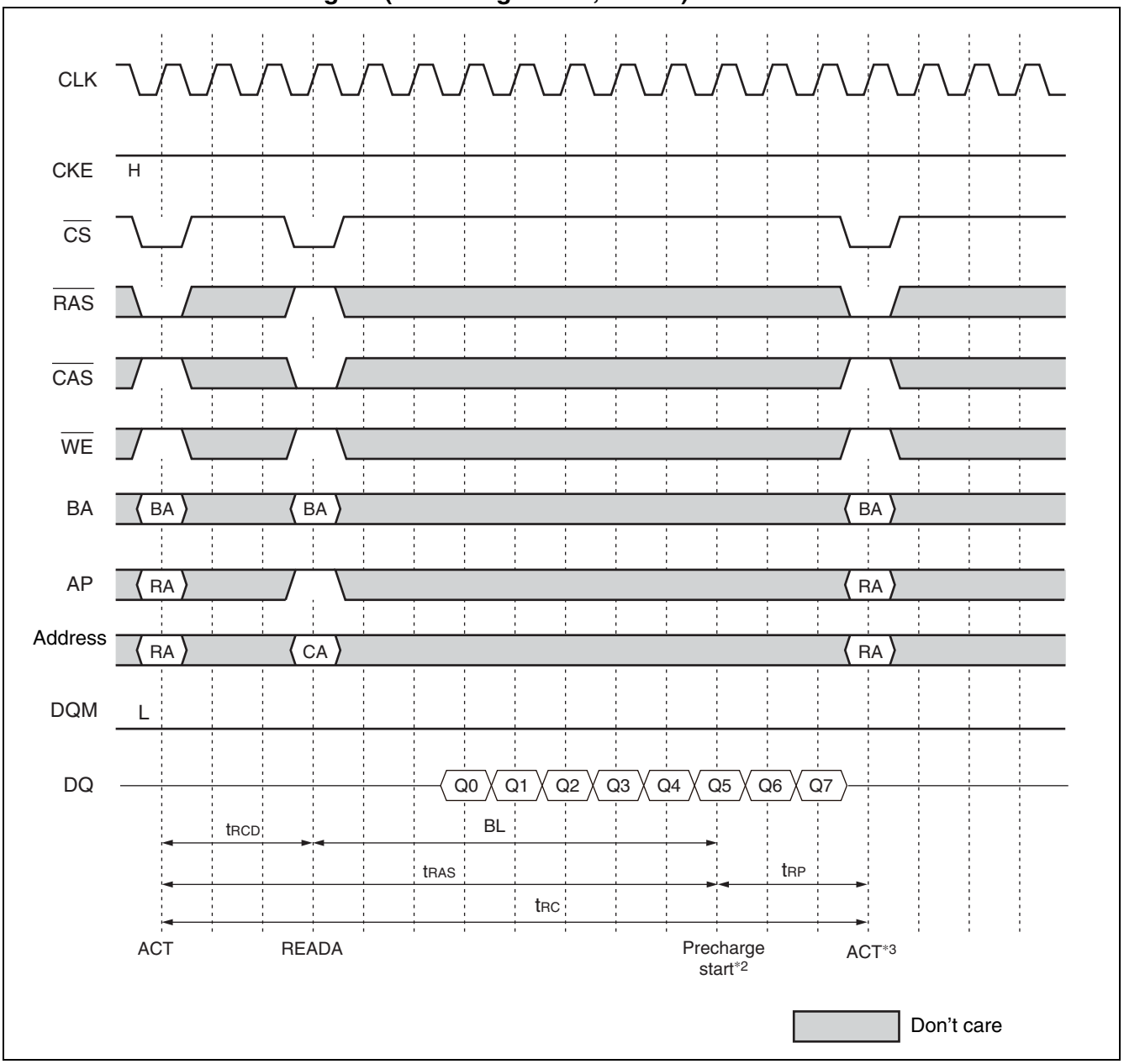
3. Read to Precharge *1(Assuming CL = 3, BL = 8)



*1: RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2: Burst read operation can be terminated by PRE command. All DQ pins become High-Z after CL from PRE command.

4. Read with Auto Precharge *1 (Assuming CL = 3, BL = 8)

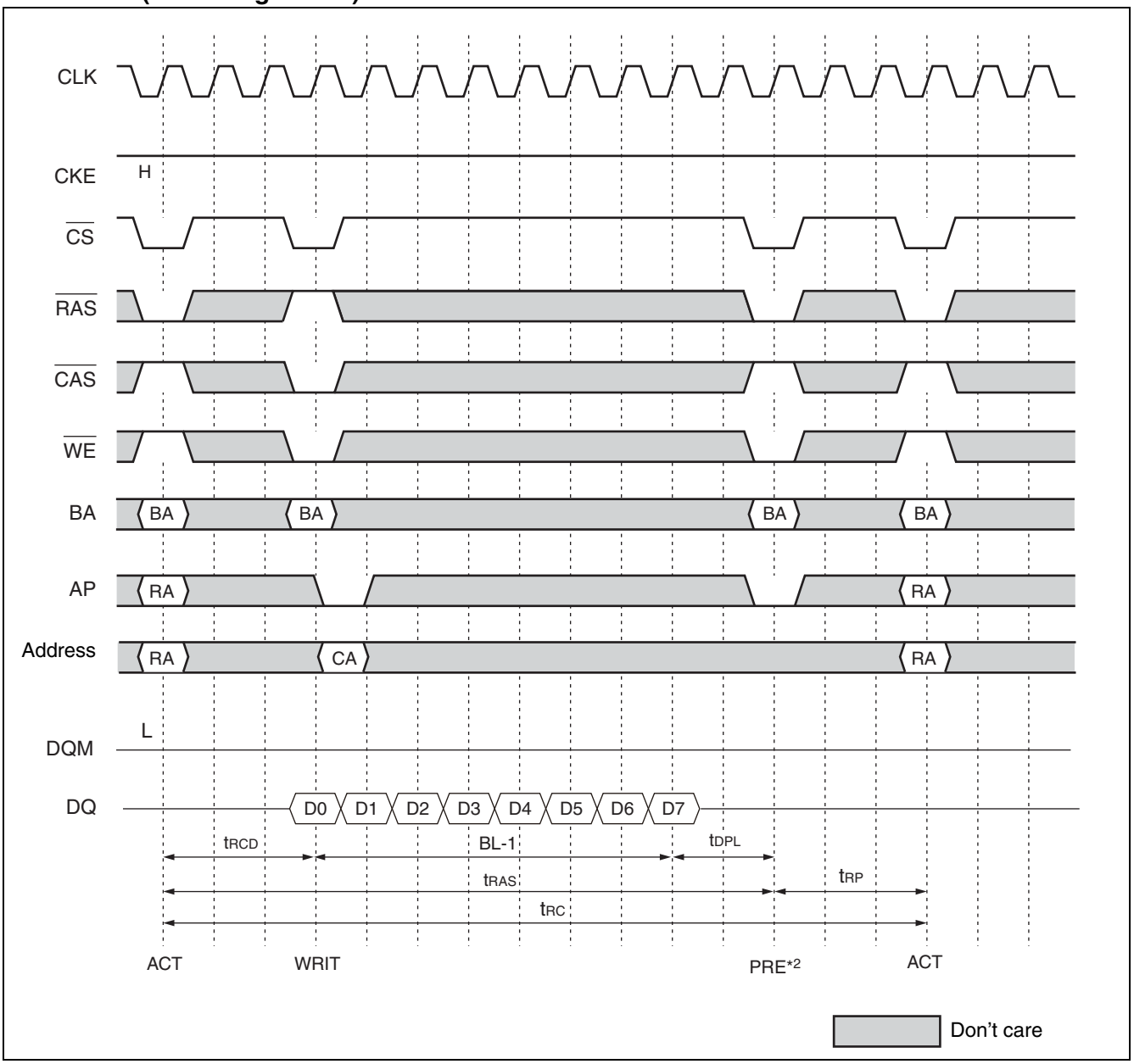


*1: RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2: Internal precharge operation starts after BL from READA command. t_{RAS} must be satisfied.

*3: Next ACT command can be issued after BL + t_{RP} from READA command. t_{RC} must be satisfied.

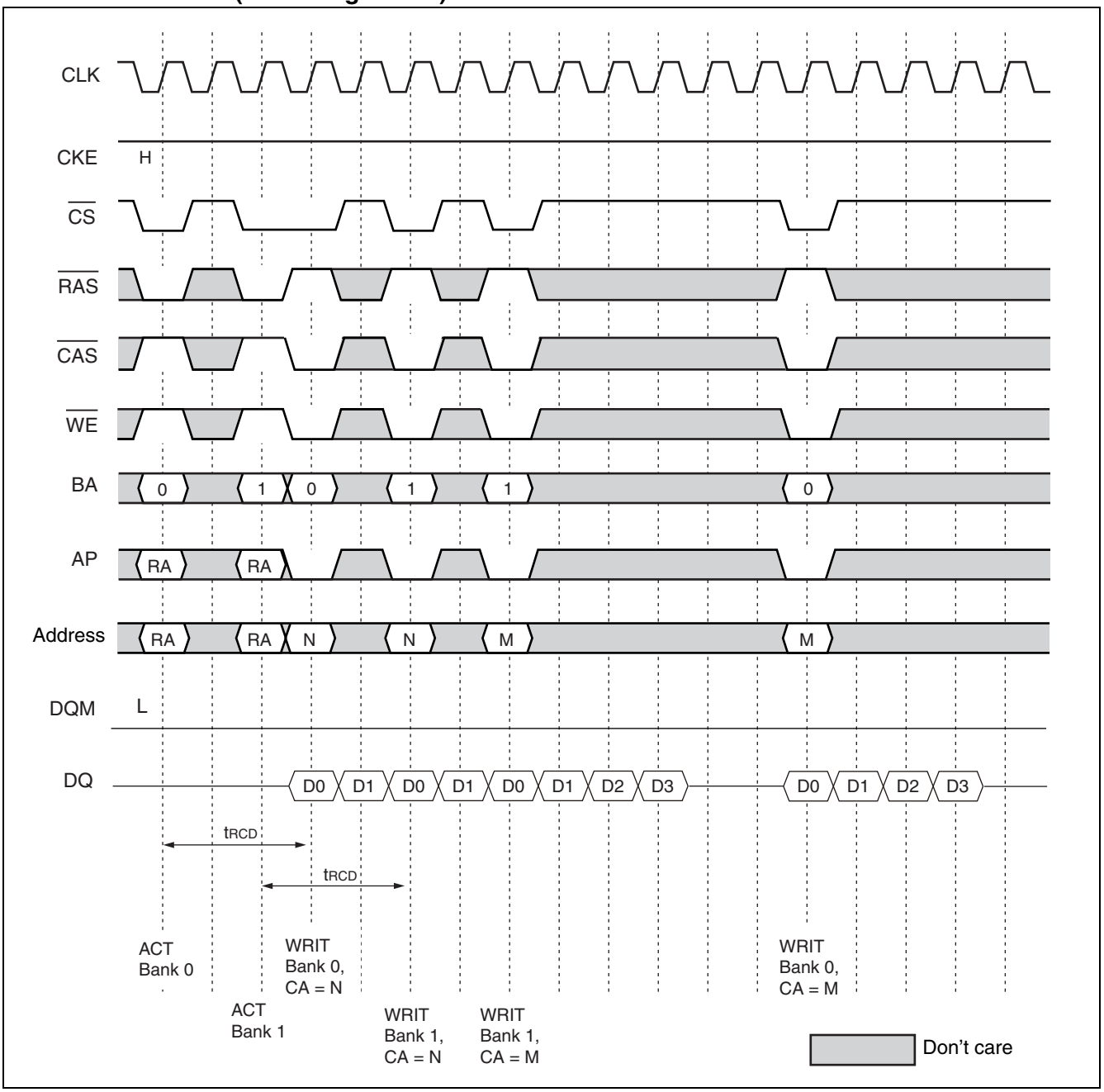
5. Write *1 (Assuming BL = 8)



*1: RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2: Burst write operation should not be terminated by PRE command. PRE can be issued after BL + t_{DPL} from WRIT command.

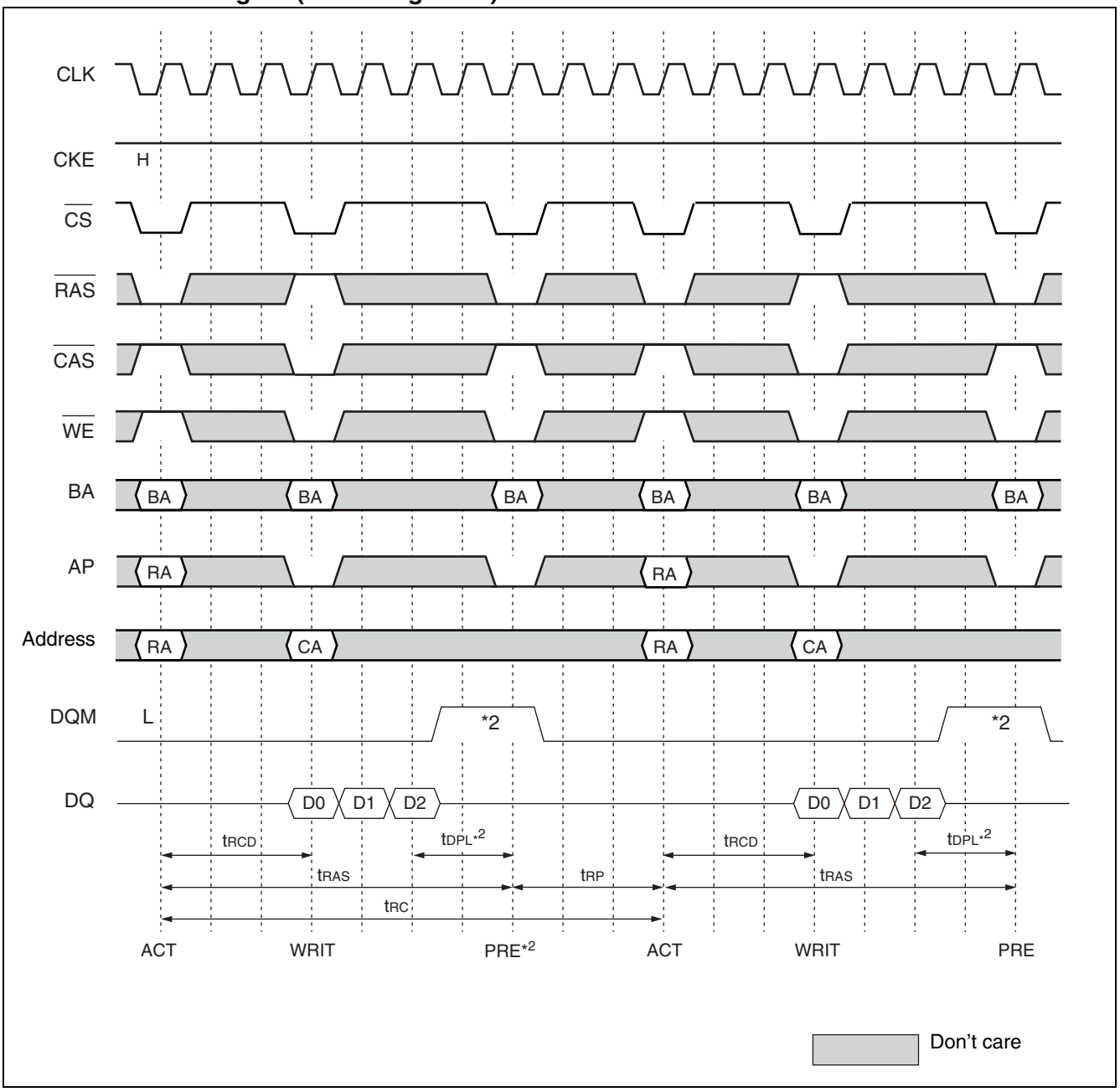
6. Write to Write *1 (Assuming BL = 4)



*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2 : Previous burst write can be interrupted by subsequent burst write.

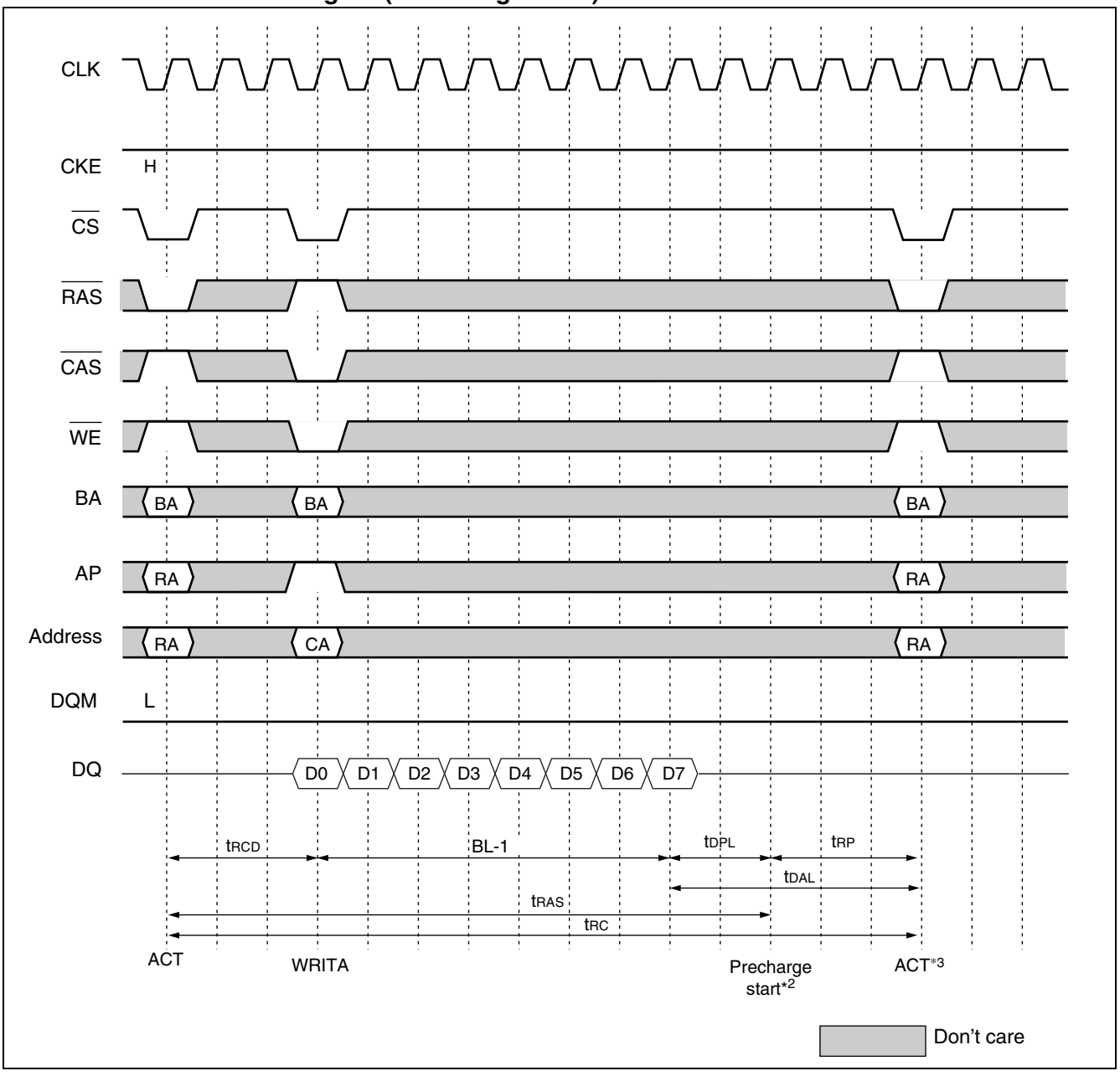
7. Write to Precharge *1 (Assuming BL=8)



* 1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

* 2 : Burst write operation can be terminated by PRE command. DQM must be High after last desired data input until PRE command is issued. PRE command must be issued after t_{DPL} from last desired data input.

8. Write with Auto Precharge *1 (Assuming BL = 8)

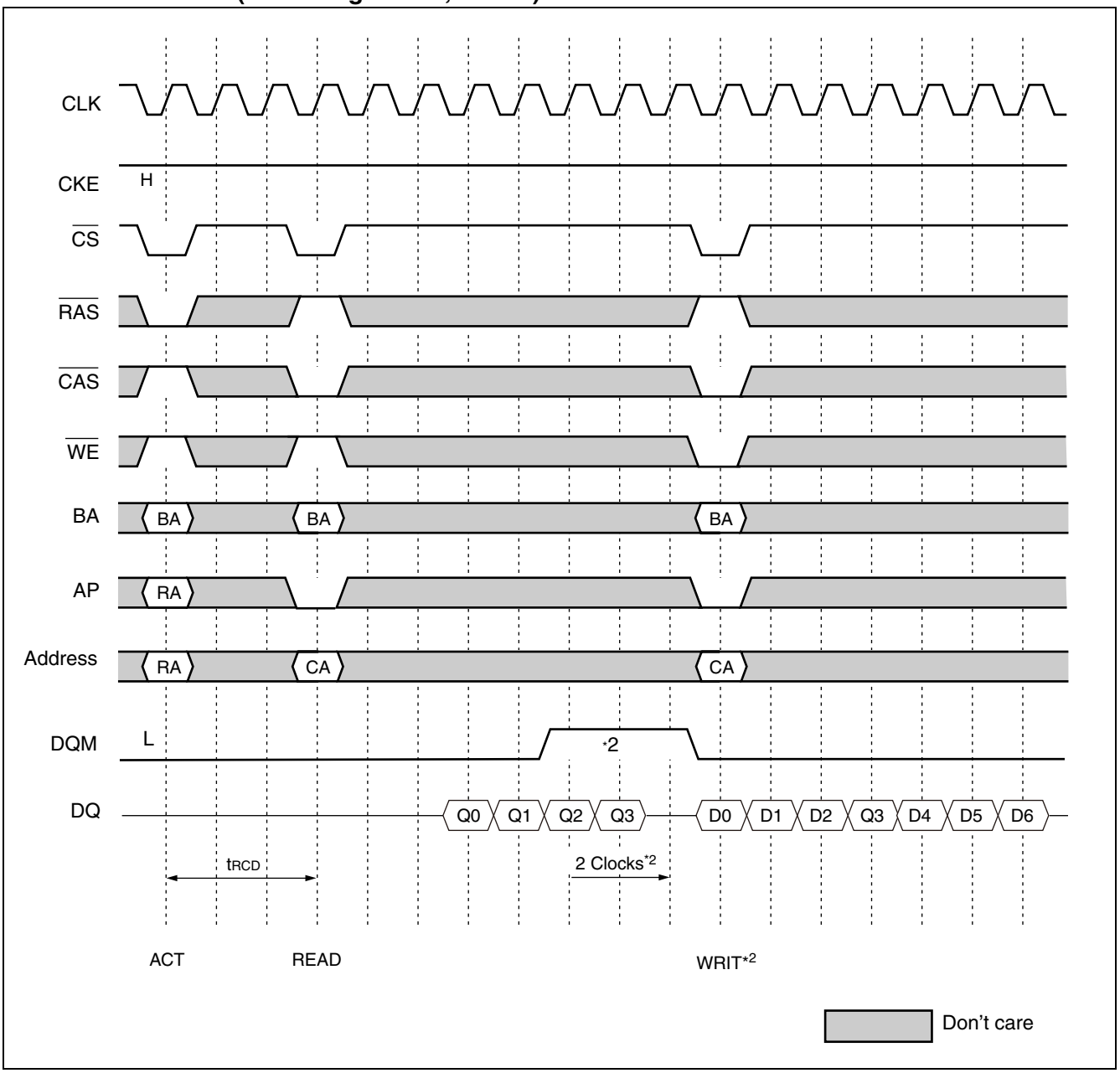


*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2 : Internal precharge operation starts after BL + t_{DPL} from WRITA command. t_{RAS} must be satisfied.

*3 : Next ACT command can be issued after t_{DAL} from last data input. t_{RC} must be satisfied.

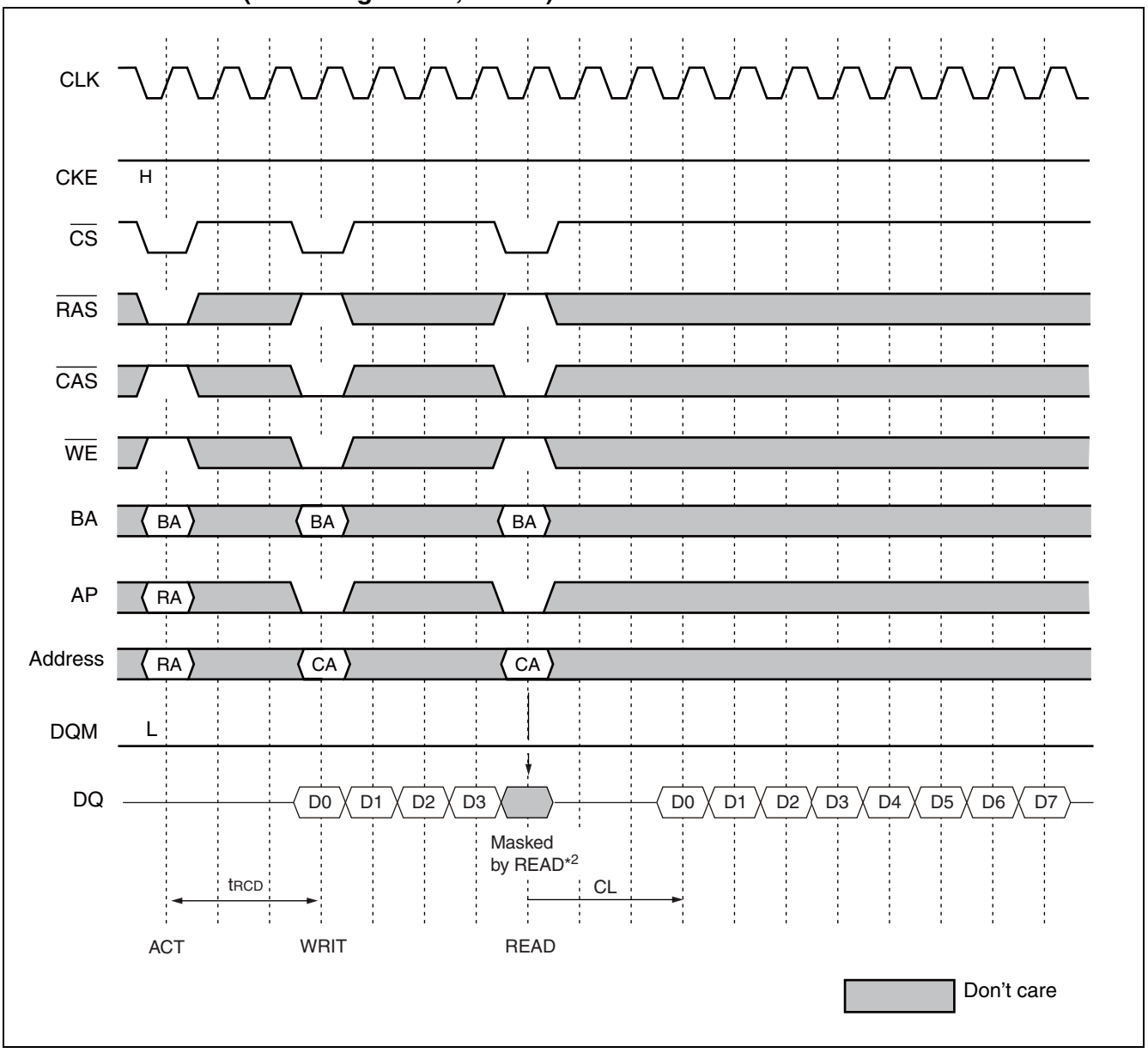
9. Read to Write *1 (Assuming CL = 3, BL = 8)



*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2 : READ command can be interrupted by WRIT command after all DQ pins become High-Z by DQM. DQ becomes High-Z after 2 clocks from DQM = H. DQM must be kept High until subsequent WRIT command is issued.

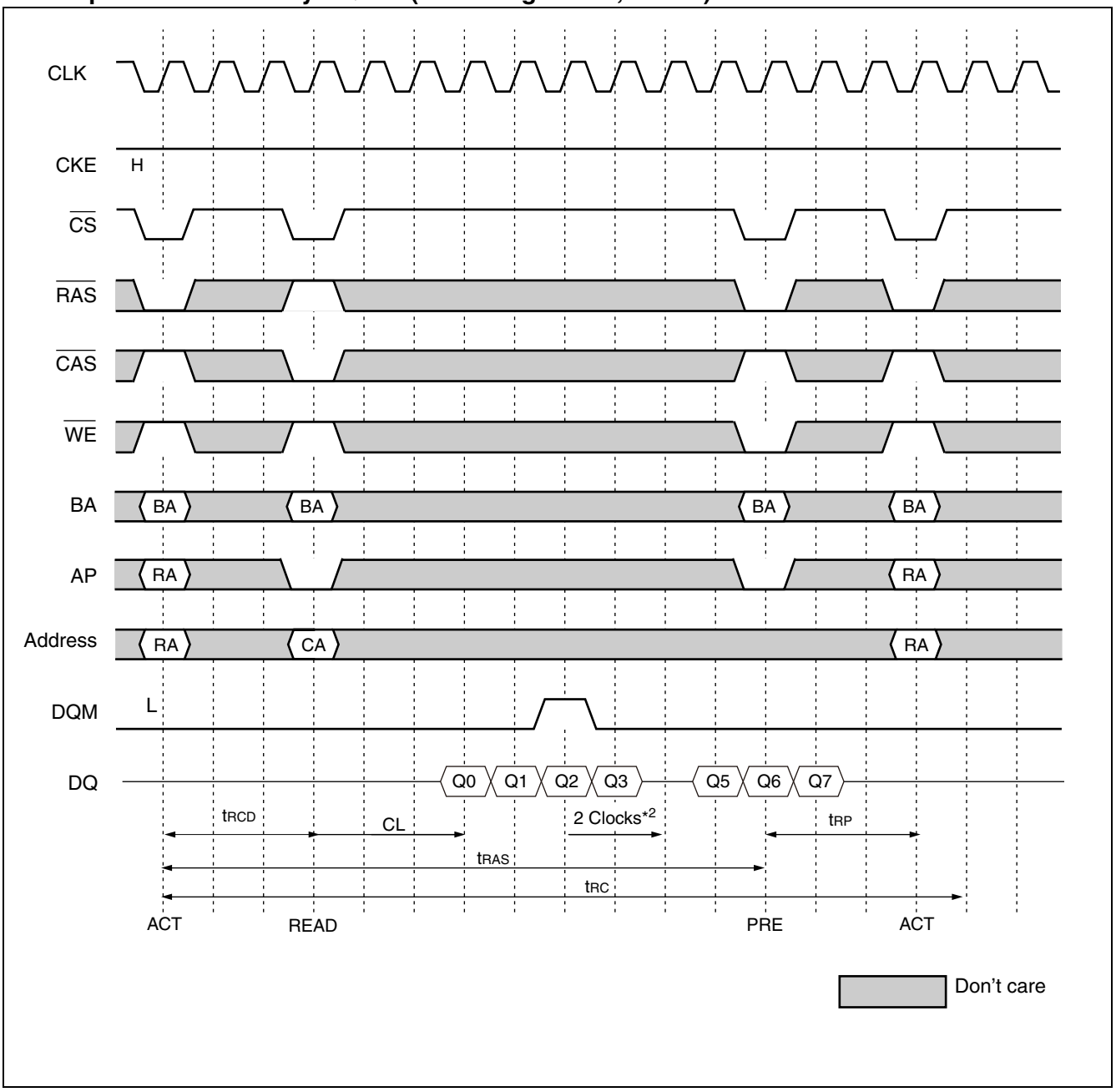
10. Write to Read *1 (Assuming CL = 3, BL = 8)



*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2 : WRIT command can be interrupted by READ. Input data is written until at 1 clock before READ command is issued. Input data coincident with READ command is masked.

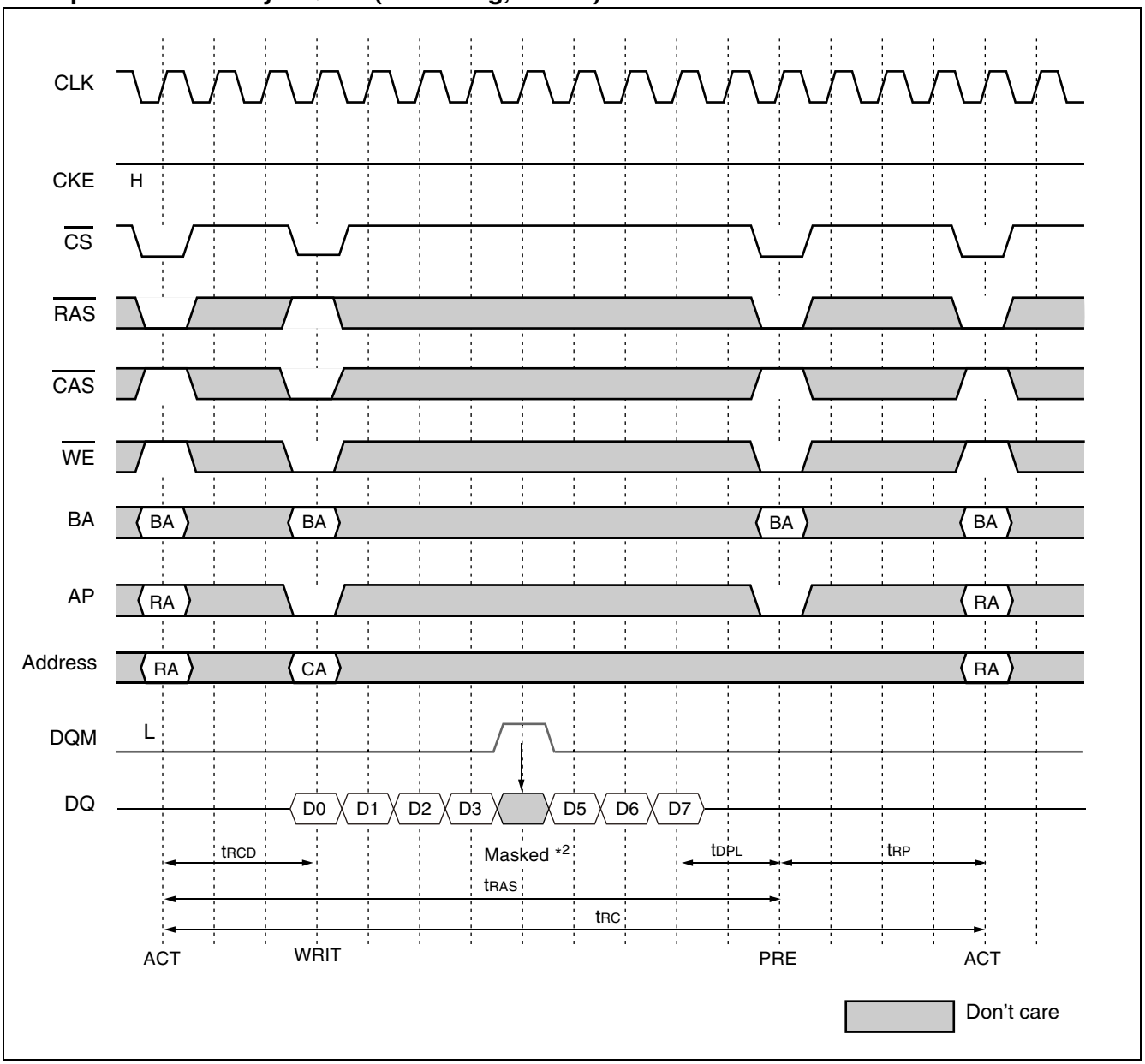
11. Output Data Disable by DQM *1 (Assuming CL = 3, BL = 8)



*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2 : When DQM is registered High during read operation, data output is disable after 2 clocks from DQM=H regardless CL.

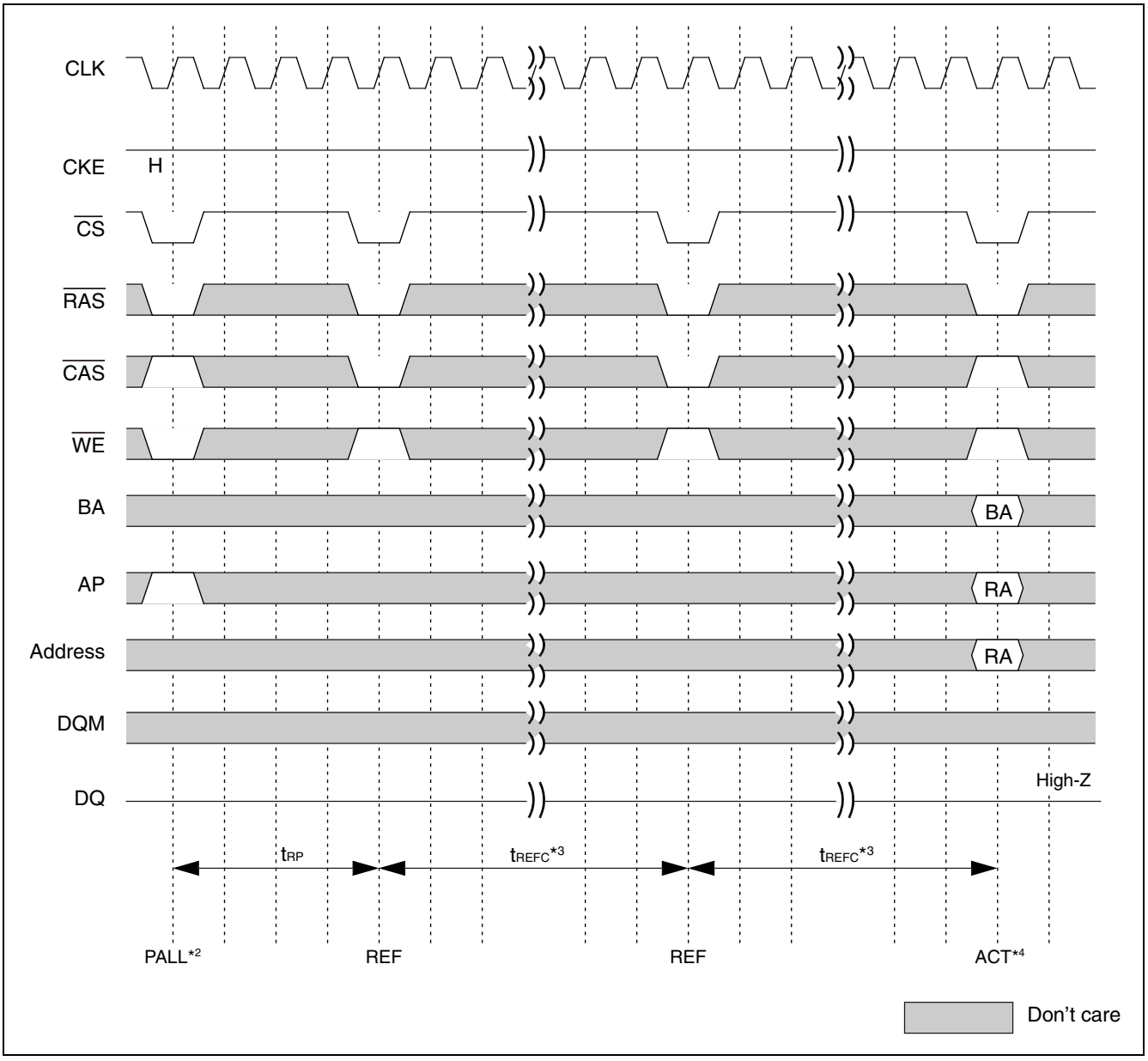
12. Input Data Mask by DQM *1 (Assuming, BL = 8)



*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2 : When DQM is registered High during write operation, input data coincident with DQM = H is masked.

13. Auto Refresh *1



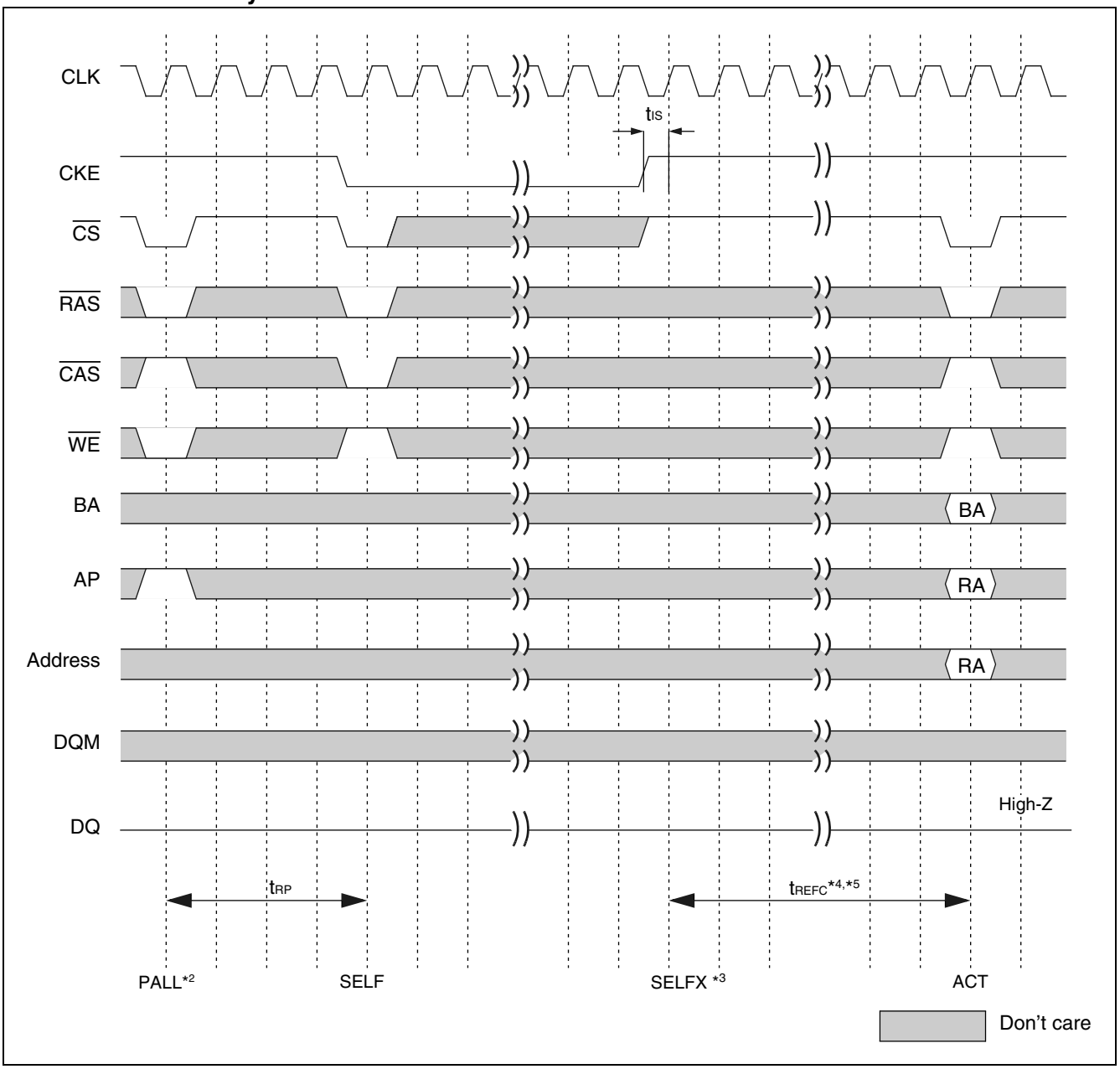
*1 : RA = Row Address, BA = Bank Address, AP = Auto Precharge

*2 : All banks must be precharged prior to the AUTO REFRESH command (REF).

*3 : Either NOP or DESL command should be asserted during t_{REFC} period.

*4 : ACT or MRS or REF command should be asserted after t_{REFC} from REF command.

14. Self Refresh Entry and Exit *1



*1 : RA = Row Address, BA = Bank Address, AP = Auto Precharge

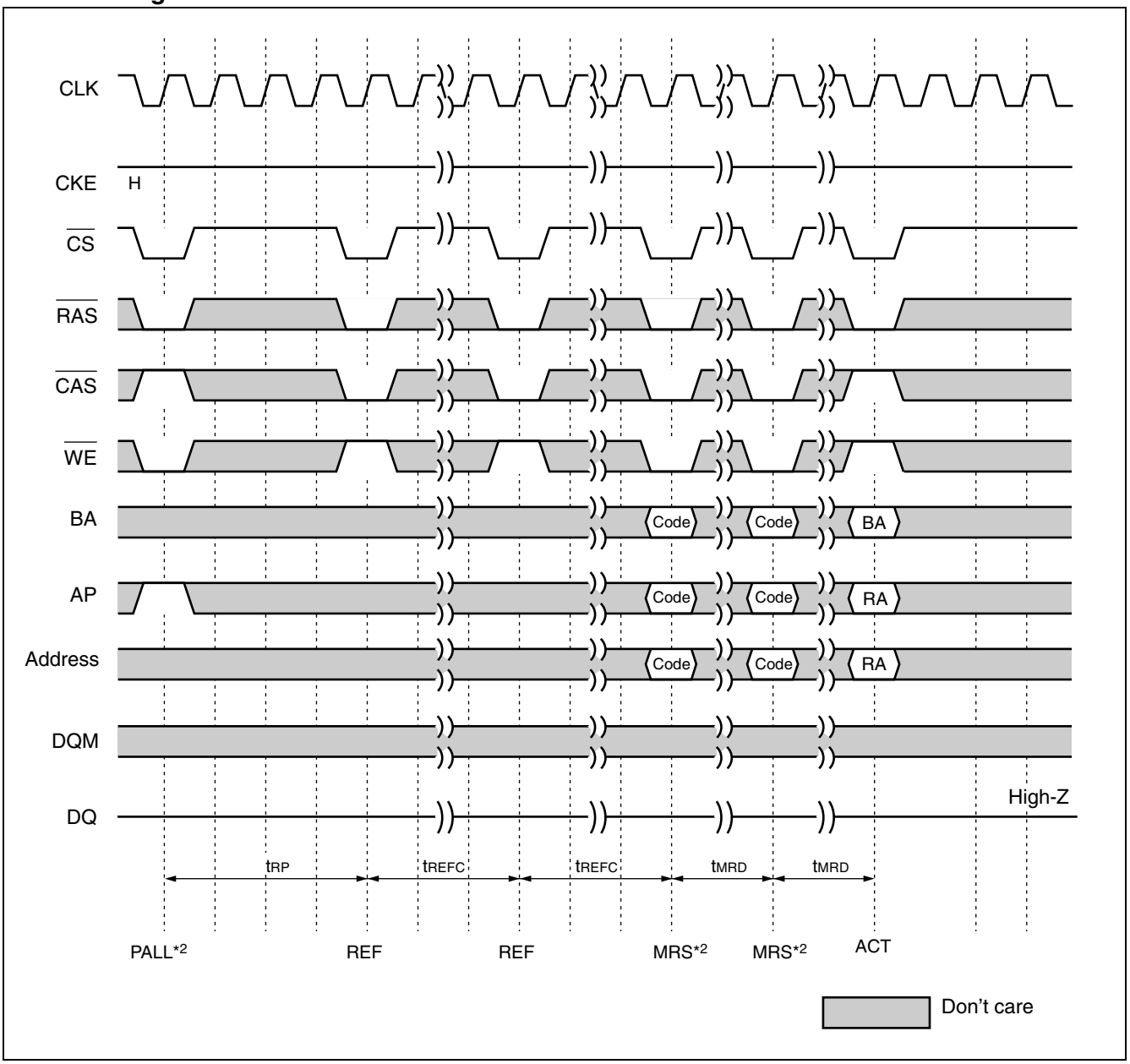
*2 : All banks must be precharged prior to SELF REFRESH ENTRY (SELF) command.

*3 : SELF REFRESH EXIT (SELFX) command can be latched at the CLK rising edge.

*4 : Either NOP or DESL command can be used during t_{REFC} period.

*5 : CKE should be held High during t_{REFC} period after SELFX command.

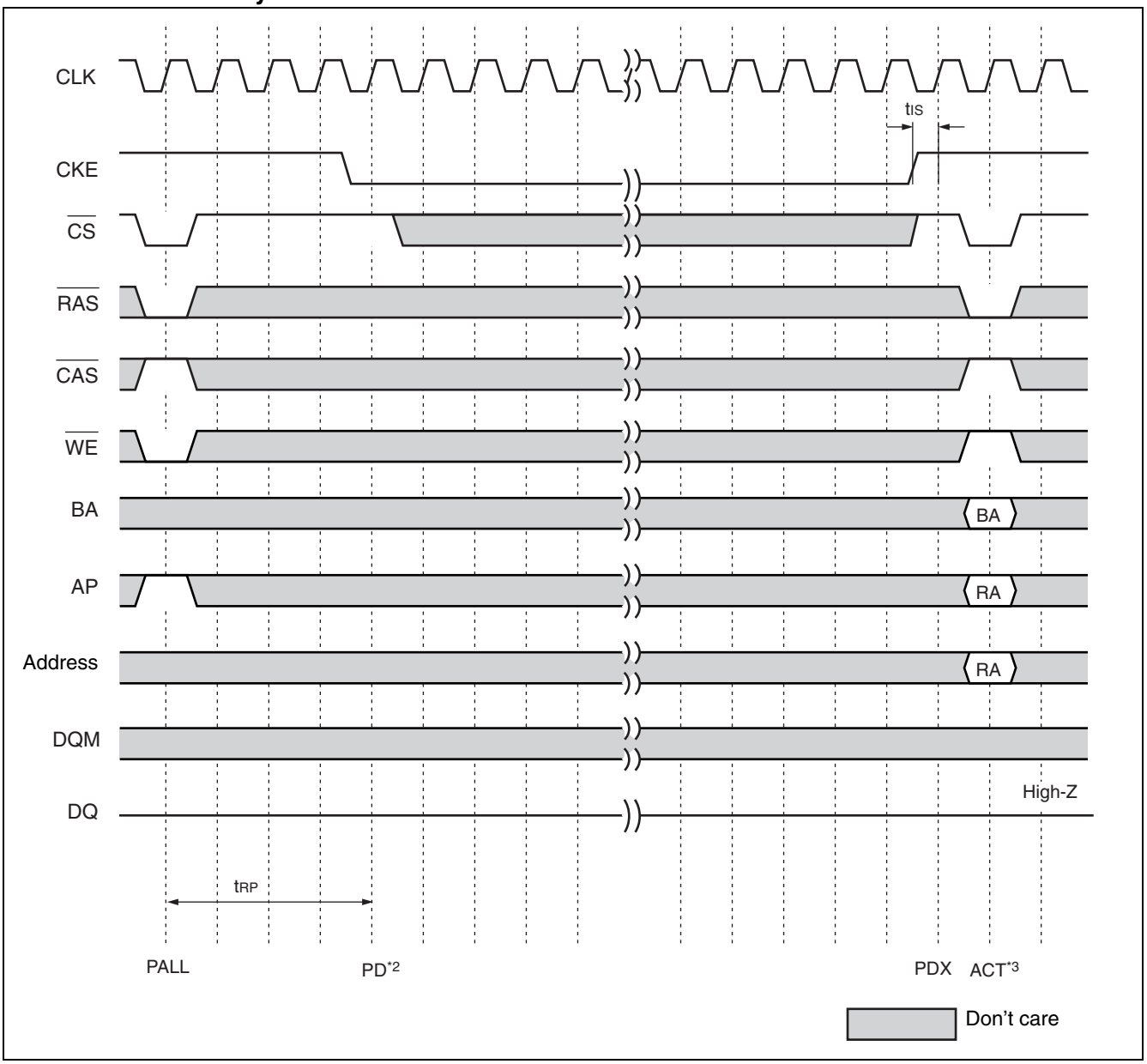
15. Mode Register Set*1



*1 : RA = Row Address, BA = Bank Address, AP = Auto Precharge

*2 : MODE REGISTER SET (MRS) command must be asserted after all banks have been precharged and all DQ are in High-Z.

16. Power Down Entry and Exit *1

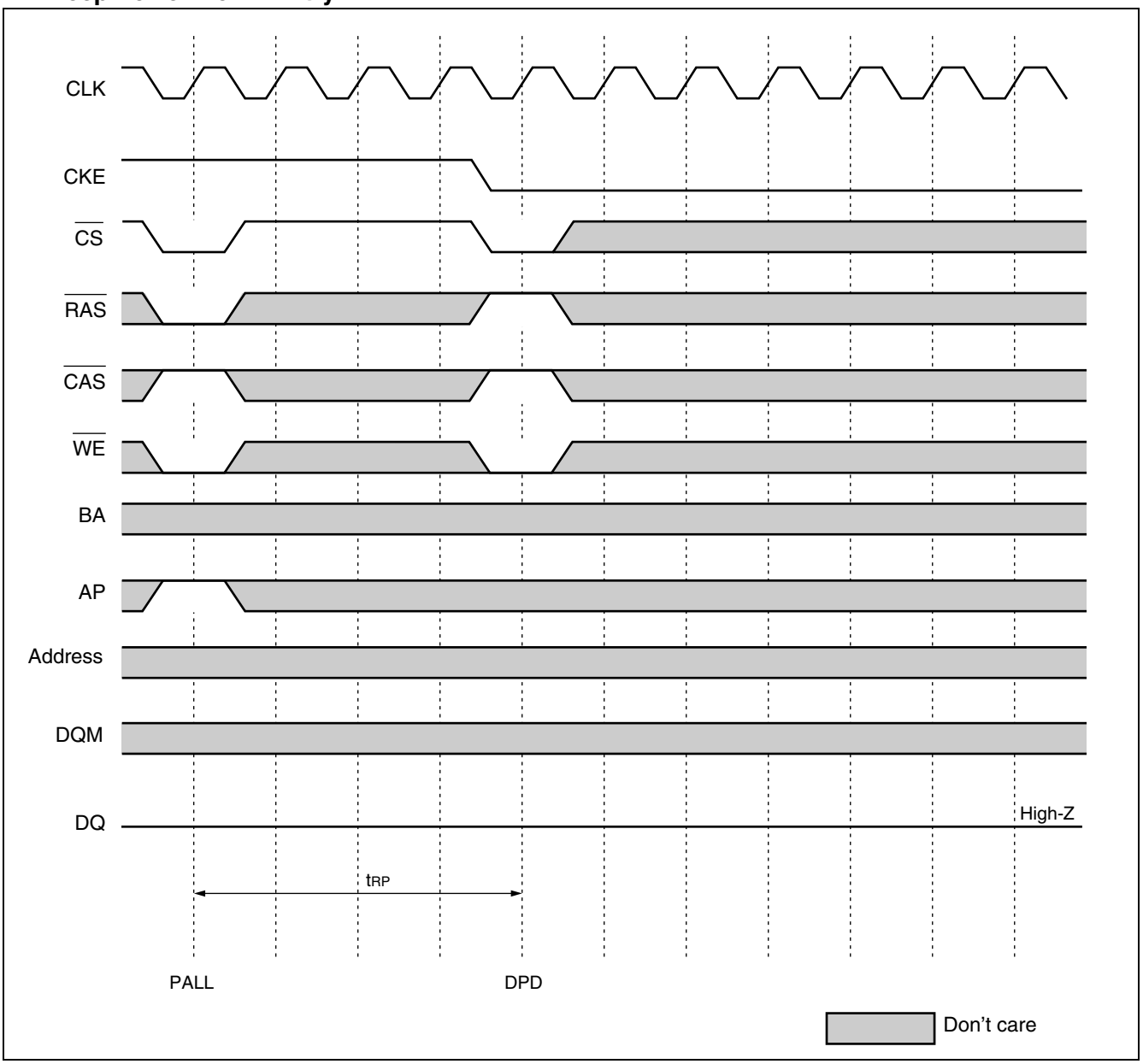


*1 : RA = Row Address, BA = Bank Address, AP = Auto Precharge

*2 : PD command can be issued after all banks have been precharged and all DQ are in High-Z.

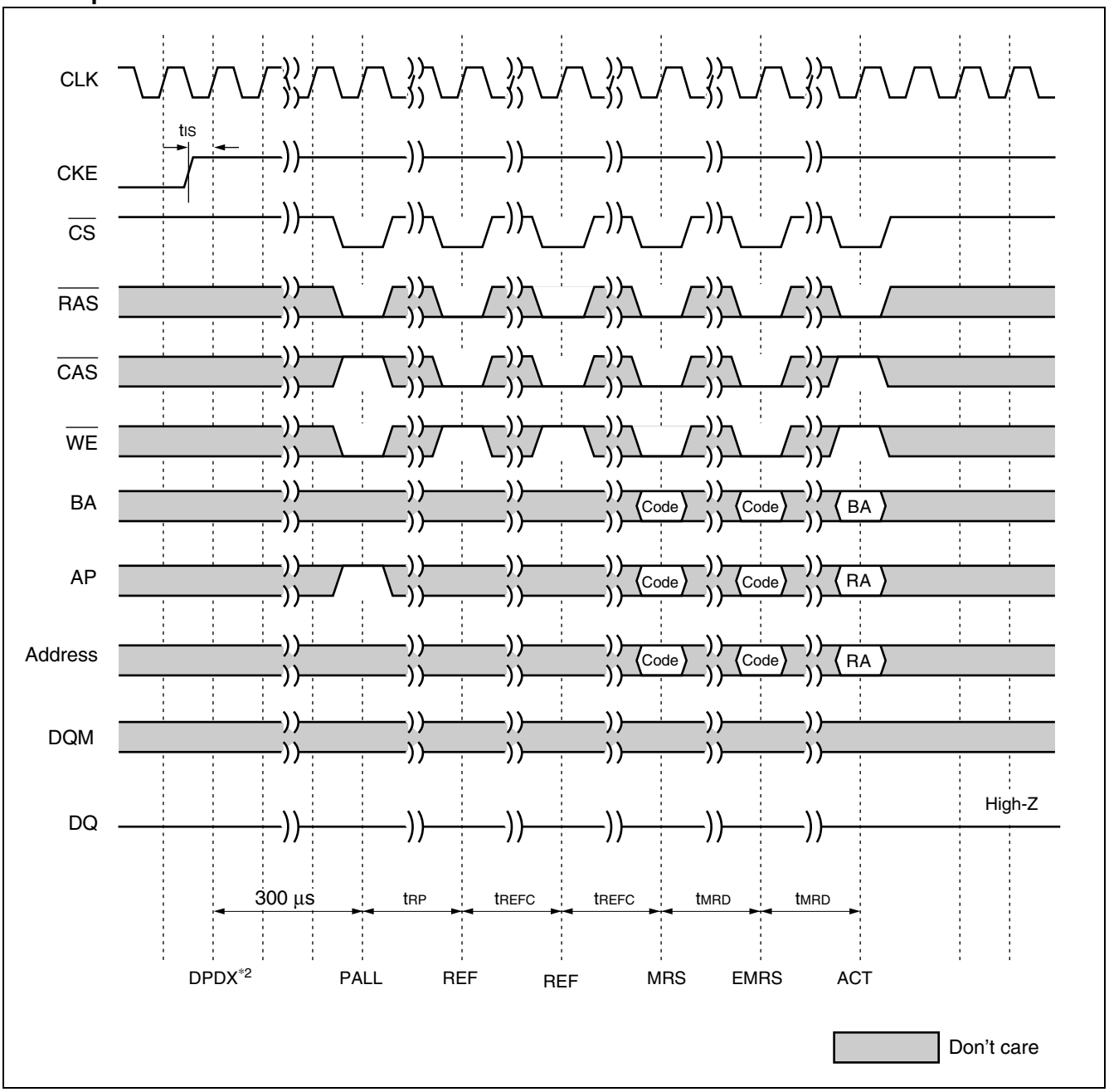
*3 : ACT command can be issued after 1 clock from POWER DOWN EXIT (PDX) command.

17. Deep Power Down Entry*



* : DEEP POWER DOWN ENTRY (DPD) Command can be issued after all banks have been precharged and all DQ are in High-Z.

18. Deep Power Down Exit *1



*1: RA = Row Address, BA = Bank Address, AP = Auto Precharge

*2: Power up initialization procedure must be performed after DPDX command.

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