

# PLL CLOCK MULTIPLIER WITH SS

**IDT5V80024**

## Description

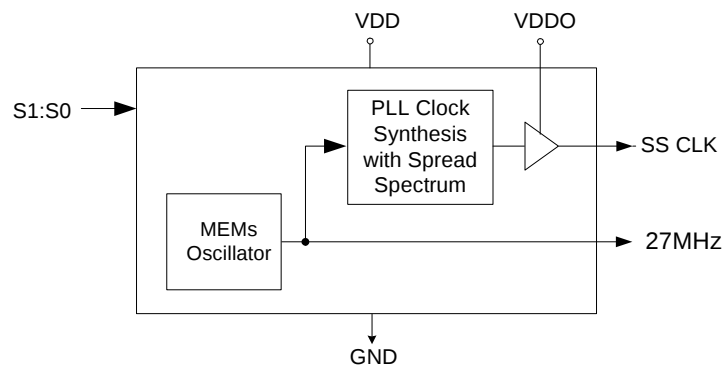
The IDT5V80024 is the most cost effective way to generate a high-quality, high-frequency clock output. The device also features a 27MHz output, making it ideal for systems to replace a high frequency oscillator along with a 1.8V 27MHz crystal.

Using Phase-Locked Loop (PLL) techniques, the device employs IDT's proprietary MEMs oscillator technology to produce common output frequencies for consumer, computing, and embedded applications that require spread spectrum to reduce system EMI.

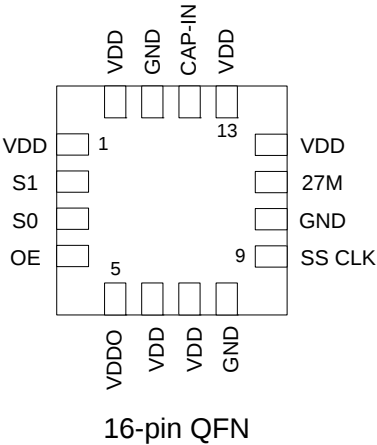
## Features

- Packaged in a small form factor 16-pin QFN
- Eliminates the need for an external crystal or input clock source
- Max.  $\pm 50$ ppm error on CLK and 27MHz output
- Typical  $\pm 75$  ps short term cycle-cycle jitter
- Down spread spectrum capability to reduce EMI
- Output voltage of 3.3 V
- Operating voltage of 1.8V
- Supports industrial temperature range
- Supports output frequency on CLK up to 130MHz
- Advanced, low-power CMOS process

## Block Diagram



Pin Assignment



SS CLK Output Frequency/Part Number Table

| Frequency   | Orderable Part Number |
|-------------|-----------------------|
| 27 MHz      | 5V80024-027NLGI       |
| 50 MHz      | 5V80024-050NLGI       |
| 66.6666 MHz | 5V80024-666NLGI       |
| 122.8 MHz   | 5V80024-122NLGI       |

Note: Contact IDT for any other frequencies.

Spread Spectrum Selection Table

| S1 | S0 | Spread Amount | Direction |
|----|----|---------------|-----------|
| 0  | 0  | No spread     | —         |
| 0  | 1  | -0.5%         | Down      |
| 1  | 0  | -1.0%         | Down      |
| 1  | 1  | -1.5%         | Down      |

\* Default setting is S1:S0 =00

## Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description                                                                               |
|------------|----------|----------|-----------------------------------------------------------------------------------------------|
| 1          | VDD      | Power    | Connect to +1.8V.                                                                             |
| 2          | S1       | Input    | Input select pin for spread spectrum selection. See table above. Internal pull-down resistor. |
| 3          | S0       | Input    | Input select pin for spread spectrum selection. See table above. Internal pull-down resistor. |
| 4          | OE       | Input    | Output enable for SS CLK and 27M outputs.                                                     |
| 5          | VDDO     | Power    | Connect to +3.3V.                                                                             |
| 6          | VDD      | Power    | Connect to +1.8V.                                                                             |
| 7          | VDD      | Power    | Connect to +1.8V.                                                                             |
| 8          | GND      | Ground   | Connect this pin to ground.                                                                   |
| 9          | SS CLK   | Output   | Single-ended clock output with spread spectrum.                                               |
| 10         | GND      | Ground   | Connect this pin to ground.                                                                   |
| 11         | 27M      | Output   | 27MHz reference output at 1.8V.                                                               |
| 12         | GND      | Ground   | Connect this pin to ground.                                                                   |
| 13         | VDD      | Power    | Connect to +1.8V.                                                                             |
| 14         | CAP-IN   | –        | This pin should be connected to GND (pin 15) through a 10µF capacitor                         |
| 15         | GND      | Ground   | Connect this pin to ground.                                                                   |
| 16         | VDD      | Power    | Connect to +1.8V.                                                                             |

## External Components

### Decoupling Capacitor

As with any high-performance mixed-signal IC, the IDT5V80024 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01  $\mu$ F must be connected between VDD and GND. It must be connected close to the IDT5V80024 to minimize lead inductance. No external power supply filtering is required for the IDT5V80024.

### Series Termination Resistor

A 33  $\Omega$  terminating resistor can be used next to the CLK pin and 27M pin. The total on-chip capacitance is approximately 12 pF.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5V80024. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item                                                   | Rating              |
|--------------------------------------------------------|---------------------|
| Supply Voltage, VDD                                    | 5 V                 |
| All Inputs and Outputs                                 | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature (industrial temperature) | -40 to +85° C       |
| Storage Temperature                                    | -65 to +150° C      |
| Soldering Temperature                                  | 260° C              |

## Recommended Operation Conditions

| Parameter                                         | Min.   | Typ. | Max.   | Units |
|---------------------------------------------------|--------|------|--------|-------|
| Ambient Operating Temperature (commercial)        | 0      | –    | +70    | ° C   |
| Ambient Operating Temperature (industrial)        | -40    | –    | +85    | ° C   |
| Power Supply Voltage (measured in respect to GND) | +1.71  | +1.8 | +1.89  | V     |
| Power Supply Voltage (VDDO)                       | +3.135 | +3.3 | +3.465 | V     |

## DC Electrical Characteristics

VDD=1.8 V  $\pm$ 5% , VDDO = 3.3 V, Ambient temperature -40 to +85° C, unless stated otherwise

| Parameter                    | Symbol          | Conditions                   | Min.     | Typ. | Max.    | Units |
|------------------------------|-----------------|------------------------------|----------|------|---------|-------|
| Operating Voltage            | VDD             |                              | 1.71     | 1.8  | 1.89    | V     |
| Output Voltage               | VDDO            | CLK                          | 3.135    | 3.3  | 3.465   | V     |
| Input High Voltage           | V <sub>IH</sub> |                              | 0.65     |      |         | V     |
| Input Low Voltage            | V <sub>IL</sub> |                              |          |      | 0.35VDD | V     |
| Output High Voltage*         | V <sub>OH</sub> | I <sub>OH</sub> = -2 mA, 27M | VDD-0.45 |      |         | V     |
| Output Low Voltage*          | V <sub>OL</sub> | I <sub>OL</sub> = 2 mA, 27M  |          |      | 0.45    | V     |
| Output High Voltage*         | V <sub>OH</sub> | I <sub>OH</sub> = -2 mA, CLK | VDD-0.45 |      |         | V     |
| Output Low Voltage*          | V <sub>OL</sub> | I <sub>OL</sub> = 2 mA, CLK  |          |      | 0.4     | V     |
| IDD Operating Supply Current |                 | No load                      |          | 15   | 22      | mA    |
| Input Capacitance            |                 |                              |          | 4    |         | pF    |

\*Note: Guaranteed by design.

## AC Electrical Characteristics–CLK

VDD=1.8 V  $\pm$ 5%, VDDO = 3.3 V, Ambient Temperature -40 to +85° C, unless stated otherwise

| Parameter                            | Symbol           | Conditions | Min.       | Typ. | Max. | Units |
|--------------------------------------|------------------|------------|------------|------|------|-------|
| Output Frequency                     | F <sub>OUT</sub> |            | See Page 2 |      |      | MHz   |
| Frequency Synthesis Error            |                  |            | -50        |      | 50   | ppm   |
| Output Clock Rise Time               | t <sub>OR</sub>  | 80% to 20% |            | 1    |      | ns    |
| Output Clock Fall Time               | t <sub>OF</sub>  | 20% to 80% |            | 1    |      | ns    |
| Output Clock Duty Cycle              | t <sub>OD</sub>  | VDD/2      | 45         | 50   | 55   | %     |
| Short Term Cycle-to-Cycle Jitter     | t <sub>ja</sub>  | CLK output |            | 75   | 100  | ps    |
| Long Term Jitter                     |                  | CLK output |            | TBD  | TBD  | ps    |
| Aging                                |                  | First year |            |      | 5    | ppm   |
| Power-up Time                        |                  |            |            | 10   | 45   | ms    |
| Spread Spectrum Modulation Frequency |                  |            |            | 32   |      | kHz   |

Note: Measured with a 7pF load.

## AC Electrical Characteristics–27M

VDD=1.8 V  $\pm$ 5%, Ambient Temperature -40 to +85° C, unless stated otherwise

| Parameter                        | Symbol           | Conditions | Min. | Typ. | Max. | Units |
|----------------------------------|------------------|------------|------|------|------|-------|
| Output Frequency                 | F <sub>OUT</sub> |            | 27   |      |      | MHz   |
| Frequency Synthesis Error        |                  |            | -50  |      | 50   | ppm   |
| Output Clock Rise Time           | t <sub>OR</sub>  | 80% to 20% |      | 1    |      | ns    |
| Output Clock Fall Time           | t <sub>OF</sub>  | 20% to 80% |      | 1    |      | ns    |
| Output Clock Duty Cycle          | t <sub>OD</sub>  | VDD/2      | 45   | 50   | 55   | %     |
| Short Term Cycle-to-Cycle Jitter | t <sub>ja</sub>  | 27M        |      | 50   | 75   | ps    |
| One Sigma Clock Period Jitter    | t <sub>js</sub>  | 27M        |      | 15   |      | ps    |
| Long Term Jitter                 |                  | 27M        |      | TBD  | TBD  | ps    |
| Aging                            |                  | First year |      |      | TBD  | ppm   |
| Power-up Time                    |                  |            |      | 10   | 45   | ms    |



## Revision History

| Rev. | Originator | Date     | Description of Change                                                                                                                                                                                                                |
|------|------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A    | K.B.       | 07/12/11 | Initial datasheet release                                                                                                                                                                                                            |
| B    | K.B.       | 10/21/11 | 1. Added 1.8V to 3.3 VDDO for CLK to Features<br>2. Added Power Supply Voltage (VDDO) spec to recommended Operating Conditions.<br>3. Updated DC char table.<br>4. Updated AC char table for CLK.<br>5. Added AC char table for 27M. |
| C    | J.C.       | 02/03/12 | 1. Updated Features bullets<br>2. Updated minimum output voltage spec from 1.71V to 3.135V<br>3. Updated IDD Operating Supply Current Typ. and Max. values<br>4. Updated Short Term C-C Jitter Typ. and Max. values                  |
| D    | J.C.       | 02/23/12 | Update "CLK Output Frequency/Part Number Tree" table by removing erroneous/invalid part numbers and updating frequencies                                                                                                             |
|      |            |          |                                                                                                                                                                                                                                      |

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