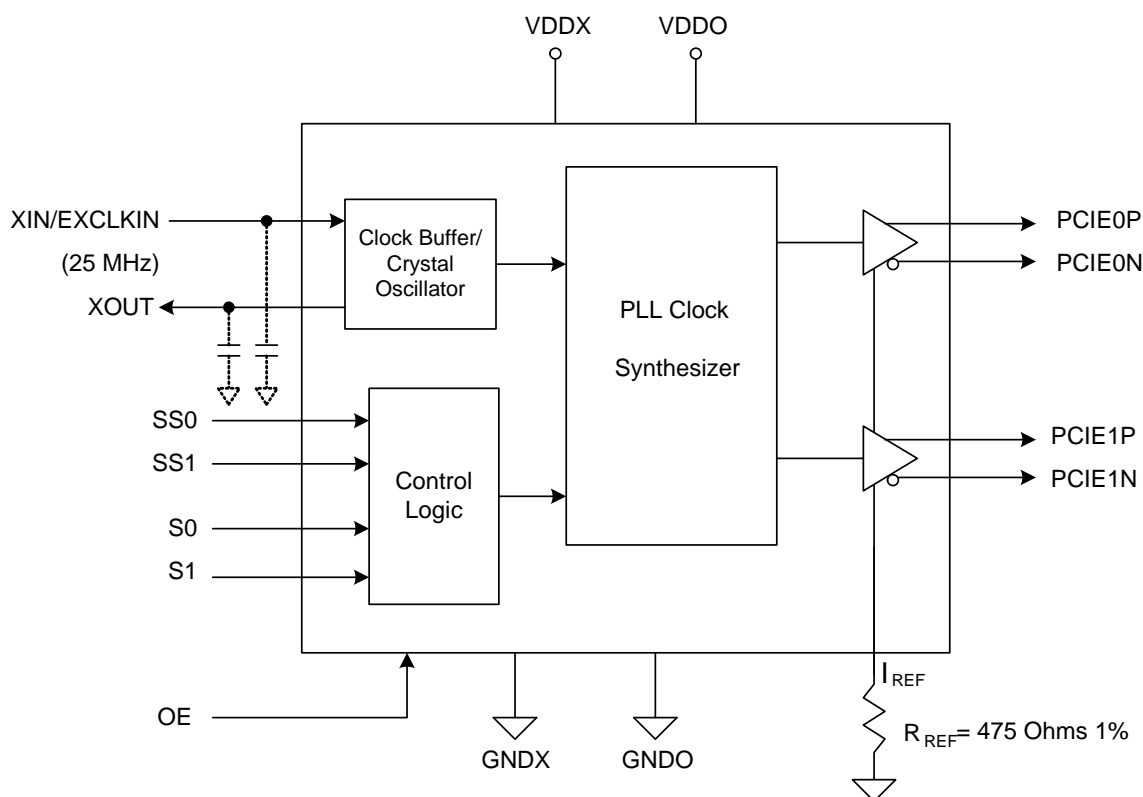# Two Outputs PCI-Express Clock Generator

## Features

- 25 MHz crystal or clock input

- Two sets of differential PCI-Express clocks

- Pin selectable output frequencies

- Supports HCSL compatible output levels

- Spread Spectrum capability on all output clocks with pin selectable spread range

- 16-pin TSSOP package

- Operating voltage 3.3 V

- Commercial and Industrial operating temperature range

## Functional Description

CY24293 is a two output PCI-Express clock generator device intended for networking applications. The device takes 25 MHz crystal or clock input and provides two pairs of differential outputs at 25 MHz, 100 MHz, 125 MHz, or 200 MHz for HCSL signaling standard.

The device incorporates Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction. The spread type and amount can be selected using select pins.
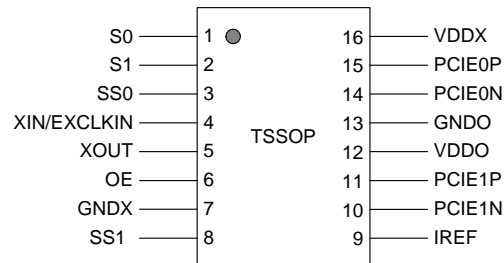
## Logic Block Diagram

**Cypress Semiconductor Corporation**   •   198 Champion Court   •   San Jose, CA  95134-1709   •   408-943-2600
Document Number: 001-46117  Rev. *E
Revised October 5, 2011

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## Contents

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## Pinouts

Figure 1. Pin Diagram - CY24293 16-pin TSSOP



## Pin Definitions - CY24293 16-pin TSSOP

| Pin Number | Pin Name | Pin Type | Description |
|---|---|---|---|
| 1 | S0 | Input | Frequency select pin. Has internal weak pull-up. Refer to Table 1. |
| 2 | S1 | Input | Frequency select pin. Has internal weak pull-up. Refer to Table 1. |
| 3 | SS0 | Input | Spread spectrum select pin 0. Has internal weak pull-up. Refer to Table 2. |
| 4 | XIN/EXCLKIN | Input | Crystal or clock input. 25 MHz fundamental mode crystal or clock input. |
| 5 | XOUT | Output | Crystal output. 25 MHz fundamental mode crystal input. Float for clock input. |
| 6 | OE | Input | High true output enable pin. When set low, PCI-E outputs are tri-stated. Has internal weak pull-up. |
| 7 | GNDX | Power | Ground |
| 8 | SS1 | Input | Spread spectrum select pin 1. has internal weak pull-up. Refer to Table 2. |
| 9 | IREF | Output | Current set for all differential clock drivers. Connect 475 Ω resistor to ground. |
| 10 | PCIE1N | Output | Differential PCI-Express complementary clock output. Tristated when disabled. |
| 11 | PCIE1P | Output | Differential PCI-Express true clock output. Tristated when disabled. |
| 12 | VDDO | Input | 3.3 V Power supply for output driver and analog circuits. |
| 13 | GNDO | Power | Ground |
| 14 | PCIE0N | Output | Differential PCI-Express complementary clock output. Tristated when disabled. |
| 15 | PCIE0P | Output | Differential PCI-Express true clock output. Tristated when disabled. |
| 16 | VDDX | Input | 3.3 V Power supply for oscillator and digital circuits. |

Table 1. Output Selection Table

| S1 | S0 | PCIE0[N,P], PCIE1[N,P] |
|---|---|---|
| 0 | 0 | 25 MHz |
| 0 | 1 | 100 MHz |
| 1 | 0 | 125 MHz |
| 1 | 1 | 200 MHz |

Table 2. Spread Selection Table

| SS1 | SS0 | Spread% |
|---|---|---|
| 0 | 0 | No Spread |
| 0 | 1 | −0.5% |
| 1 | 0 | −0.75% |
| 1 | 1 | No Spread |

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## Application Information

### Crystal Recommendations

CY24293 requires a parallel resonance crystal. Substituting a series resonance crystal causes the CY24293 to operate at the wrong frequency and violate the ppm specification. For most applications, there is a 300 ppm frequency shift between series and parallel crystals due to incorrect loading.

**Table 3.  Crystal Recommendations**

| Frequency | Cut | Load Cap | Eff Series Rest (max) | Drive (max) | Tolerance (max) | Stability (max) | Aging (max) |
|---|---|---|---|---|---|---|---|
| 25.00 MHz | Parallel | 16 pF | 30 Ω | 1.0 mW | 30 ppm | 10 ppm | 5 ppm/yr. |

### Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, consider the total capacitance the crystal sees to calculate the appropriate capacitive loading (CL).

Figure 2 shows a typical crystal configuration using two trim capacitors. It is important to note that the trim capacitors in series with the crystal are not parallel. It is a common misconception that load capacitors are in parallel with the crystal and must be approximately equal to the load capacitance of the crystal. This is not true.

### Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading.

As mentioned in the previous section, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1, Ce2) must be calculated to provide equal capacitive loading on both sides.

**Figure 2.  Crystal Loading Example**



Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2:

**Load capacitance (each side)**

$$Ce = 2 * CL - (Cs + Ci)$$

**Total capacitance (as seen by the crystal)**

$$CLe = \cfrac{1}{\left(\cfrac{1}{Ce1 + Cs1 + Ci1} + \cfrac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL .................................................. Crystal load capacitance

CLe ........................................ Actual loading seen by crystal using standard value trim capacitors

Ce .................................................... External trim capacitors

Cs ............................................. Stray capacitance (terraced)

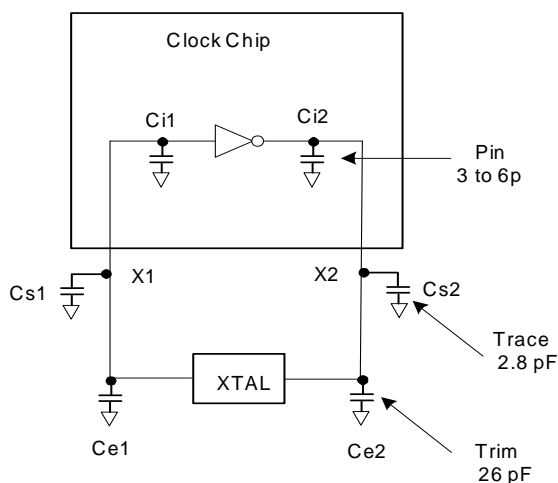Ci ........................................................ Internal capacitance

### Current Source ($I_{REF}$) Reference Resistor

If the board target trace impedance (Z) is 50 Ω, then for $R_{REF}$ = 475 Ω (1%), provides IREF of 2.32 mA. The output current ($I_{OH}$) is equal to $6*I_{REF}$.

### Output Termination

The PCI-Express differential clock outputs of the CY24293 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are explained in the section PCI-Express Layout Guidelines on page 5.

## PCB Layout Recommendations

For optimum device performance and the lowest phase noise, the following guidelines must be observed:

1. Each 0.01 µF decoupling capacitor must be mounted on the component side of the board as close to the $V_{DD}$ pin as possible.

2. No vias must be used between the decoupling capacitor and the $V_{DD}$ pin.

3. The PCB trace to the $V_{DD}$ pin and the ground via must be kept as short as possible. Distance of the ferrite bead and bulk decoupling from the device is less critical.

4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces must be routed away from the CY24293. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

## Decoupling Capacitors

The decoupling capacitors of 0.01 µF must be connected between $V_{DD}$ and GND as close to the device as possible. Do not share ground vias between components. Route power from the power source through the capacitor pad and then into the CY24293 pin.

## PCI-Express Layout Guidelines

### HCSL Compatible Layout Guidelines

**Table 4. Common Recommendations for Differential Routing**

| Differential Routing [1] | Dimension or Value | Unit |
|---|---|---|
| L1 length, route as non-coupled 50 $\Omega$ trace | 0.5 max | inch |
| L2 length, route as non-coupled 50 $\Omega$ trace | 0.2 max | inch |
| L3 length, route as non-coupled 50 $\Omega$ trace | 0.2 max | inch |
| $R_S$ | 33 | $\Omega$ |
| $R_T$ | 49.9 | $\Omega$ |

**Table 5. Differential Routing for PCI-Express Load or Connector**

| Differential Routing [1] | Dimension or Value | Unit |
|---|---|---|
| L4 length, route as coupled microstrip 100 $\Omega$ differential trace | 2 to 32 | inch |
| L4 length, route as coupled stripline 100 $\Omega$ differential trace | 1.8 to 30 | inch |

**Figure 3. PCI-Express Device Routing**
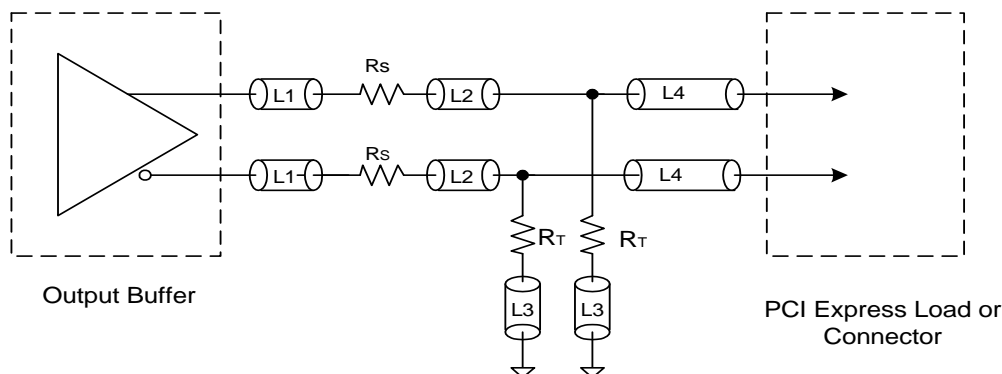


**Note**
1. Refer to Figure 3.

## Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

| Parameter | Description | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | –0.5 | 4.6 | V |
| $V_{IN}$ | Input voltage | Relative to $V_{SS}$ | –0.5 | $V_{DD}$ + 0.5 | V |
| $T_S$ | Temperature, Storage | Non Functional | –65 | +150 | °C |
| $T_J$ | Temperature, Junction | Non Functional | –65 | +150 | °C |
| $ESD_{HBM}$ | ESD Protection (Human Body Model) | JEDEC EIA/JESD22-A114-E | 2000 | – | V |
| UL-94 | Flammability rating | – | V-0 at 1/8 in. | | |
| MSL | Moisture sensitivity level | – | 3 | | |

## Recommended Operation Conditions

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 3.0 | – | 3.6 | V |
| $T_{AC}$ | Commercial ambient temperature | 0 | – | +70 | °C |
| $T_{AI}$ | Industrial ambient temperature | –40 | – | +85 | °C |
| $t_{PU}$ | Power up time for all $V_{DD}$ to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | – | 500 | ms |

## DC Electrical Characteristics

Unless otherwise stated, $V_{DD}$ = 3.3 V ± 0.3 V, ambient temperature = –40 °C to +85 °C Industrial, 0 °C to +70 °C Commercial

| Parameter [2] | Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low voltage | – | –0.3 | – | 0.8 | V |
| $V_{IH}$ | Input high voltage | – | 2.0 | – | $V_{DD}$ + 0.3 | V |
| $V_{OL}$ | Output low voltage of PCIE0[P/N], PCIE1[P/N] | HCSL termination ($R_S$ = 33 Ω, $R_T$ = 49.9 Ω) | –0.2 | 0 | 0.05 | V |
| $V_{OH}$ | Output high voltage of PCIE0[P/N], PCIE1[P/N] | HCSL termination ($R_S$ = 33 Ω, $R_T$ = 49.9 Ω) | 0.65 | 0.71 | 0.85 | V |
| $I_{DD}$ | Operating supply current | No load, OE = 1 | – | 45 | 60 | mA |
| $I_{DDOD}$ | Output disabled current | OE = 0 | – | – | 50 | mA |
| $C_{IN}$ | Input capacitance | All input pins | – | 5 | – | pF |
| $R_{PU}$ | Pull-up resistance | S0, S1, SS0, SS1, OE | – | 70k | – | Ω |

**Note**
2. Parameters are guaranteed by design and characterization. Not 100% tested in production

## AC Electrical Characteristics

Unless otherwise stated: $V_{DD}$ = 3.3 V ± 0.3 V, ambient temperature = –40 °C to +85 °C Industrial, 0 °C to +70 °C Commercial, Outputs HCSL terminated.

| Parameter [2] | Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{IN}$ | Input clock frequency (crystal or external clock) | – | – | 25 | – | MHz |
| $F_{OUT}$ | Output frequency | HCSL termination | – | – | 200 | MHz |
| $F_{ERR}$ | Frequency synthesis error | – | – | 0 | – | ppm |
| $T_{CCJ}$ | Cycle-to-cycle jitter [3] | – | – | – | 75 | ps |
| $SP_{MOD}$ | Spread modulation frequency | – | – | 32 | – | kHz |
| $T_{DC}$ | Output clock duty cycle [3, 4] | – | 45 | 50 | 55 | % |
| $T_{OEH}$ | Output enable time | OE going high to differential outputs becoming valid | – | – | 200 | ns |
| $T_{OEL}$ | Output disable time | OE going low to differential outputs becoming invalid | – | – | 200 | ns |
| $T_{LOCK}$ | Clock stabilization from power up | Measured from 90% of the applied power supply level | – | 1 | 2 | ms |
| $T_R$ | Output rise time [3, 5] | Measured from 0.175 V to 0.525 V | 130 | – | 700 | ps |
| $T_F$ | Output fall time [3, 5] | Measured from 0.525 V to 0.175 V | 130 | – | 700 | ps |
| $DT_R$ | Rise time variation [3, 5] | For a given frequency, Max ($T_R$) – Min ($T_R$) | – | – | 125 | ps |
| $DT_F$ | Fall time variation [3, 5] | For a given frequency, Max ($T_F$) – Min ($T_F$) | – | – | 125 | ps |
| $T_{OSKEW}$ | Output skew [4] | Measured at $V_{CROSS}$ point | – | – | 50 | ps |
| $V_{CROSS}$ | Absolute crossing point voltage [4, 6] | – | 0.25 | 0.35 | 0.55 | V |
| $V_{Xdelta}$ | Variation of $V_{CROSS}$ over all clock edges [4, 7] | – | – | – | 140 | mV |

## Test and Measurement Setup

**Figure 4.  Test Load Configuration for Differential Output Signals**
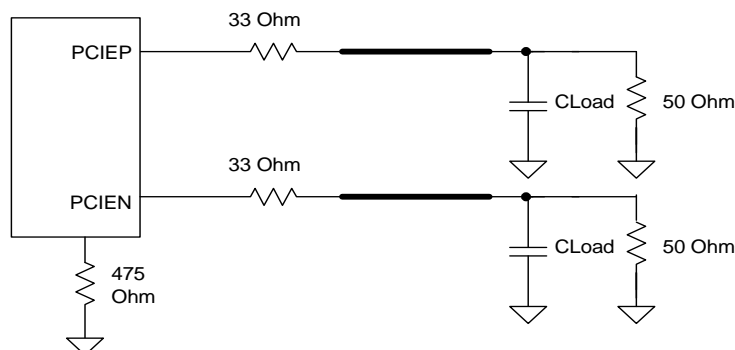


**Notes**
3. Measured with Cload = 4 pF max. (scope probe + trace load).
4. Measured at crossing point where the instantaneous voltage value of the rising edge of PCIEP equals the falling edge of PCIEN.
5. Measurement taken from a differential waveform.
6. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
7. Refers to the difference between the PCIEP rising edge $V_{CROSS}$ average value and the PCIEN rising edge $V_{CROSS}$ average value.

## Ordering Information

| Part Number | Type | Production Flow |
|---|---|---|
| **Pb-free** | | |
| CY24293ZXC | 16-pin TSSOP | Commercial, 0 °C to 70 °C |
| CY24293ZXCT | 16-pin TSSOP Tape and Reel | Commercial, 0 °C to 70 °C |
| CY24293ZXI | 16-pin TSSOP | Industrial, –40 °C to 85 °C |
| CY24293ZXIT | 16-pin TSSOP Tape and Reel | Industrial, –40 °C to 85 °C |

### Ordering Code Definitions

CY   24293   Z   X   X   X

X = T or blank
T = Tape and Reel; blank = Tube

Temperature Range: X = C or I
C = Commercial; I = Industrial

Pb-free

Package Type:
Z = 16-pin TSSOP

Base Device Part Number

Company ID: CY = Cypress

## Package Diagram

**Figure 5.  16-pin TSSOP 4.40 mm Body Z16.173/ZZ16.173 Package Outline, 51-85091**
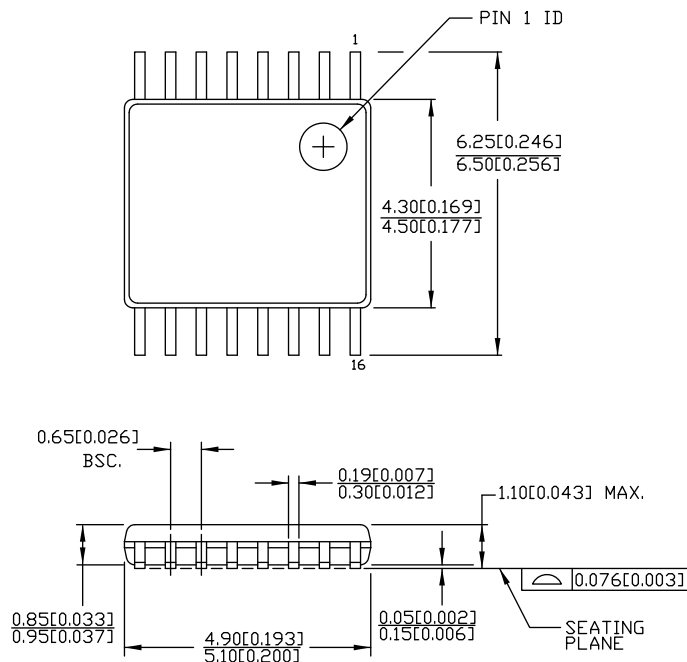


DIMENSIONS IN MM[INCHES] <u>MIN.</u>
MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05gms

| PART # | |
|---|---|
| Z16.173 | STANDARD PKG. |
| ZZ16.173 | LEAD FREE PKG. |

51-85091 *D

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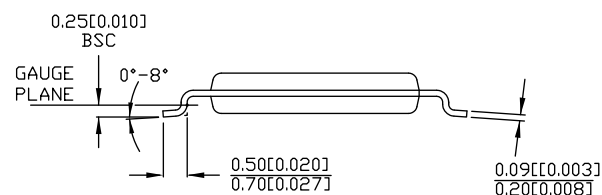
## Acronyms

| Acronym | Description |
|---------|-------------|
| EIA | electronic industries alliance |
| EMI | electromagnetic interference |
| ESD | electrostatic discharge |
| HCSL | high speed current steering logic |
| JEDEC | joint electron devices engineering council |
| PCB | printed circuit board |
| PCI | peripheral component interconnect |
| PLL | phase-locked loop |
| TSSOP | thin shrunk small outline package |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| kHz | kilohertz |
| MHz | megahertz |
| µF | microfarad |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| mW | milliwatt |
| ns | nanosecond |
| Ω | ohm |
| ppm | parts per million |
| % | percent |
| pF | picofarad |
| ps | picosecond |
| V | volt |

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## Document History Page

| Document Title: CY24293, Two Outputs PCI-Express Clock Generator | | | | |
|---|---|---|---|---|
| Document Number: 001-46117 | | | | |
| **REV.** | **ECN NO.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 2490167 | PYG / DPF / AESA | See ECN | New Data Sheet |
| *A | 2507681 | DPF / AESA | 05/23/2008 | Added Note 1: Parameters are guaranteed by design and characterization. Not 100% tested in production.<br>Added Note 2 for Duty cycle spec in the AC Elect. Characteristics.<br>Added HCSL termination in Condition for $V_{OL}$, $V_{OH}$ DC Elect. Char.<br>Added $V_{Xdelta}$ value of 140 mV in the Differential 100 MHz HCSL output.<br>Changed Cload from 2 pF to 4 pF in Note 2.<br>Added internal weak Pull-ups for S0, S1, SS0, SS1 and OE pins.<br>Updated $T_{OEH}$ and $T_{OEL}$ to 200 ns (max.).<br>Updated data sheet template |
| *B | 2621901 | CXQ / AESA | 12/19/2008 | Updated $I_{DD}$ spec in DC Electrical Characteristics.<br>Added max spec for $I_{DDOD}$ DC Electrical Characteristics.<br>Added $R_{PU}$ in DC Electrical Characteristics.<br>Replaced $T_{RFVAR}$ with $DT_R$ and $DT_F$ in AC Electrical Characteristics.<br>Added definitions for rise and fall time variation, crossing point variation in AC Electrical Characteristics.<br>Reduced cycle-to-cycle jitter spec to 75ps in AC Electrical Characteristics. |
| *C | 2683343 | CXQ / PYRS | 04/03/2009 | Removed "Preliminary" from data sheet title and headings<br>Added "max" to crystal ESR spec.<br>Changed "LVDS Down Device" to "LVDS Device" in Table 8 and Figure 4. |
| *D | 3289802 | BASH | 06/27/2011 | Updated to latest template.<br>Added Table of Contents.<br>Updated package Diagram.<br>Added Ordering Code Definitions.<br>Added Acronyms and Units of Measure. |
| *E | 3395894 | PURU | 10/05/2011 | Updated Features (Removed LVDS related information).<br>Updated Functional Description (Removed LVDS related information).<br>Updated Output Termination under Application Information (Removed LVDS related information).<br>Removed the section LVDS Compatible Layout Guidelines under the main section PCI-Express Layout Guidelines.<br>Updated AC Electrical Characteristics (Removed LVDS related information).<br>Updated Package Diagram.<br>Updated in new template. |

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