ADC1005 10-Bit µP Compatible A/D Converter

Check for Samples: ADC1005

FEATURES

- **Easy interface to all microprocessors**
- **Differential analog voltage inputs**
- **Operates ratiometrically or with 5 V_{DC} voltage reference or analog span adjusted voltage reference**
- **0V to 5V analog input voltage range with single 5V supply**
- **On-chip clock generator**
- **TLL/MOS input/output compatible**
- **0.3″ standard width 20-pin DIP**

KEY SPECIFICATIONS

- **Resolution 10 bits**
- **Linearity Error ±½ LSB and ±1 LSB**
- **Conversion Time 50 µs**

DESCRIPTION

NOTE: This device is obsolete. This data sheet is provided for information only.

The ADC1005 is a CMOS 10-bit successive approximation A/D converter. The 20-pin ADC1005 outputs 10-bit data in a two-byte format for interface with 8-bit microprocessors.

The ADC1005 has differential inputs to permit rejection of common-mode signals, allow the analog input range to be offset, and also to permit the conversion of signals not referred to ground. In addition, the reference voltage can be adjusted, allowing smaller voltage spans to be measured with 10-bit resolution.

Connection Diagram

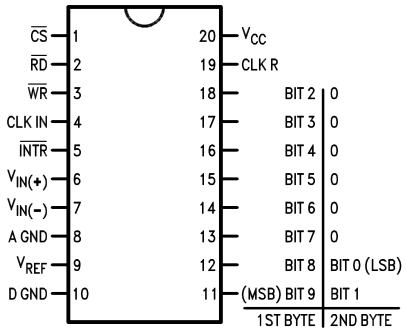


Figure 1. ADC 1005 (for an 8–bit data bus)
Dual-In-Line Package - Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

Supply Voltage (V_{CC})			6.5V
Logic Control Inputs			−0.3V to +15V
Voltage at Other Inputs and Outputs			−0.3V to V_{CC} +0.3V
Input Current Per Pin			±5 mA
Input Current Per Package			±20 mA
Storage Temperature Range			−65°C to +150°C
Package Dissipation at T_A=25°C			875 mW
Lead Temperature	Soldering, 10 seconds	Dual-In-Line Package (Ceramic)	300°C
ESD Susceptibility[4]			800V

(1) All voltages are measured with respect to ground.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Operating Ratings[1][2]

Supply Voltage (V_{CC})		4.5V to 6.0V
Temperature Range		$T_{MN} \le T_A \le T_{MAX}$
ADC1005BCJ	ADC1005BCJ-1, ADC1005CCJ-1	−40°C≤T_A≤+85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
(2) All voltages are measured with respect to ground.

Electrical Characteristics

The following specifications apply for V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = 1.8 MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** All other limits $T_A = T_j$ = 25°C.

Parameter	Conditions	ADC1005BCJ			ADC1005BCJ-1, ADC1005CCJ-1			Limit Units
		Typ[1]	Tested Limit[2]	Design Limit[3]	Typ[1]	Tested Limit[2]	Design Limit[3]	
Converter Characteristics								
Linearity Error[4]								
ADC1005BCJ			**±0.5**					LSB
ADC1005BCJ-1						±0.5	**±0.5**	LSB
ADC1005CCJ-1						±1	**±1**	LSB
Zero Error								
ADC1005BCJ			**±0.5**					LSB
ADC1005BCJ-1						±0.5	**±0.5**	LSB
ADC1005CCJ-1						±1	**±1**	LSB
Fullscale Error								
ADC1005BCJ			**±0.5**					LSB
ADC1005BCJ-1						±0.5	**±0.5**	LSB
ADC1005CCJ-1						±1	**±1**	LSB
Reference MIN		4.8	**2.2**		4.8	2.4	**2.2**	kΩ
Input MAX		4.8	**8.3**		4.8	7.6	**8.3**	kΩ
Resistance								

(1) Typicals are at 25°C and represent most likely parametric norm.
(2) Tested and guaranteed to TI's AOQL (Average Outgoing Quality Level).
(3) Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.
(4) Linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line which passes through the end points of the transfer characteristic.

Electrical Characteristics (continued)

The following specifications apply for V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = 1.8 MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** All other limits $T_A = T_j$ = 25°C.

Parameter	Conditions	ADC1005BCJ			ADC1005BCJ-1, ADC1005CCJ-1			Limit Units
		Typ(1)	Tested Limit(2)	Design Limit(3)	Typ(1)	Tested Limit(2)	Design Limit(3)	
Common-Mode Input(5) MIN	$V_{IN}(+)$ or $V_{IN}(-)$		**V_{CC}+0.05**			V_{CC}+0.05	**V_{CC}+0.05**	V
Common-Mode Input(5) MAX	$V_{IN}(+)$ or $V_{IN}(-)$		**GND−0.05**			GND−0.05	**GND−0.05**	V
DC Common-Mode Error	Over Common-Mode Input Range	±⅛	**±¼**		±⅛	±¼	**±¼**	LSB
Power Supply Sensitivity	V_{CC}=5 V_{DC}±5% V_{REF} = 4.75V	±⅛	**±¼**		±⅛	±¼	**±¼**	LSB
DC Characteristics								
$V_{IN(1)}$ Logical "1" Input Voltage MIN	V_{CC}=5.25V (except CLK_{IN})		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage MAX	V_{CC}=4.75V (Except CLK_{IN})		**0.8**			0.8	**0.8**	V
I_{IN}, Logical "1" Input Current MAX	V_{IN}=5.0V	0.005	**1**		0.005	1	**1**	µA
I_{IN}, Logical "0" Input Current MAX	V_{IN}=0V	−0.005	**−1**		−0.005	−1	**−1**	µA
$V_{T+(MIN)}$, Minimum CLK_{IN} Positive going Threshold Voltage		3.1	**2.7**		3.1	2.7	**2.7**	V
$V_{T(MAX)}$, Maximum CLK_{IN} Positive going Threshold Voltage		3.1	**3.5**		3.1	3.5	**3.5**	V
$V_{T-(MIN)}$, Minimum CLK_{IN} Negative going Threshold Voltage		1.8	**1.5**		1.8	1.5	**1.5**	V
$V_{T-(MAX)}$, Maximum CLK_{IN} Negative going Threshold Voltage		1.8	**2.1**		1.8	2.1	**2.1**	V
$V_{H(MIN)}$, Minimum CLK_{IN} Hysteresis (V_{T+}-V_{T-})		1.3	**0.6**		1.3	0.6	**0.6**	V
$V_{H(MAX)}$, Maximum CLK_{IN} Hysteresis (V_{T+}-V_{T-})		1.3	**2.0**		1.3	2.0	**2.0**	V
$V_{OUT(1)}$, Logical "1" Output Voltage MIN	V_{CC}=4.75V I_{OUT}=−360 µA I_{OUT}=−10 µA		**2.4** **4.5**			2.8 4.6	**2.4** **4.5**	V V
$V_{OUT(0)}$, Logical "0" Output Voltage MAX	V_{CC}=4.75V I_{OUT}=1.6 mA		**0.4**			0.34	**0.4**	V
I_{OUT}, TRI-STATE® Output	V_{OUT} = 0V	−0.01	**−3**		−0.01	−0.3	**−3**	µA

(5) For $V_{IN(-)} \geq V_{IN(+)}$ the digital output code will be 00 0000 0000. Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Electrical Characteristics (continued)

The following specifications apply for V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = 1.8 MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** All other limits $T_A = T_j$ = 25°C.

Parameter	Conditions	ADC1005BCJ			ADC1005BCJ-1, ADC1005CCJ-1			Limit Units
		Typ(1)	Tested Limit(2)	Design Limit(3)	Typ(1)	Tested Limit(2)	Design Limit(3)	
Current MAX	V_{OUT} = 5V	0.01	**3**		0.01	0.3	**3**	µA
I_{SOURCE}, Output Source Current MIN	V_{OUT}=0V	−14	**−6.5**		−14	−7.5	**−6.5**	mA
I_{SINK}, Output Sink Current MIN	V_{OUT}=5V	16	**8.0**		16	9.0	**8.0**	mA
I_{CC}, Supply Current MAX	f_{CLK}=1.8 MHz $\overline{CS}$ ="1"	1.5	**3**		1.5	2.5	**3**	mA

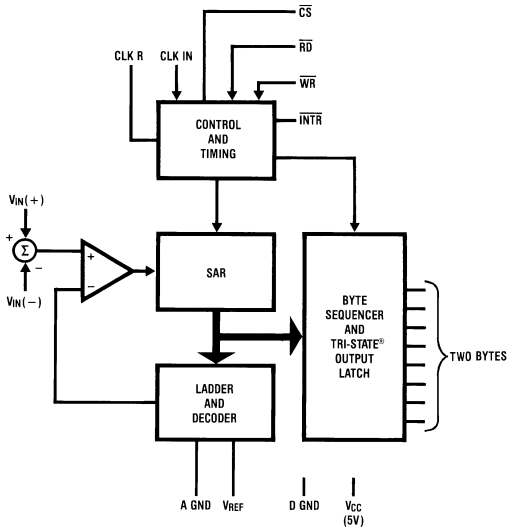
AC Electrical Characteristics

The following specifications apply for V_{CC} = 5V, V_{REF} = 5V,V_{REF} = 5V, $t_r = t_f$ = 20 ns unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** All other limits $T_A = T_j$ = 25°C.

Parameter		Conditions	Typ(1)	Tested Limit(2)	Design Limit(3)	Limit Units
f_{CLK}, Clock Frequency	MIN			0.2	0.2	MHz
	MAX			2.6	2.6	MHz
Clock Duty Cycle	MIN			40	40	%
	MAX			60	60	%
t_C, Conversion Time	MIN			80	80	$1/f_{CLK}$
	MAX			90	90	$1/f_{CLK}$
	MIN	f_{CLK}=1.8 MHz		45	45	µs
	MAX	f_{CLK}=1.8 MHz		50	50	µs
$t_{W(\overline{WR})L}$, Minimum $\overline{WR}$ Pulse Width		$\overline{CS}$ =0	100	150	150	ns
t_{ACC}, Access Time (Delay from falling edge of $\overline{RD}$ to Output Data Valid)		$\overline{CS}$ =0 C_L=100 pF, R_L = 2k	170	300	300	ns
t_{1H}, t_{0H}, TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)		R_L=10k, C_L=10 pF	125		200	ns
		R_L=2k, C_L=100 pF	145	230	230	ns
t_{WI}, t_{RI}, Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	450	ns
t_{IRS}, $\overline{INTR}$ to 1st Read Set-up Time			400	550	550	ns
C_{IN}, Capacitance of Logic Inputs			5		7.5	pF
C_{OUT}, Capacitance of Logic Outputs			5		7.5	pF

(1) Typicals are at 25°C and represent most likely parametric norm.
(2) Tested and guaranteed to TI's AOQL (Average Outgoing Quality Level).
(3) Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Functional Diagram



Typical Performance Characteristics

Logic Input Threshold Voltage vs Supply Voltage

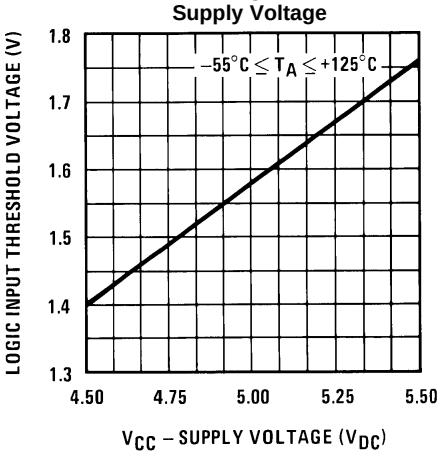


Figure 2.

Delay from Falling Edge of RD to Output data Valid vs Load Capacitance

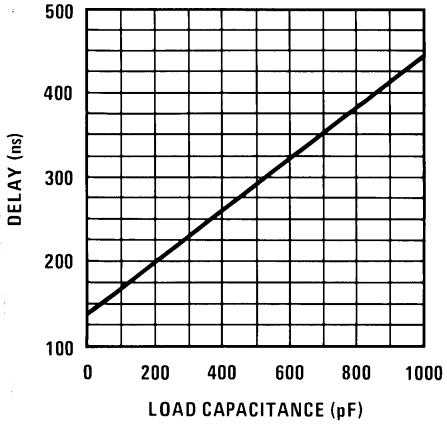


Figure 3.

CLK IN Schmitt Trip Levels vs Supply Voltage

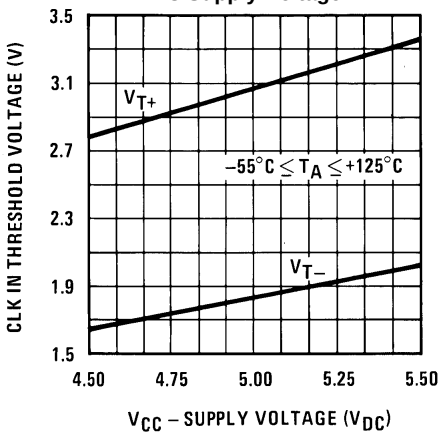


Figure 4.

Output Current vs Temperature

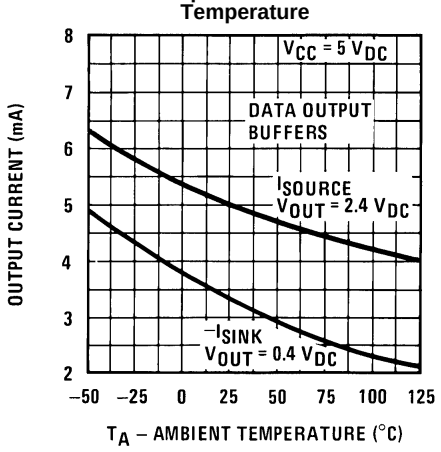


Figure 5.

Typical Linearity Error vs Clock Frequency

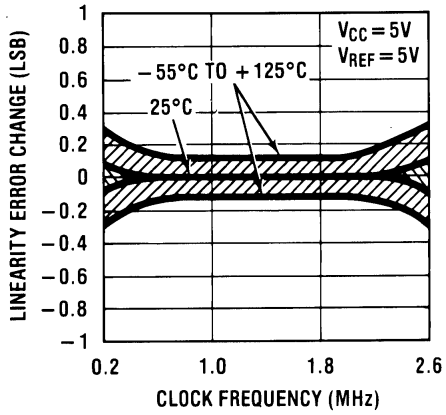


Figure 6.

TEST CIRCUIT DIAGRAMS

Timing Diagrams

Figure 7. Start Conversion

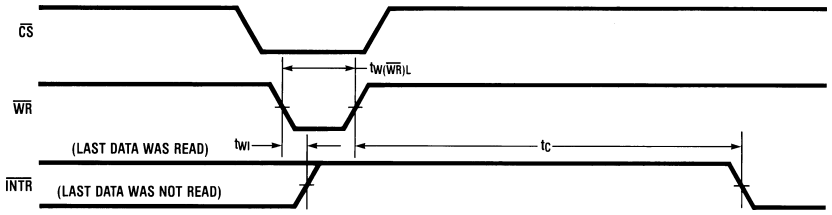
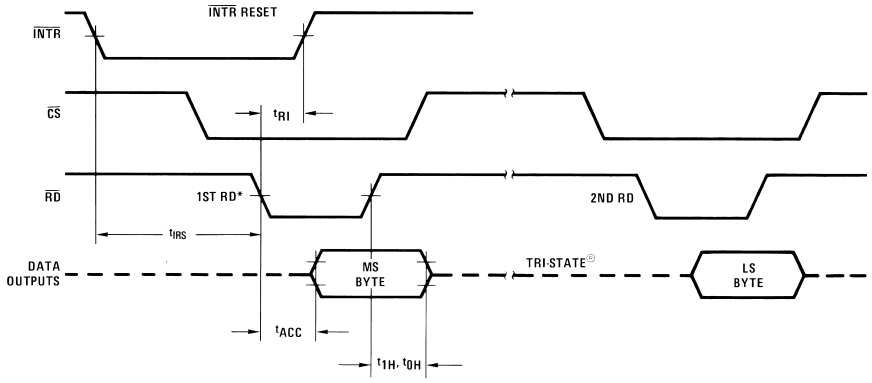


Figure 8. Output Enable and Reset INTR

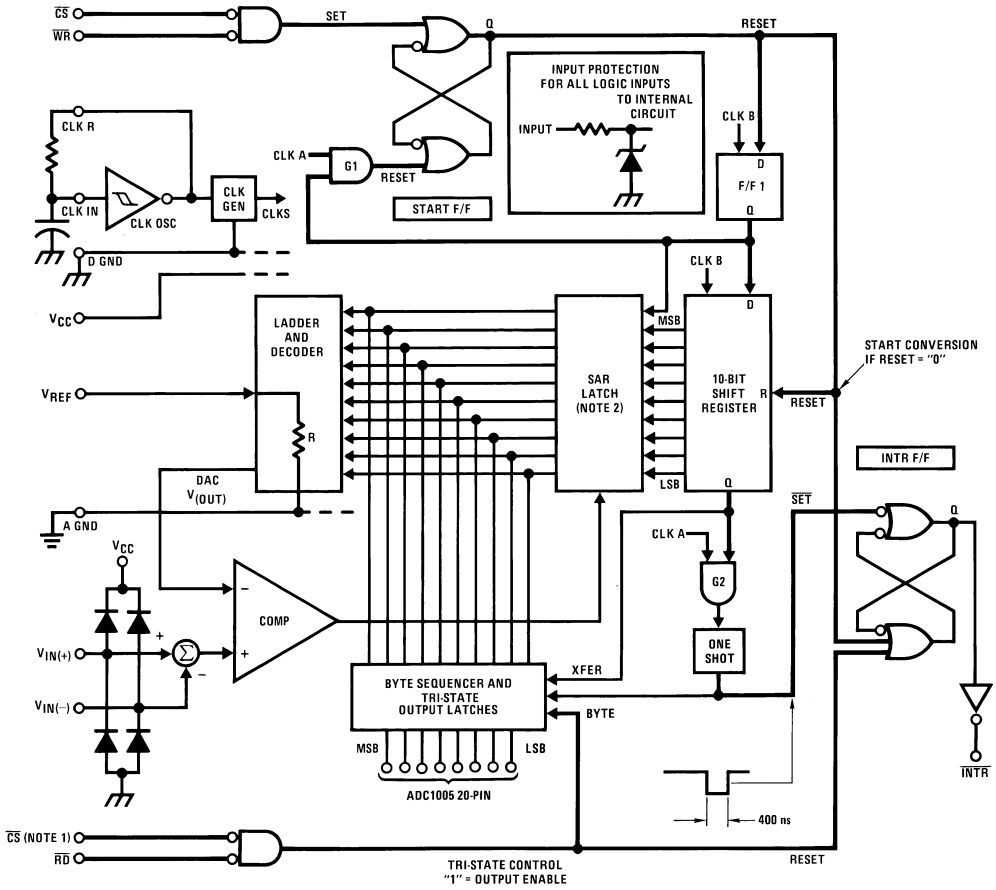


Note: All timing is measured from the 50% voltage points.

Table 1. Byte Sequencing for ADC1005

Byte Order	8-Bit Data Bus Connection							
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1st	MSB Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2
2nd	Bit 1	LSB Bit 0	0	0	0	0	0	0

Block Diagram



(1) $\overline{CS}$ shown twice for clarity.

(2) SAR=Successive Approximation Register.

Functional Description

GENERAL OPERATION

A block diagram of the A/D converter is shown in Block Diagram. All of the inputs and outputs are shown and the major logic control paths are drawn in heavier weight lines.

Converter Operation

The ADC1005 uses an advanced potentiometric resistive ladder network. The analog inputs, as well as the taps of this ladder network are switched into a weighted capacitor array. The output of this capacitor array is the input to a sampled data comparator. This comparator allows the successive approximation logic to match the analog input voltage [$V_{IN}(+) - V_{IN}(-)$] to taps on the R network. The most significant bit is tested first and after 10 comparisons (80 clock cycles) a digital 10-bit binary code (all “1”s = full-scale) is transferred to an output latch.

Starting a Conversion

The conversion is initialized by taking $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 10-bit shift register, resets the interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 10-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 10-bit shift register then can have the "1" clocked in, allowing the conversion process to continue. If the set signal were still present, this reset pulse would have no effect and the 10-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals. The converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

To summarize, on the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start after at least one of these inputs makes a low-to-high transition.*

Output Control

After the "1" is clocked through the 10-bit shift register (which completes the SAR search) it causes the new digital word to transfer to the TRI-STATE output latches. When the XFER signal makes a high-to-low transition the one shot fires, setting the INTR F/F. An inverting buffer then supplies the $\overline{INTR}$ output signal.

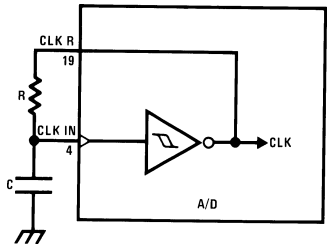
Note that this $\overline{SET}$ control of the INTR F/F remains low for approximately 400 ns. If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low) the $\overline{INTR}$ output will still signal the end of the conversion (by a high-to-low transition). This is because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled.

Free-Running and Self-Clocking Modes

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to ensure start up.

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN makes use of a Schmitt trigger as shown in Figure 9.



$$f_{CLK} \cong \frac{1}{1.1\,RC}$$

Figure 9. Self-Clocking the A/D

REFERENCE VOLTAGE

The voltage applied to the reference input of these converters defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 1024 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance of typically 4.8 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system (Figure 10) the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirements of the system references as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy (Figure 11), where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be small to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout, and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/1024$).

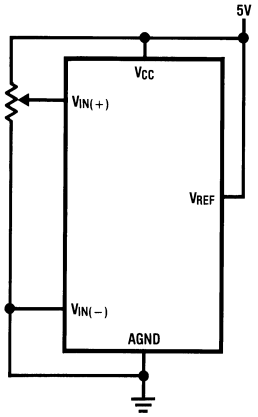


Figure 10. Ratiometric

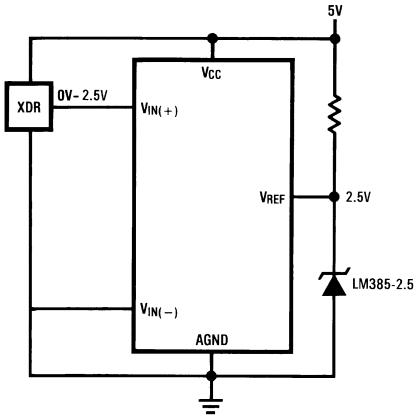


Figure 11. Absolute with a Reduced Span

THE ANALOG INPUTS

Analog Differential Voltage Inputs and Common-Mode Rejection

The differential inputs of these converters reduce the effects of common-mode input noise, which is defined as noise common to both selected "+" and "−" inputs (60 Hz is most typical). The time interval between sampling the "+" input and the "−" input is half of an internal clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal, this error is:

$$V_{ERROR(MAX)} = V_{PEAK} (2\pi f_{CM}) \times \frac{4}{f_{CLK}} \quad (1)$$

where f_{CM} is the frequency of the common-mode signal, V_{PEAK} is its peak voltage value and f_{CLK} is the clock frequency at the CLK IN pin.

For a 60 Hz common-mode signal to generate a ¼ LSB error (1.2 mV) with the converter running at 1.8 MHz, its peak value would have to be 1.46V. A common-mode signal this large is much greater than that generally found in data acquisition systems.

Input Current

Due to the sampling nature of the analog inputs, short duration spikes of current enter the "+" input and exit the "−" input at the clock rising edges during the conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period.

Input Bypass Capacitors

Bypass capacitors at the inputs will average the current spikes noted in 3.2 and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full scale. For continuous conversions with a 1.8 MHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 µA. Therefore, *bypass capacitors should not be used at the analog inputs or the V_{REF} pin* for high resistance sources (>1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a linear function of the differential input voltage.

Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* if the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications (≤0.1 kΩ) a 4700 pF bypass capacitor at the inputs will prevent pickup due to series lead induction of a long wire. A 100Ω series resistor can be used to isolate this capacitor – both the R and the C are placed outside the feedback loop – from the output of an op amp, if used.

Noise

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 1 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, can reduce system noise pickup but can create analog scale errors. See Input Current, Input Bypass Capacitors, and Input Source Resistance if input filtering is to be used.

OFFSET AND REFERENCE ADJUSTMENT

Zero Offset

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V(−) input and applying a small magnitude positive voltage to the V(+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 00 0000 0000 to 00 0000 0001 and the ideal ½ LSB value (½ LSB = 2.45 mV for V_{REF} = 5.0 V_{DC}).

The zero of the A/D normally does not require adjustment. However, for cases where $V_{IN(MIN)}$ is not ground and in reduced span applications (V_{REF} < 5V), an offset adjustment may be desired. The converter can be made to output an all zero digital code for an arbitrary input by biasing the A/D's V_{IN}(−) input at that voltage. This utilizes the differential input operation of the A/D.

Full Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input for a digital output code that is just changing from 11 1111 1110 to 11 1111 1111.

Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground), this new zero reference should be properly adjusted first. A V_{IN}(+) voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/1024) is applied to selected “+” input and the zero reference voltage at the corresponding “−” input should then be adjusted to just obtain the 000_{HEX} 001_{HEX} code transition.

The full-scale adjustment should be made [with the proper V_{IN}(−) voltage applied] by forcing a voltage to the V_{IN}(+) input given by:

$$V_{IN}(+)\ \text{FS adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{1024}\right] \quad (2)$$

where V_{MAX} = the high end of the analog input range and V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced).

The V_{REF} (or V_{CC}) voltage is then adjusted to provide a code change from $3FF_{HEX}$ to $3FE_{HEX}$. This completes the adjustment procedure.

For an example see Figure 12 below.

POWER SUPPLIES

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 µF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and the other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to the digital ground. Any V_{REF} bypass capacitors, analog input filters capacitors, or input signal shielding should be returned to the analog ground point .

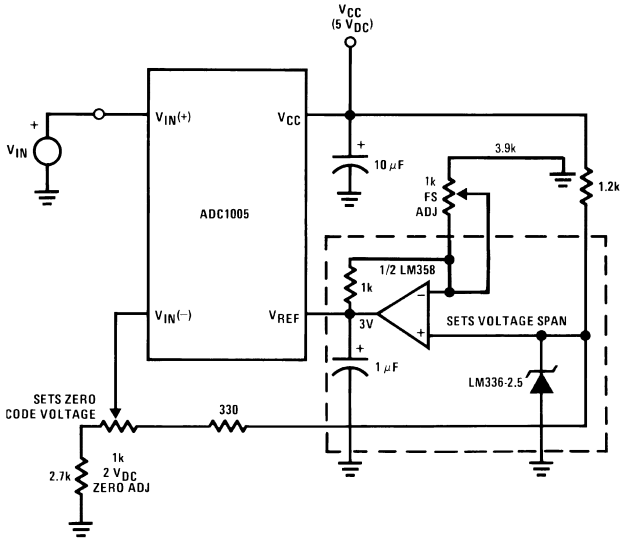
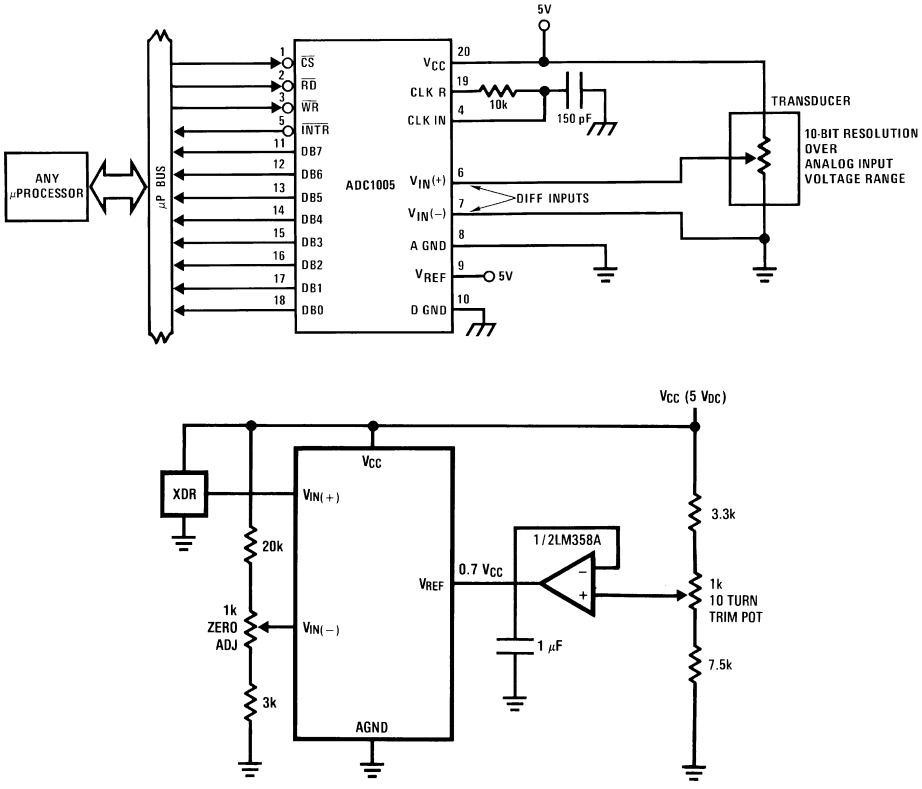


Figure 12. Zero-Shift and Span-Adjust (2V ≤ V_{IN} ≤ 5V)

Typical Applications



$V_{IN}(-) = 0.15\ V_{CC}$
15% of V_{CC} ≤ V_{XDR} ≤ 85% of V_{CC}

Figure 13. Operating with Ratiometric Transducers

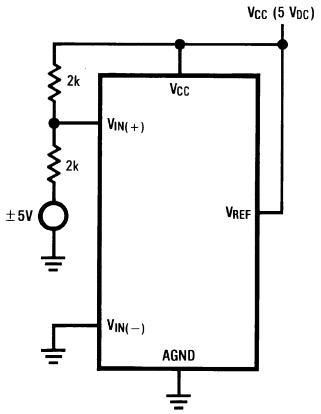


Figure 14. Handling ±5V Analog Inputs

TRI-STATE Test Circuits and Waveforms

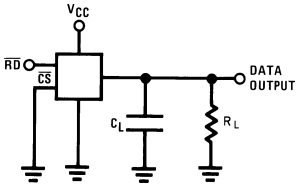
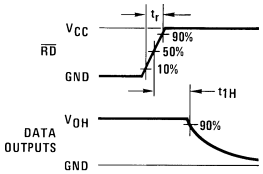


Figure 15. t_{1H}



t_r=20 ns

Figure 16. t_{IH}, C_L=10 pF

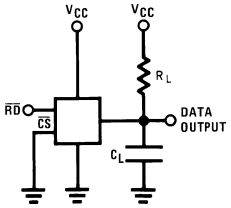
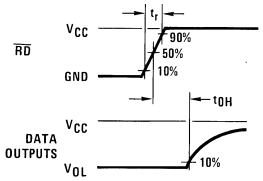


Figure 17. t_{0H}



t_r=20 ns

Figure 18. t_{IH}, C_L=10 pF

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F **Page**

- Changed layout of National Data Sheet to TI format 12

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