VD6803/VD6803T

3.15 megapixel EDoF image sensor

Features

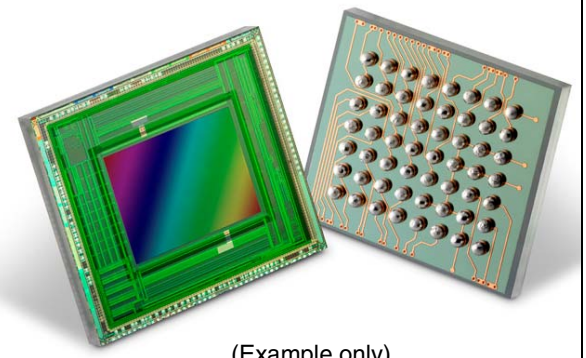
- 3.15 megapixel resolution sensor (2048 x 1536)
- Integrated Software Lens™ for extended depth of field (EDoF)
- Conventional reconstructed wafer or chipscale package utilizing through-silicon via technology (TSV)
- 10-bit parallel data interface, horizontal and vertical syncs, 80 MHz (max) clock. I^2C command interface
- Fully SMIA 1.0 profile 0 compliant
- Ultra low power standby mode
- Analog binning (2x2)
- On-the-fly defect correction
- Internal regulator for VDDCore

Description

The VD6803 is a high performance 3.15 megapixel CMOS image sensor with integrated Software Lens™ technology. The device provides excellent image quality at focus distances down to 15 cm when used with a suitable matching lens. The VD6803 is intended for use across a wide range of imaging applications where the cost, power consumption or physical size of conventional autofocus solutions is prohibitive.

The VD6803 is equipped with a 10-bit parallel interface capable of generating 3 MP (QXGA) raw Bayer images at 20 fps (80 MHz). The device is controlled over a 2-wire I^2C compliant serial interface (400 KHz).

The VD6803 is available either as a conventional wafer for wire-bond applications or reflowable chipscale package utilizing through-silicon via (TSV) technology.



(Example only)

The COB size is 5.6 x 5.6 mm. The TSV package is just 5.6 x 5.6 x 0.8mm in size.

The VD6803 also offers an ultra low power consumption hardware standby mode consuming less than 150 µW (typ.).

Technical specification

Pixel resolution	2048 x 1536 (QXGA)
Sensor technology	IMG175 ST's 90 nm based CMOS imaging process
Pixel size	1.75 µm x 1.75 µm
Exposure control	+ 81 dB
Analogue gain	+ 24 dB (max)
Digital gain	+ 6 dB (max)
Supply voltages	Analog: 2.8V Digital: 1.8V / 2.8V
Typical power consumption	< 400 mW (viewfinder mode) < 700 mW (capture mode)
COB size	5.6 x 5.6 mm
TSV size (l x w x h)	5.6 x 5.6 x 0.8 mm

Contents

List of tables

List of figures

1 Overview

The VD6803 3.15 MP image sensor produces raw 3.15 MP digital video data at up to 20 frames per second. The image data is digitized using an internal 10-bit column ADC. The resulting pixel data is formatted and transmitted over a 10-bit parallel interface including horizontal and vertical synchronizations signals and a pixel clock signal qualifying valid data. The maximum sustained pixel clock rate is 80 MHz.

The sensor is fully configurable through a I^2C serial interface. The I^2C interface is specified in the following document: SMIA 1.0 Part 2: CCP2 Specification Class 2.

The module is available either as a conventional reconstructed wafer for wire-bond applications (VD6803) or reflowable chipscale package using TSV technology (VD6803T). The TSV package is 5.6 mm x 5.6 mm x 0.8 mm in size. The COB package is 5.6 mm x 5.6 mm in size.

2 Die specification

2.1 Silicon thickness

The VD6803 is available in a 56-bump TSV package (VD6803T) or conventional reconstructed wafer. The VD6803 wafer is delivered with a standard thickness of 180 µm.

2.2 Layout, optical centre, scribe widths

All dimensions and coordinates are referenced to the die centre.

Table 1. Die size

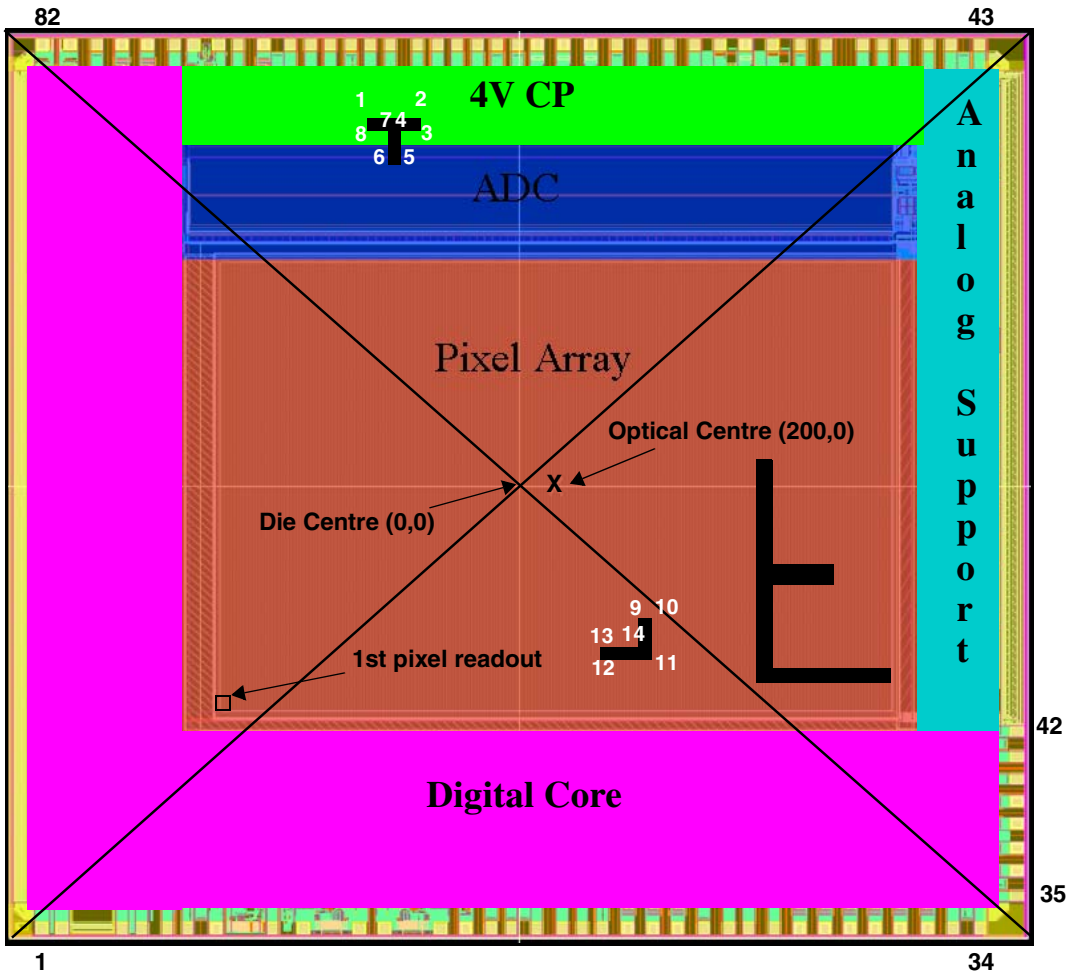
	Conditions	X size (µm)	Y size (µm)	Area (mm2)
Die size	Including seal	5500	5500	30.25
	Including scribe	5600	5600	31.36

Table 2. Array details

Parameter	X (µm)	Y (µm)
Die centre	0	0
Array centre	200	0

2.3 Bond pad positions and numbers

Figure 1. Bond pad positions, optical centre and die orientation



Note: 'T' and 'L' fiducials on the top side of the die can be used for orientation and pin 1 identification. Refer to Table 3 and Table 4 for fiducial coordinates.

Table 3. Fiducial coordinates (Die center reference)

Fiducial Point No.(1)	X coordinate	Y coordinate	X coordinate	Y coordinate
	As drawn / µm	As drawn / µm	After shrink/ µm	After shrink/ µm
1	-568.845	1802.000	No shrink	No shrink
2	-208.845	1802.000	No shrink	No shrink
3	-208.845	1682.000	No shrink	No shrink
4	-328.845	1682.000	No shrink	No shrink
5	-328.845	1442.000	No shrink	No shrink
6	-448.845	1442.000	No shrink	No shrink
7	-448.845	1682.000	No shrink	No shrink
8	-568.845	1682.000	No shrink	No shrink
9	853.150	-1435.000	No shrink	No shrink
10	973.150	-1435.000	No shrink	No shrink
11	973.150	-1795.000	No shrink	No shrink
12	613.150	-1795.000	No shrink	No shrink
13	613.150	-1675.000	No shrink	No shrink
14	853.150	-1675.000	No shrink	No shrink

1. Refer to *Figure 1 on page 10* for locations of fiducial points identified.

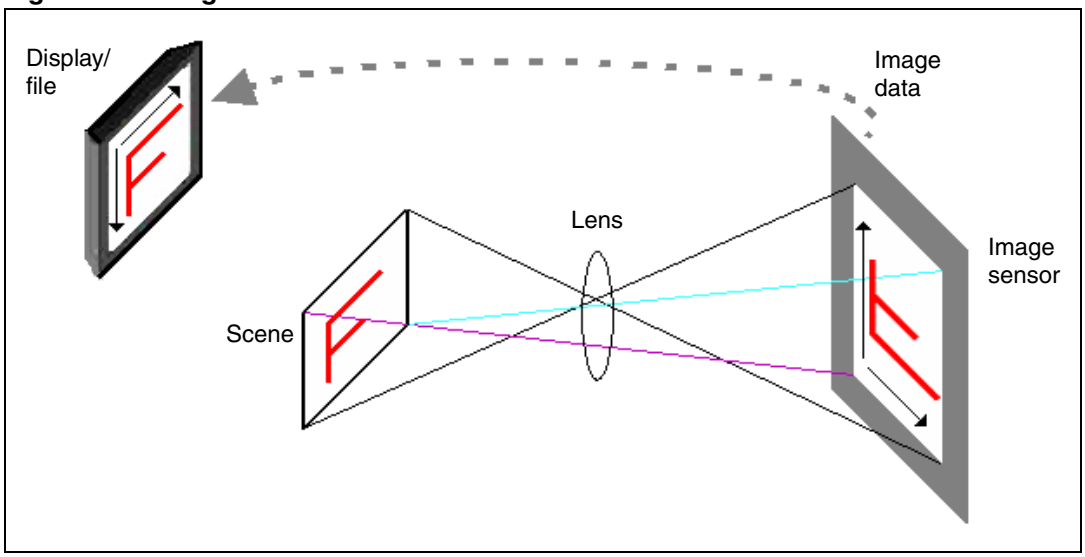
Table 4. Fiducial coordinates (Optical center reference)

Fiducial Point No.(1)	X coordinate	Y coordinate	X coordinate	Y coordinate
	As drawn / µm	As drawn / µm	After shrink/ µm	After shrink/ µm
1	-768.845	1802.000	No shrink	No shrink
2	-408.845	1802.000	No shrink	No shrink
3	-408.845	1682.000	No shrink	No shrink
4	-528.845	1682.000	No shrink	No shrink
5	-528.845	1442.000	No shrink	No shrink
6	-648.845	1442.000	No shrink	No shrink
7	-648.845	1682.000	No shrink	No shrink
8	-768.845	1682.000	No shrink	No shrink
9	653.150	-1435.000	No shrink	No shrink
10	773.150	-1435.000	No shrink	No shrink
11	773.150	-1795.000	No shrink	No shrink
12	413.150	-1795.000	No shrink	No shrink
13	413.150	-1675.000	No shrink	No shrink
14	653.150	-1675.000	No shrink	No shrink

1. Refer to *Figure 1 on page 10* for locations of fiducial points identified.

The actual image of the scene projected through the lens onto the pixel array means that it is necessary to readout the array starting at the bottom-left corner so that the final displayed image is correct.

Figure 2. Image orientation



This document is related to the die, so the image orientation (depicted in this document with an “F”) shows the image as it is really being captured by the sensor.

The pixel readout is fully programmable (x and y flip) but the default read fashion is from left to right and bottom to top. Hence, the “F” orientation.

2.4 Bond pad details for COB package

Table 5. Bond pad positions and names for COB package

Pad #	Ext. signal	Int. signal	Pad X co-ord	Pad Y co-ord	Comments
1	VDDCORE	VDD	-2573	-2689	Core digital supply 1V2 (generated by internal regulator)
2	VDDCORE	VDD	-2466	-2689	
3	VDIG	VDDE	-2141	-2689	Digital I/O supply: Parallel interface = 2V8 (compliant 1V8)
4	VDIG	VDDE	-2035	-2689	
5	DGND	GNDE	-1898	-2689	Digital I/O gnd
6	DGND	GND	-1786	-2689	
7	XSHUTDOWN	XSHUTDOWN	-1643	-2689	Active low reset
8	VDIG	VDDE	-1347	-2689	
9	CCP2_DATAP	CCP2_DATAP	-1181	-2689	Unconnected in a Parallel interface configuration
10	CCP2_DATAN	CCP2_DATAN	-878	-2689	
11	CCP2_CLKN	CCP2_CLKN	-742	-2689	

Table 5. Bond pad positions and names for COB package (continued)

Pad #	Ext. signal	Int. signal	Pad X co-ord	Pad Y co-ord	Comments
12	CCP2_CLKP	CCP2_CLKP	-439	-2689	Unconnected in a Parallel interface configuration
13	EXTCLK	EXTCLK	-285	-2689	Master input clock
14	VDDCORE	VDD	-146	-2689	
15	VDDCORE	PLLVDD	-41	-2689	In wire bond applications, connect to vddcore.
16	VDIG	VDDE	96	-2689	
17	DGND	PLLGND	236	-2689	
18	DGND	GND	343	-2689	
19	DGND	GNDE	450	-2689	
20	D0	D0	588	-2689	Parallel Data Output
21	D1	D1	724	-2689	
22	D2	D2	859	-2689	
23	VDDCORE	VDD	998	-2689	
24	DGND	GND	1135	-2689	
25	DGND	GNDE	1242	-2689	
26	VDIG	VDDE	1379	-2689	
27	D4	D4	1516	-2689	
28	D3	D3	1653	-2689	
29	PCLK	PCLK	1788	-2689	Parallel port output pixel clock
30	D6	D6	1923	-2689	
31	D5	D5	2059	-2689	
32	D7	D7	2207	-2689	
33	VDIG	VDDE	2344	-2689	
34	DGND	GNDE	2495	-2689	
35	DGND	GND	2690	-2493	
36	D9	D9	2690	-2337	
37	D8	D8	2690	-2199	
38	VSYNC	VSYNC	2690	-2051	Parallel Port Vertical Sync
39	HSYNC	HSYNC	2690	-1915	Parallel Port Horizontal Sync
40	HV	HV	2690	-1779	For NVM programming. Connect to 7.9V during programming. Otherwise leave floating.
41	AGND	AVSSVIDEO	2690	-1643	
42	VANA	AVDDVIDEO	2690	-1492	2V8 Analog Supply

Table 5. Bond pad positions and names for COB package (continued)

Pad #	Ext. signal	Int. signal	Pad X co-ord	Pad Y co-ord	Comments
43	VANA	AVDDVIDEO	2487	2690	
44	VANA	AVDDVIDEO	2332	2690	
45	VANA	AVDDPOWER	2213	2690	
46	AGND	AVSSVIDEO	2077	2690	
47	AGND	AVSSVIDEO	1966	2690	
48	AGND	AVSSPOWER	1858	2690	
49	DGND	GND	1658	2690	
50	VDDCORE	VDD	1521	2690	
51	VTGLO	VTGLO	1370	2690	No connect
52	VCAP	SUPPLY4V	1225	2690	Internal 4V supply. Decouple with 470 nF to AGND.
53	NEGAVDD	NEGAVDD	1084	2690	No connect
54	AGND	AVSSVIDEO	951	2690	
55	VANA	AVDDVIDEO	812	2690	
56	DGND	GND	667	2690	
57	VDDCORE	VDD	529	2690	
58	ATEST0	ATEST0	389	2690	No connect
59	ATEST1	ATEST1	243	2690	No connect
60	ATEST2	ATEST2	101	2690	No connect
61	VDDCORE	VDD	-7	2690	
62	VDDCORE	VDD	-117	2690	
63	VANA	AVDDVIDEO	-223	2690	
64	AGND	AVSSVIDEO	-332	2690	
65	VANA	AVDDVIDEO	-440	2690	
66	VANA	AVDDPOWER	-546	2690	
67	AGND	AVSSVIDEO	-693	2690	
68	AGND	AVSSPOWER	-801	2690	
69	VDDCORE	VDD	-907	2690	
70	DGND	GND	-1017	2690	
71	DGND	GND	-1123	2690	
72	DGND	GNDE	-1233	2690	
73	GPIO_DFT3	GPIO_DFT3	-1376	2690	No connect
74	VDIG	VDDE	-1515	2690	
75	PORTEST	PORTEST	-1620	2690	No connect

Table 5. Bond pad positions and names for COB package (continued)

Pad #	Ext. signal	Int. signal	Pad X co-ord	Pad Y co-ord	Comments
76	PORSGN	PORSGN	-1755	2690	No connect
77	DGND	GND	-1859	2690	
78	GPIO_DFT_2	GPIO_DFT2	-2004	2690	No connect
79	GPIO_DFT1	GPIO_DFT1	-2142	2690	No connect
80	VDDCORE	VDD	-2278	2690	
81	SDA	SDA	-2420	2690	
82	SCL	SCL	-2572	2690	

2.5 Bond pad details for TSV package

Table 6. Bond pad positions and names for TSV package

Pad #	Ext. signal	Pad X co-ord	Pad Y co-ord	Comments
1	VANA	2.1	2.25	2V8 analog supply
2	ATEST0	1.5	2.25	No connect
3	VCAP	0.9	2.25	Internal 4V supply. Decouple with 470 nF to AGND.
4	VANA	0.3	2.25	
5	DGND	-0.3	2.25	Digital I/O GND
6	GPIO_DFT_3	-0.9	2.25	No connect
7	GPIO_DFT_2	-1.5	2.25	No connect
8	GPIO_DFT_1	-2.1	2.25	No connect
9	NC	2.1	1.75	
10	AGND	1.5	1.75	
11	NC	0.9	1.75	
12	DGND	0.3	1.75	
13	NC	-0.3	1.75	
14	VDIG	-0.9	1.75	Digital I/O supply: Parallel interface = 2V8 (compliant 1V8)
15	NC	-1.5	1.75	
16	SDA	-2.1	1.75	
17	VDIG	2.1	1.25	
18	NC	1.5	1.25	
19	NC	0.9	1.25	
20	NC	0.3	1.25	

Table 6. Bond pad positions and names for TSV package (continued)

Pad #	Ext. signal	Pad X co-ord	Pad Y co-ord	Comments
21	NC	-0.3	1.25	
22	NC	-0.9	1.25	
23	NC	-1.5	1.25	
24	SCL	-2.1	1.25	
25	HV	2.1	0.75	For NVM programming. Connect to 7.9V during programming. Otherwise leave floating.
26	NC	-2.1	0.75	
27	HSYNC	2.1	0.25	Parallel Port Horizontal Sync
28	NC	-2.1	0.25	
29	VSYNC	2.1	-0.25	Parallel Port Vertical Sync
30	NC	-2.1	-0.25	
31	NC	2.1	-0.75	
32	VDDCORE	-2.1	-0.75	Connected internally for TSV.
33	D9	2.1	-1.25	Parallel Data Output
34	D7	1.5	-1.25	
35	PCLK	0.9	-1.25	Parallel Port Output Pixel Clock
36	D0	0.3	-1.25	
37	DGND	-0.3	-1.25	
38	EXTCLK	-0.9	-1.25	Master input clock
39	NC	-1.5	-1.25	
40	VDIG	-2.1	-1.25	
41	D8	2.1	-1.75	
42	D5	1.5	-1.75	
43	D3	0.9	-1.75	
44	D1	0.3	-1.75	
45	NC	-0.3	-1.75	
46	CCP2_CLKN	-0.9	-1.75	Unconnected in a Parallel interface configuration
47	CCP2_DATAN	-1.5	-1.75	
48	DGND	-2.1	-1.75	
49	DGND	2.1	-2.25	
50	D6	1.5	-2.25	
51	D4	0.9	-2.25	
52	D2	0.3	-2.25	
53	VDIG	-0.3	-2.25	

Table 6. Bond pad positions and names for TSV package (continued)

Pad #	Ext. signal	Pad X co-ord	Pad Y co-ord	Comments
54	CCP2_CLKP	-0.9	-2.25	Unconnected in a Parallel interface configuration
55	CCP2_DATAP	-1.5	-2.25	
56	XSHUTDOWN	-2.1	-2.25	Active low reset

2.6 Pad opening sizes

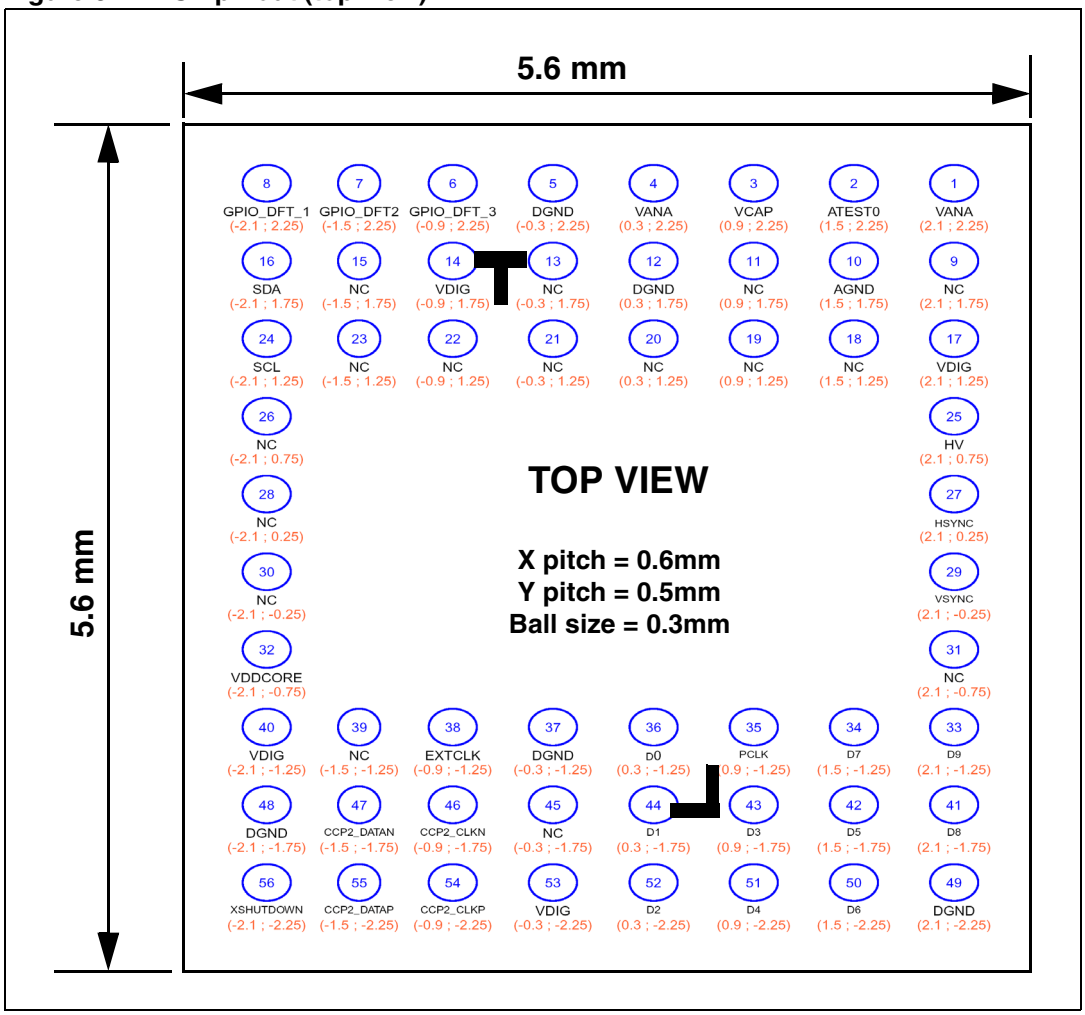
Table 7. Pad openings

	X (µm)	Y (µm)
Pad openings	65	70

2.7 TSV information

Figure 3 shows the pinout of the VD6803T 56-bump TSV wafer-level package. The TSV device can be assembled using a conventional lead-free reflow process.

Figure 3. TSV pinout (top view)

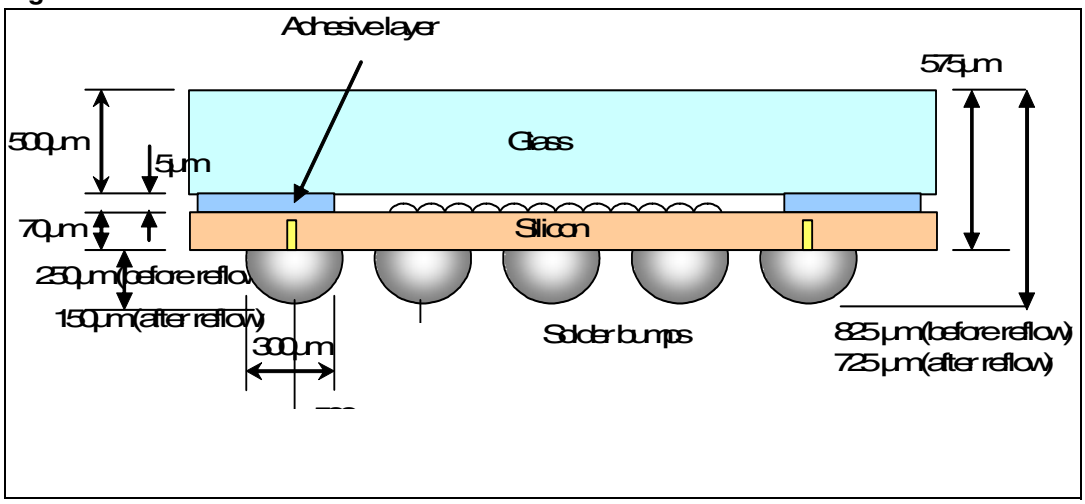


Note: 1 'T' and 'L' fiducials on the top side of the die can be used for orientation and pin 1 identification. There is also a 'T' fiducial and other features on the bump side. The 'T' and 'L' fiducials shown in Figure 3 are provided as an example and do not show the correct location.

2 Figure 3 is a top view looking down on the package. The die orientation is the same as in Figure 1 on page 10.

The Bump pitch is 600 µm in X and 500 µm in Y. Other useful dimensions are shown in *Figure 4*.

Figure 4. TSV Z-dimensions

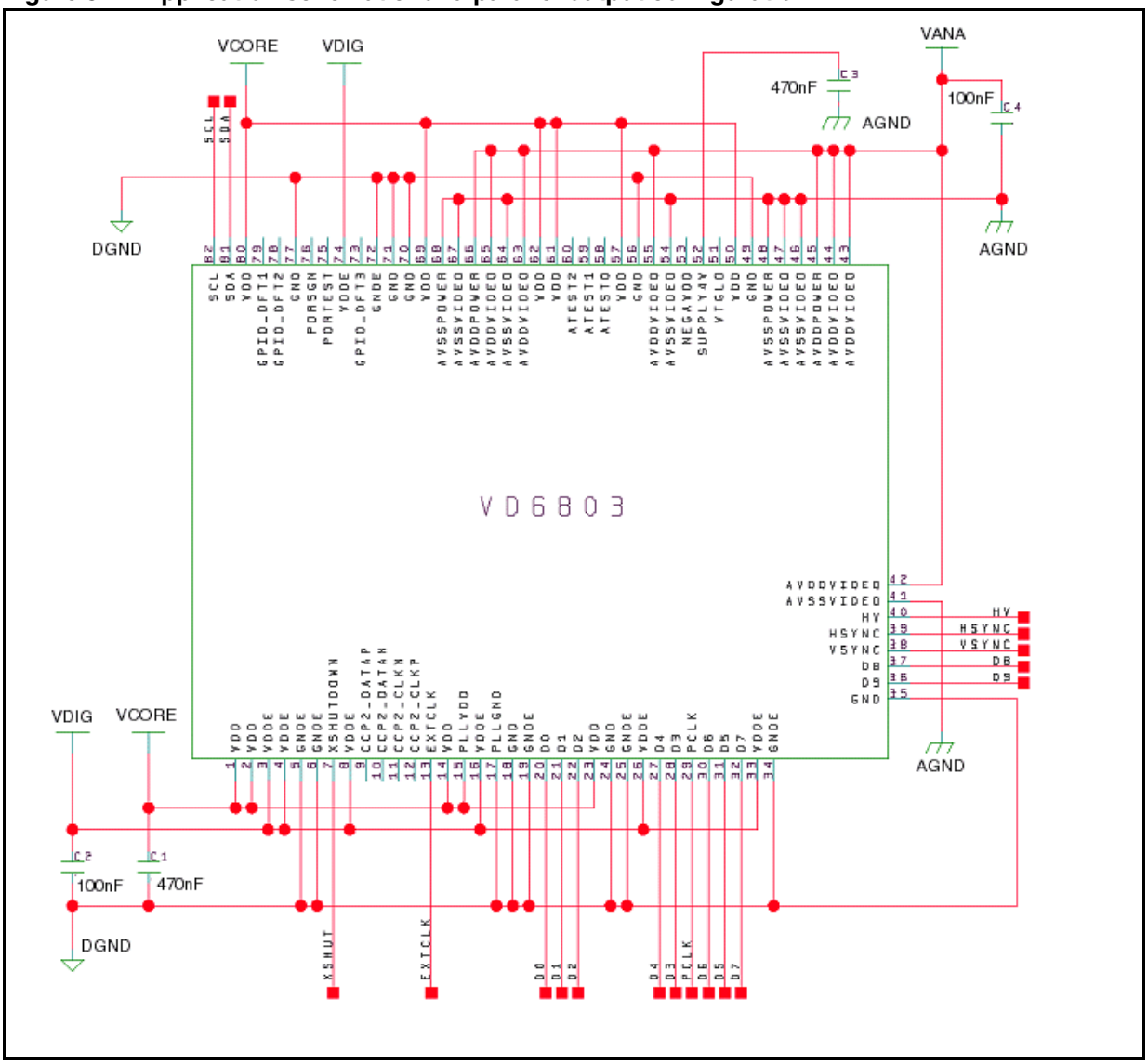


2.8 Application circuits

2.8.1 Application circuit for COB (chip-on-board)

Typical wire-bonded application circuit for parallel interface configuration is shown in *Figure 5 on page 20*.

Figure 5. Application schematic for a parallel output configuration



Note: 1 VDDCORE is an internal 1.2V core voltage that does not require an external supply. All VDDCORE pins however must be connected. VDDCORE requires a minimum capacitance of 400 nF at the rated voltage of 1.2V.

2 Capacitors should be situated as close to the supply pads as possible.

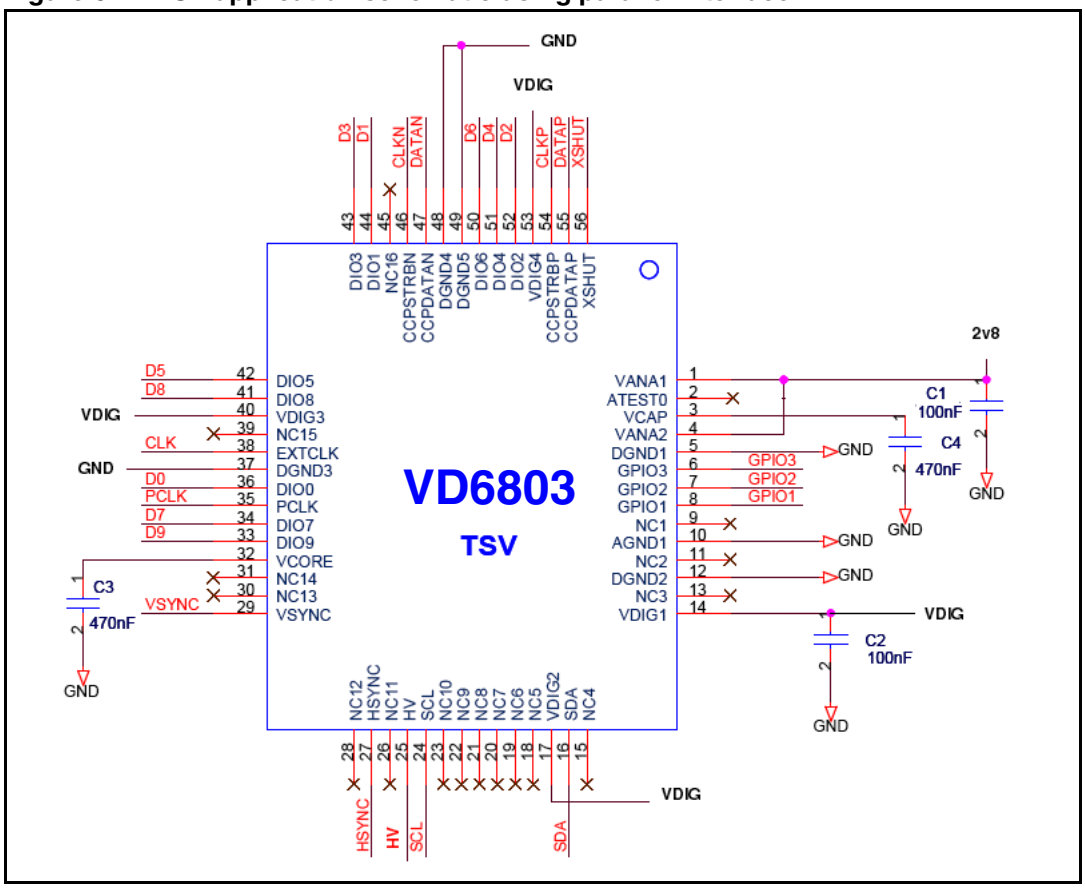
3 VDIG is 2v8 or 1V8 in a parallel output configuration.

4 The capacitor on SUPPLY3V6 is a charge pump capacitor. It must have a minimum capacitance of 470 nF at the rated voltage of 3.6V

2.8.2 TSV application circuit

The die to module substrate connectivity is shown in *Figure 6*.

Figure 6. TSV application schematic using parallel interface



Note: 1 VDDCORE is an internal 1.2V core voltage that does not require an external supply. All VDDCORE pins however must be connected. VCORE requires a minimum capacitance of 400 nF at the rated voltage of 1.2V.

2 Capacitors should be situated as close to the supply pads as possible.

3 VDIG is 2v8 or 1V8 in a parallel output configuration.

4 The capacitor on SUPPLY3V6 is a charge pump capacitor. It must have a minimum capacitance of 470 nF at the rated voltage of 3.6V

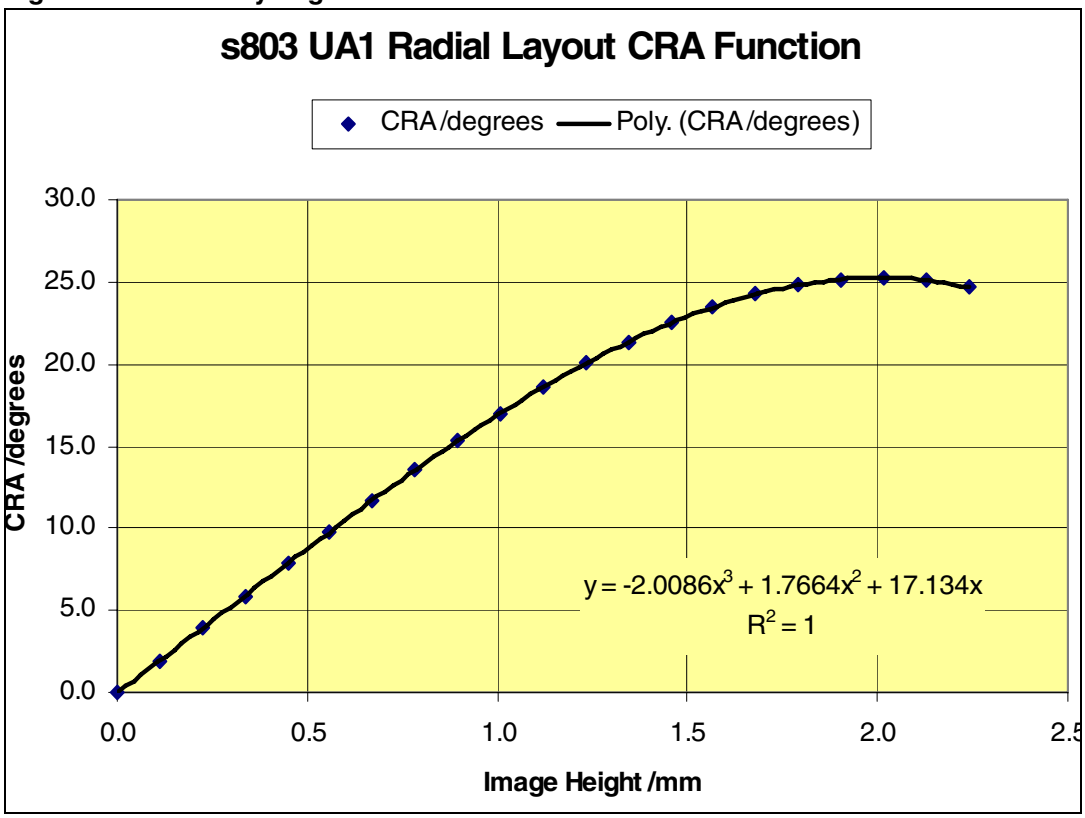
2.9 Chief ray angle (CRA)

The VD6803 radial microlens pattern is described in *Table 8* and *Figure 7 on page 23*.

Table 8. Chief ray angle

Image height / mm	CRA / degrees
0.000	0.000
0.112	1.938
0.224	3.904
0.336	5.880
0.448	7.850
0.560	9.796
0.672	11.702
0.784	13.551
0.896	15.325
1.008	17.009
1.120	18.584
1.232	20.034
1.344	21.342
1.456	22.492
1.568	23.466
1.680	24.247
1.792	24.818
1.904	25.163
2.016	25.264
2.128	25.104
2.240	24.668

Figure 7. Chief ray angle



2.10 Delivery/shipping method

For conventional wafer, tested dice can be delivered in two possible ways

- Option /RW
  - Reconstructed Wafer (8 inches), placed on UV tape and mounted on metal wafer rings then packaged in plastic containers for shipment.
  - Both wafer rings and boxes must be shipped back to STMicroelectronics.
- Option /WP
  - Tested dice delivered in Waffle Pack
  - Tray 6 x 6 (36 pcs), bulk 720 pcs

More detailed information on delivery methods is available on request.

3 Functional description

This chapter details the main blocks in the device, see:

- *Section 3.1: Analog video block*
- *Section 3.2: Digital video block on page 25*
- *Section 3.3: Device operating modes on page 25*

This chapter also describes:

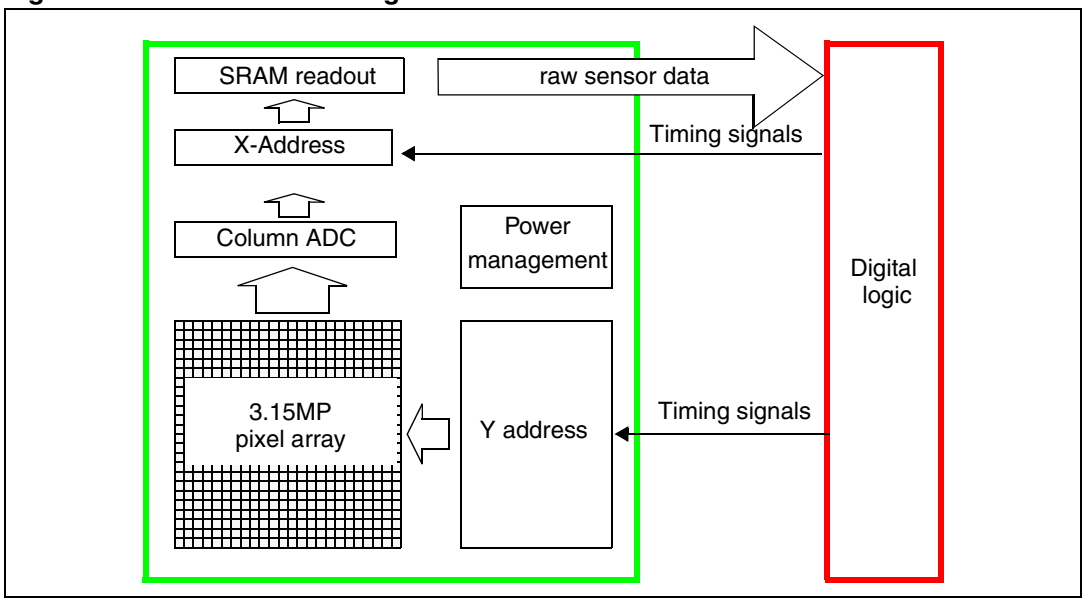
- the device's operating modes, see *Section 3.4 on page 26*
- clock and frame rate control, see *Section 3.5 on page 30*
- control and video interface formats, see *Section 3.6 on page 32*

3.1 Analog video block

3.1.1 Block diagram

The analog video block, shown in *Figure 8*, consists of a 3.15 MP resolution pixel array, power management circuitry. The digital block provides all timing signals to drive the analog block.

Figure 8. Overview of analog video block



Pixel voltage values are read out and digitized using the address decoders and column ADC.

3.2 Digital video block

3.2.1 Features

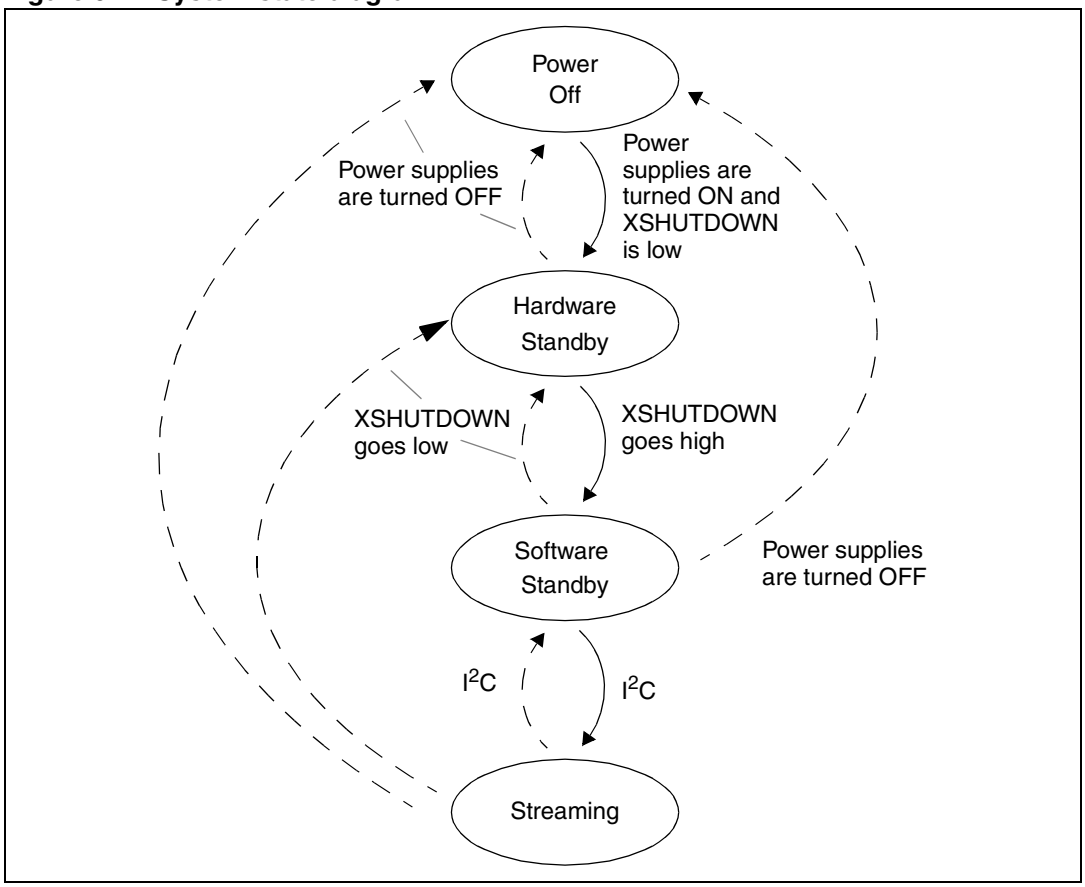
- Frame rate: 20 frame/s maximum can be reduced down to less than 3 frame/s (3.15 MP) using frame extension.
- Automatic dark calibration to ensure consistent video level over varying scenes.
- On-chip power-on-reset cell.
- Output format: 3.15 MP 2056 x 1544 (maximum).

3.2.2 Dark calibration algorithm

VD6803 runs a dark calibration algorithm on the raw image data to control the video offsets caused by dark current. This ensures that a high quality image is output over a range of operating conditions. First frame dark level is correctly calibrated, for subsequent frames the adjustment of the dark level is damped by a leaky integrator function to avoid possible frame to frame flicker.

3.3 Device operating modes

Figure 9. System state diagram



3.3.1 Power off

Power supplies are off.

3.3.2 Hardware standby

This is the lowest power consumption mode. I^2C communications are not supported in this mode. The clock input pad, PLL and the video blocks are powered down. This state is entered by pulling the control pin XSHUTDOWN down.

3.3.3 Software standby

Software standby mode preserves the contents of the I^2C register map. I^2C communications are supported in this mode. The software standby mode is selected using a serial interface command. If this state is entered from hardware standby the data pads remain high impedance. If this state is entered from streaming then the data pads go high impedance at the end of the current frame. At this point the video block and PLL power down. The internal video timing is reset to the start of a video frame in preparation for the enabling of active video. The values of the serial interface registers like exposure and gain are preserved. The system clock must remain active when communicating with the sensor.

This state is entered by releasing the device from hard reset by: setting XSHUTDOWN high, writing 0x00 to the mode control register (0x0100) or commanding a soft reset by writing 0x01 to the software reset register (0x0103). Note that after a soft reset or the transition of XSHUTDOWN to high, all registers are returned to their default values.

3.3.4 Streaming

The VD6803 streams live video. This mode is entered by writing 0x01 to the mode control register (0x0100).

3.4 Power management

VD6803 requires a dual power supply. The analog circuits are powered by a nominal 2.8 V supply. The digital logic and digital I/O are powered by a 2.8 V supply or 1.8 V supply. Different sections of the sensor are powered depending on the system state. See *Table 9* for details.

Table 9. Power management matrix

Mode	Functional block powered down					Video data inhibit
	I^2C	Digital	PLL and pins(1)	Output pins	Analog	
Hardware standby	Yes	Yes	Yes	Yes	Yes	Yes
Software standby	No	Yes	Yes	Yes	Yes	Yes
Streaming	No	No	No	No	No	No

1. PLL (Phase Locked Loop) generates fast clock which can be used by other chips.

3.4.1 Power-up procedure

The digital and analog supply voltages can be powered up in any order for example, VDIG then VANA or VANA then VDIG. However VANA must be up soon after VDIG see *Table 10* for timing constraints.

On power up the on-chip power-on reset cell ensures that the I^2C register values are initialized correctly to their default values.

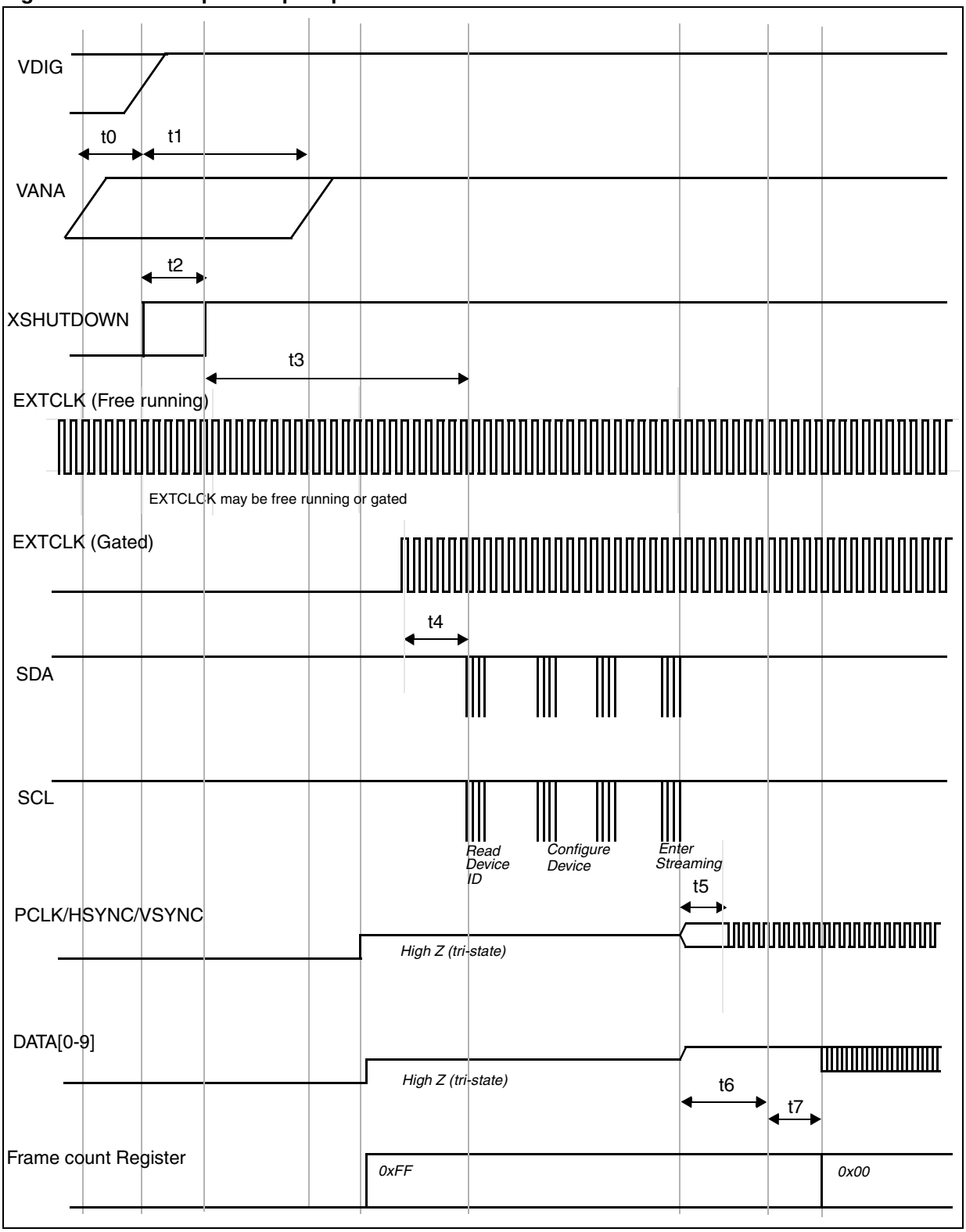
The EXTCLK clock can either be initially low and then enabled during software standby mode or EXTCLK can be a free running clock.

Table 10. Power-up sequence timing constraints

Symbol	Parameter	Min.	Max.	Units
t0	VANA rising – VDIG rising	VANA and VDIG may rise in any order		ns
t1	VDIG rising – VANA rising	-	1.7(1)	ms
t2	VDIG rising – XSHUTDOWN rising	XSHUTDOWN must rise coincident with, or later than, VDIG		us
t3	XSHUTDOWN – First I^2C transaction	2800(2)	-	EXTCLK cycles
t4	Minimum no of EXTCLK cycles prior to the first I^2C transaction	2800(2)	-	EXTCLK cycles
t5	PLL start up/lock time	-	1	ms
t6	Entering streaming mode – First frame start sequence (fixed part)	-	10	ms
t7	Entering streaming mode – First frame start sequence (variable part) = Integration time	fine_integration_ time_min	-	ms

1. The rise of VANA can be later but the image quality of the first frames of data may not be within specification, contact ST Microelectronics for more details.
2. With an EXTCLK of 27 MHz, 2800 cycles equates to 103.7us; with an EXTCLK of 6 MHz, 2800 cycles equates to 466.7us.

Figure 10. VD6803 power-up sequence



3.4.2 Internal power-on reset (POR)

The VD6803 internally performs a power-on reset (POR) when the 1V2 Vcore digital supply rises through the trigger level, Vtrig_rising. Similarly, if the 1V2 Vcore digital power supply falls through the trigger level, Vtrig_falling, then the power-on reset will also trigger.

Definitions:

Rise threshold voltage (VTRIGR) is the supply voltage level that is recognized by the POR as voltage “HIGH”. Only after the supply reaches this level does the output of POR change to high level if it is off, after a specified amount of delay.

Fall threshold voltage (VTRIGF) is the supply voltage level that is recognized by the POR as voltage “LOW”. Only after the supply reaches this level does the output of POR change to low (ground) level if it is on.

Burst width (pw). Burst is the negative pulse riding the supply signal. The burst width is measured as the amount of duration for which the supply signal dropped beyond the threshold levels. Bursts whose time duration is below ‘pw’ will not be reflected on POR output signal.

Delay duration (TPOR) is defined as the time duration for which POR stays off before re-powering. Each reset of POR will impart a specified delay duration before POR re-powers.

Figure 11. POR timing

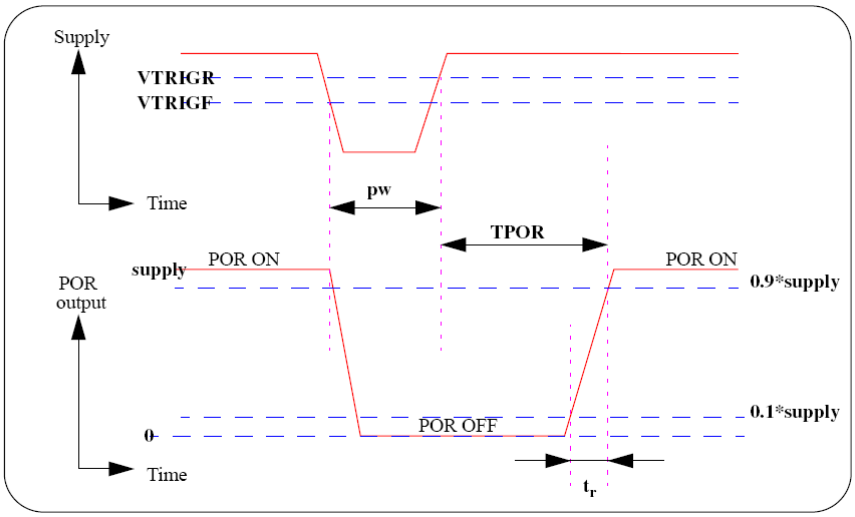


Table 11. POR cell characteristics

Symbol	Constraint	Min	Typ.	Max.	Units
VTRIGR	POR rise voltage detection			0.95	V
VTRIGF	POR fall voltage detection	0.35			V
Tburst (pw)	Burst filter		2		µs
Tpor	Delay duration		20		µs

3.4.3 Failsafe signals

All signals going into the VD6803 must be at either a low state or high impedance when power is removed from the device. The exceptions to this rule are the EXTCLK, XSHUTDOWN and the I^2C signals. These pads have been designed to be high impedance when the VD6803 is powered-down. This means that the input signal on the specified pads can be either high or low with no leakage problems.

3.5 Clock and frame rate timing

3.5.1 Video frame rate control

The output frame rate of VD6803 can be reduced by extending either the line length or the frame length. The extension is achieved by adding extra blanking bytes at the end of a line or “blank” video lines to act as timing padding. The frame rate can be reduced from the default 20 frame/s at 3.15 MP resolution to less than 3 frame/s at 3.15 MP resolution.

The advantage of the frame extension approach is that it does not reduce the pixel readout rate or the active frame time and therefore does not introduce unwanted motion distribution effects to the image.

3.5.2 PLL and clock input

The VD6803 has an embedded PLL block. This block generates all necessary internal clocks from an input range defined in *Table 12*. The input clock pad accepts up to 27 MHz signals.

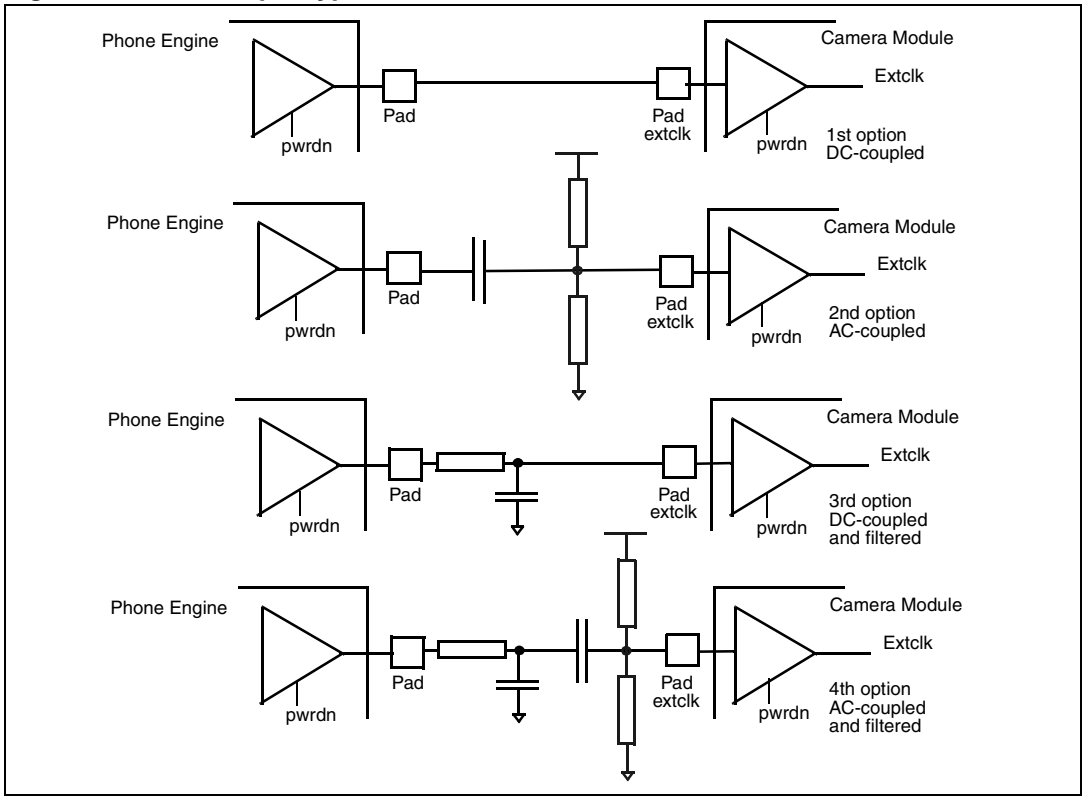
Table 12. System input clock frequency range

Minimum (MHz)	Maximum (MHz)
6	27

3.5.3 Clock input type

As required by the SMIA specification the VD6803 can receive the clock types shown in *Figure 12*.

Figure 12. Clock input types



The clock is fail-safe/high impedance when either AC or DC coupled and in any mode including the power off state.

3.6 Control and video interface formats

Image data is transferred from the VD6803 through a high speed 10 bits parallel link including horizontal and vertical synchronization output. The serial control data is transferred to and from the VD6803 on an I^2C bus.

3.6.1 I^2C serial control bus

The internal registers in VD6803 can be configured by a master device through an I^2C bus (SDA, SCL). VD6803 sends and receives commands over this bus at up to 400 Kbits/s.

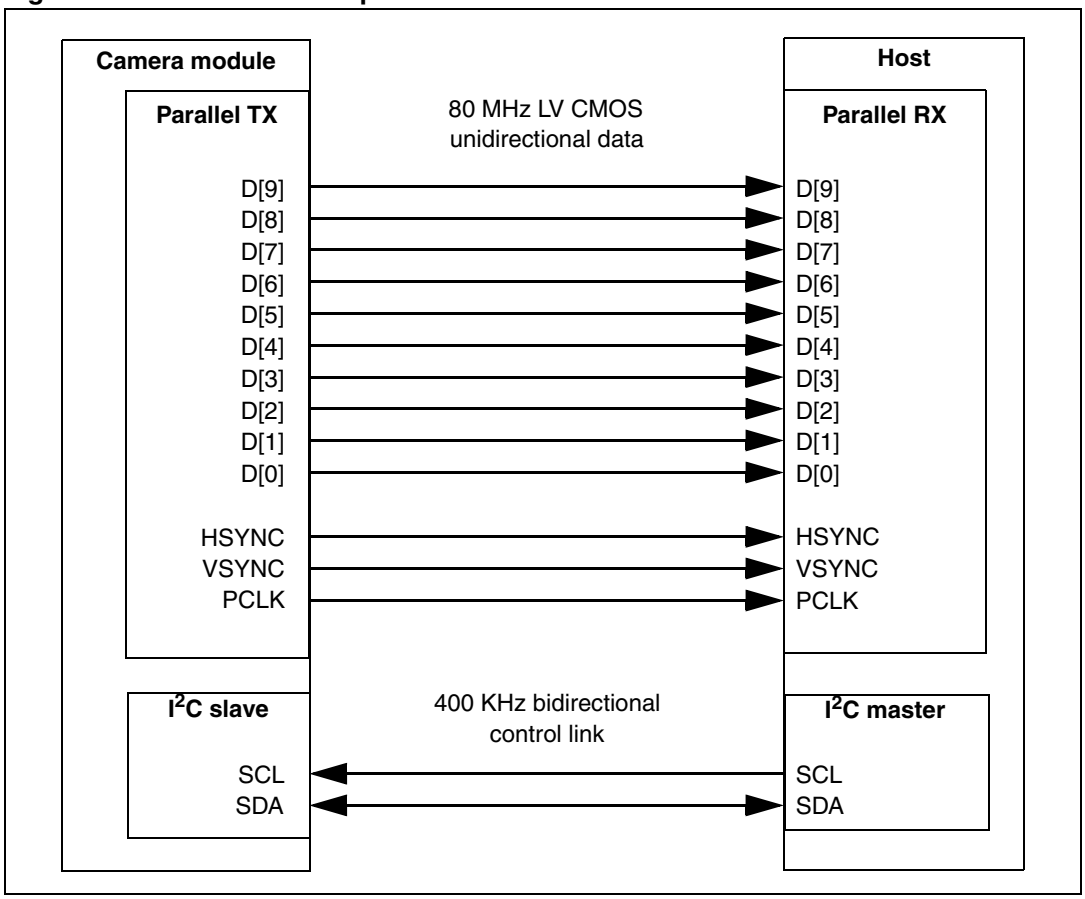
3.6.2 Parallel data link

The parallel data link supports the transmission of raw Bayer data at 3.15 MP resolution up to 20 frame/s.

The main features are:

- 3.15 MP @ 20 fps @ 10-bit
- 1V8/2V5/2V8 signalling levels
- 10-bit parallel video output port
- output pixel rate up to 80 MSPS
- full resolution peak output rates of between 6 MSPS and 80 MSPS are supported
- separate horizontal and vertical sync outputs
- fully programmable clock and sync, both position (sync only) and polarity
- tri-state output control allows multiple camera systems (port disabled upon reset)
- programmable frame/line blanking value

Figure 13. LV CMOS 10-bit parallel interface



4 Camera I²C interface

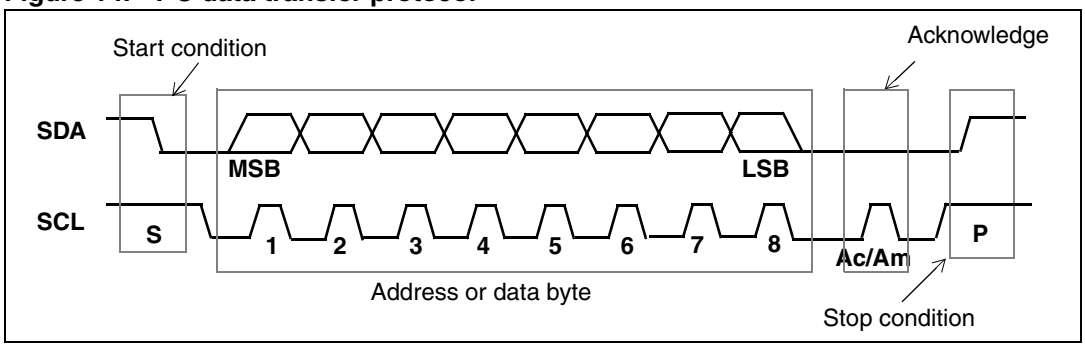
4.1 I²C interface

This section specifies the camera control interface (I²C). The I²C-type interface uses 1.8 V I/O with two signals: serial data line (SDA) and serial clock line (SCL). I²C is used for control data transfer. Each device connected to the bus is using a unique address and a simple master/slave relationships exists.

Both SDA and SCL lines are connected to a positive supply voltage through pull-up resistors located on the baseband. Lines are only actively driven low. A high condition occurs when lines are floating and the pull-up resistors pull lines up. When no data is transmitted both lines are high. See *Chapter 9: Electrical characteristics on page 83* for electrical and timing information.

Clock signal (SCL) generation is performed by the master device[(a)]. The master device initiates data transfer. The I²C bus on the camera module has a maximum speed of 400 Kbits/s and uses a device address of 0x20.

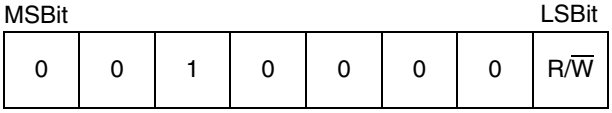
Figure 14. I²C data transfer protocol



Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit, Ac for camera acknowledge and Am for master acknowledge (baseband or hardware accelerator whichever is I²C bus master). The internal data is produced by sampling SDA at a rising edge of SCL. The external data must be stable during the high period of SCL. The exceptions to this are start (S) or stop (P) conditions when SDA falls or rises respectively, while SCL is high.

A message contains a series of bytes preceded by a start condition and followed by either a stop or repeated start (another start condition but without a preceding stop condition) followed by another message. The first byte contains the device address (0x20) and also specifies the data direction. If the least significant bit is low (that is, 0x20) the message is a master write to the slave. If the lsb is set (that is, 0x21) then the message is a master read from the slave.

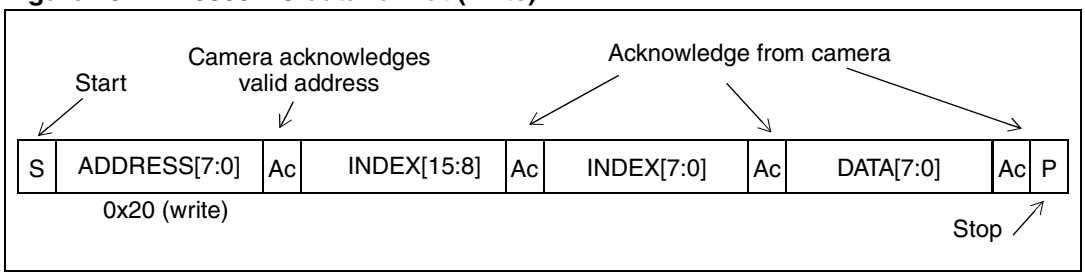
Figure 15. VD6803 I²C device address



a. The camera module is a slave device.

All serial interface communications with the sensor must begin with a start condition. The sensor acknowledges the receipt of a valid address by driving the SDA wire low. The state of the read/write bit (lsb of the address byte) is stored and the next byte of data, sampled from SDA, can be interpreted. During a write sequence the second and third bytes received provide a 16-bit index which points to one of the internal 8-bit registers.

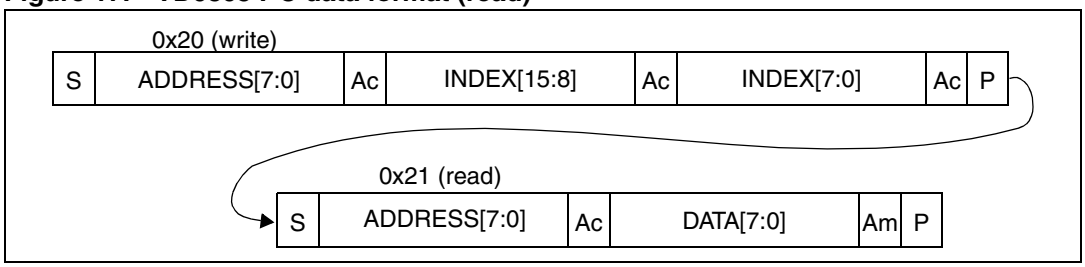
Figure 16. VD6803 I²C data format (write)



As data is received by the slave it is written bit by bit to a serial/parallel register. After each data byte has been received by the slave, an acknowledge is generated, the data is then stored in the internal register addressed by the current index.

During a read message, the contents of the register addressed by the current index is read out in the byte following the device address byte. The contents of this register are parallel loaded into the serial/parallel register and clocked out of the device by the falling edge of SCL.

Figure 17. VD6803 I²C data format (read)



At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device (that is, the camera module for a write and the baseband for a read).

A message can only be terminated by the bus master, either by issuing a stop condition or by a negative acknowledge (that is, NOT pulling the SDA line low) after reading a complete byte during a read operation.

The interface also supports auto-increment indexing. After the first data byte has been transferred, the index is automatically incremented by 1. The master can therefore send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a *stop* condition. If the auto increment feature is used the master does not have to send address indexes to accompany the data bytes.

Figure 18. VD6803 I²C data format (sequential write)

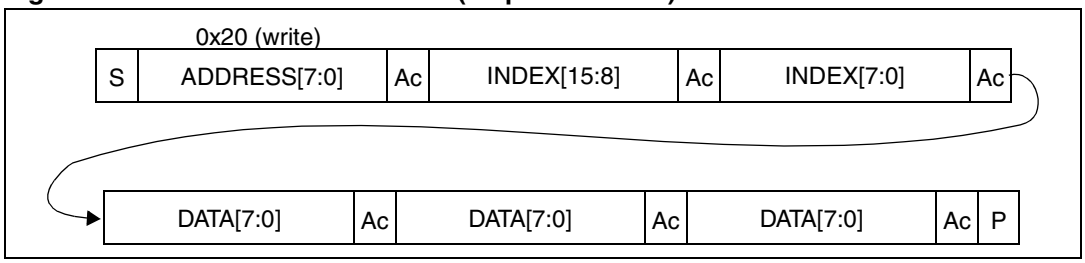
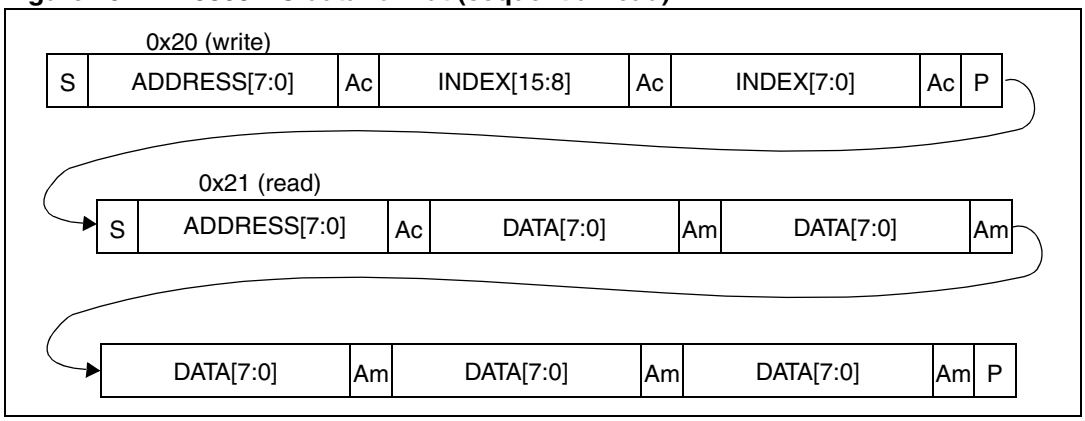


Figure 19. VD6803 I²C data format (sequential read)



4.2 VD6803 I²C register map

The registers are grouped according to function with each group occupying a pre-allocated region of the address space. This scheme is purely a conceptual feature and is not related to the actual hardware implementation. All registers can be found at the I²C device address of 0x20.

The VD6803 registers are grouped into several different classes, see *Table 13*.

Table 13. I²C register groupings

I²C indices	Description
Configuration registers [0x0000 to 0x0FFF]	
0x0000 to 0x00FF	Status registers
0x0100 to 0x01FF	Setup registers - operating modes
0x0200 to 0x02FF	Integration time and gain parameters
0x0300 to 0x03FF	video timing registers
0x0500 to 0x05FF	Image compression registers
0x0600 to 0x06FF	Test pattern registers

Table 13. I²C register groupings (continued)

I²C indices	Description
Parameter limit registers [0x1000 to 0x1FFF]	
0x1000 to 0x10FF	Integration time and gain parameters limits
0x1100 to 0x11FF	Video timing parameter limits
0x1200 to 0x12FF	Image scaling parameter limits
0x1300 to 0x13FF	Image compression parameter limits
0x1400 to 0x14FF	Color matrix registers
Manufacturer specific registers [0x3000 to 0x3FFF]	
0x3000 to 0x3FFF	Manufacturer specific registers.

Any internal register that can be written to, can also be read from. There are also read only registers that contain device status information, (for example, design revision details).

A read instruction from an unused register location returns the value 0x00. A read instruction from a reserved address can return any value.

A write instruction to a reserved or unused register location is illegal and the effect of such a write is undefined. It is the responsibility of the host system to only write to register locations which have been defined.

4.2.1 Multi-byte registers index space

The following section defines the valid locations for MS and LS bytes of 16-bit and 32-bit register values.

For 16-bit wide registers the index of the MS byte must be a multiple of 2. The LS bit of the 16-bit index must be zero.

Table 14. Valid indices for the MS and LS data bytes of 16-bit wide registers

16-bit register			
MS data byte	**LS data byte**	**MS data byte**	**LS data byte**
0xFFFC	0xFFFD	0xFFFE	0xFFFF
0xFFF8	0xFFF9	0xFFFA	0xFFFB
0xFFF4	0xFFF5	0xFFF6	0xFFF7
0xFFF0	0xFFF1	0xFFF2	0xFFF3
:	:	:	:
0x000C	0x000D	0x000E	0x000F
0x0008	0x0009	0x000A	0x000B
0x0004	0x0005	0x0006	0x0007
0x0000	0x0001	0x0002	0x0003

For 32-bit wide registers the index of the MS byte must be a multiple of 4, that is, the two LS bits of the 16-bit index must be zero, see *Table 15*.

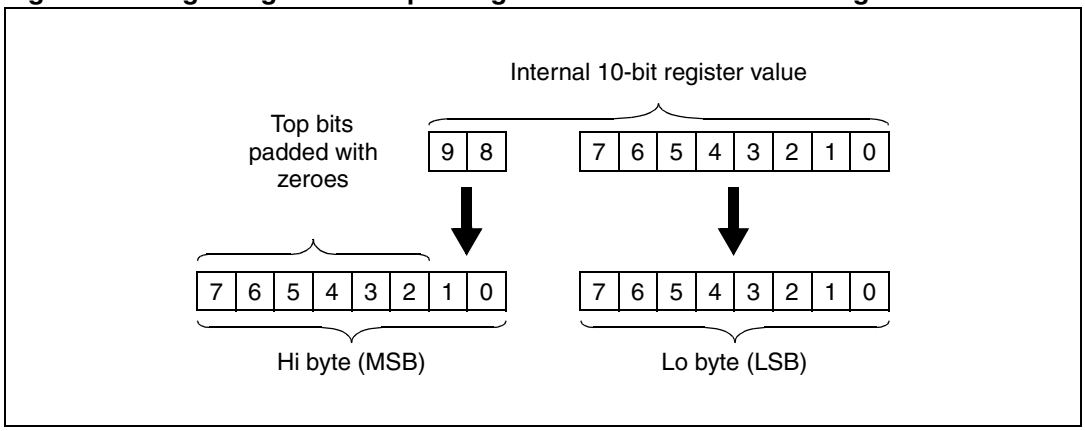
Table 15. Valid 16-bit indices for the MS and LS data bytes of 32-bit wide registers

32-bit register			
MS data byte	**LS data byte**	**MS data byte**	**LS data byte**
0xFFFC	0xFFFD	0xFFFE	0xFFFF
0xFFF8	0xFFF9	0xFFFA	0xFFFB
0xFFF4	0xFFF5	0xFFF6	0xFFF7
0xFFF0	0xFFF1	0xFFF2	0xFFF3
:	:	:	:
0x000C	0x000D	0x000E	0x000F
0x0008	0x0009	0x000A	0x000B
0x0004	0x0005	0x0006	0x0007
0x0000	0x0001	0x0002	0x0003

4.2.2 Data alignment within I²C registers

If the width of an internal register is narrower than the I²C 8-bit, 16-bit or 32-bit register which reports it's value, then the register value is right-aligned within the I²C register and the unused MS bits are padded with zeroes.

Figure 20. Right alignment for packing 10-bit data into two 8-bit registers



4.2.3 Valid register data types

The contents of the registers can represent a number of different data types, see *Table 16*. The register map uses this coding to help with the interpretation of the contents of each register.

Table 16. Valid register data types

Data type	Name	Range	Description
8UI	8-bit unsigned integer	0 to 255	-
8SI	8-bit signed integer	-128 to 127	Two's complement notation
16UI	16-bit unsigned integer	0 to 65535	-
16SI	16-bit signed integer	-32768 to 32767	Two's complement notation
16UR	16-bit unsigned iReal	0 to 255.99609375	08.08 fixed point number. 8 integer bits (MS Byte), 8 fractional bits (LS Byte)
16SR	16-bit signed iReal	-128 to 127.9960375	Two's complement notation, 8 fractional bits
32UR	32-bit unsigned iReal	0 to 65535.99998474	16.16 fixed point number. 16 integer bits (MS 2 bytes), 16 fractional bits (LS 2 bytes)
32SR	32-bit signed iReal	-32768 to 32767.99998474	Two's complement notation,16 fractional bits
32SF	32-bit IEEE floating-point number	As per IEEE 754	As per IEEE 754. 1 sign bit, 8 exponent bits, 23 fractional bits
8C or 16C	8-bit or 16-bit Coded	-	This indicates that the value is decoded to select one of several functions or modes.
8B or 16B	8 or 16 Bits	-b	Each bit represents a specific function or mode.

4.2.4 Register default values

The register's default registers values are expressed as dotted hexadecimal numbers.

4.3 Register map

4.3.1 Status registers [0x0000 to 0x000F]

Table 17. Status registers [0x0000 to 0x000F]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0000	Hi	model_id	16UI	03.54	RO	16-bit imaging array model number that is, 0x0323 = 803_{10}
0x0001	Lo					
0x0002		revision_number	8UI	20	RO	Bits 3:0 NVM version Bits 7:4 Imaging array silicon version ID: VD6803 cut 1.0 = 0x00 VD6803 cut 1.1 = 0x10 VD6803 cut 1.2 = 0x20
0x0003		manufacturer_id	8C	01	RO	Manufacturer ID: STMicroelectronics
0x0004		smia_version	8C	0A	RO	0x0A: SMIA 1.0
0x0005		frame_count	8UI	FF	RO	Frame count increments by 1 on each frame. Rolls over at 255 to 0. When moving from video to sleep the frame count will be reset to 255. The frame count will also be reset to 255 after a soft reset (register 0x0103).
0x0006		pixel_order	8C	00	RO	Color pixel readout order. Defines the order of the colour pixel readout. Changes with mirror and flip (register 0x0101). 0x00: GR/BG - normal 0x01: RG/GB - horizontal mirror 0x02: BG/GR - vertical flip 0x03: GB/RG - vertical flip and horizontal mirror
0x0008	Hi	data_pedestal	16UI	00.04	RO	The video data is offset by 4. This value is programmable using registers 0x3006/7 but changing this value could affect image quality.
0x0009	Lo					
0x000C		pixel_depth	8UI	0A	RO	Pixel data resolution.

4.3.2 Frame format description registers [0x0040 to 0x007F]

For a full description of the frame format description please refer to *Section 5.1: Frame format on page 64*.

Table 18. Frame format description registers [0x0040 to 0x007F]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0040		frame_format_model_type	8C	01	RO	Generic frame format. 0x01: 2-byte data format.(1)
0x0041		frame_format_model_subtype	8C	22	RO	Contains the number of 2-byte data format descriptors used. Upper nibble defines the number of column descriptors that is, 2. The lower nibble defines the number of row descriptors that is, 2
0x0042	Hi	frame_format_descriptor_0	16C	58.08	RO	Pixel data code: 5 (visible columns) number of pixels : readout dependent (Maximum of 2056)
0x0043	Lo					
0x0044	Hi	frame_format_descriptor_1	16C	20.08	RO	Pixel data code: 2 (dummy columns) Number of pixels: 8
0x0045	Lo					
0x0046	Hi	frame_format_descriptor_2	16C	10.02	RO	Pixel data code: 1 (embedded data lines) Number of lines: 2
0x0047	Lo					
0x0048	Hi	frame_format_descriptor_3	16C	56.08	RO	Pixel data code: 5(visible lines) Number of lines: readout dependent
0x0049	Lo					

1. See Section 4.5 of SMIA 1.0 functional specification.

4.3.3 Analogue gain description registers [0x0080 to 0x0097]

These registers are not dynamic but are required to be output on the status line so that it is possible to interpret the meaning of the analogue gain code(s). For a full description of the analogue gain description registers please refer to *Section 6.4.1: Analogue gain model on page 75*.

Table 19. Analogue gain description [0x0080 to 0x0097]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0080	Hi	analogue_gain_capability	16B	00.00	RO	Analogue gain capability 0: single global analogue gain only
0x0081	Lo					
0x0084	Hi	analogue_gain_code_min	16UI	00.00	RO	Minimum recommended analogue gain code that is, 0 (x1 gain)
0x0085	Lo					
0x0086	Hi	analogue_gain_code_max	16UI	00.F0	RO	Maximum recommended analogue gain code that is, 240 (x16 gain)
0x0087	Lo					
0x0088	Hi	analogue_gain_code_step	16UI	00.10	RO	Analogue gain code step size(1)
0x0089	Lo					
0x008A	Hi	analogue_gain_type	16UI	00.00	RO	Analogue gain type
0x008B	Lo					
0x008C	Hi	analogue_gain_m0	16SI	00.00	RO	Analogue gain m0 constant. m0 = 0
0x008D	Lo					
0x008E	Hi	analogue_gain_c0	16SI	01.00	RO	Analogue gain c0 constant. c0 = 256
0x008F	Lo					
0x0090	Hi	analogue_gain_m1	16SI	FF.FF	RO	Analogue gain m1 constant. m1 =-1
0x0091	Lo					
0x0092	Hi	analogue_gain_c1	16SI	01.00	RO	Analogue gain c1 constant c1 = 256
0x0093	Lo					

1. For above gains of 0xE0, the step size is four. See *Figure 33 on page 75* for gain values. This is an additional feature of the VD6803 is outside of the SMIA specification.

4.3.4 Setup registers [0x0100 to 0x01FF]

Table 20. Setup registers [0x0100 to 0x01FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0100		mode_select	8UI	00	RW	Mode select 0x00: Software standby 0x01: Streaming Refer to *Section 3.3: Device operating modes on page 25*.
0x0101		image_orientation	8B	00	RW	Image orientation, that is, horizontal mirror and vertical flip. Bit 0: 0 - no mirror, 1 - horizontal mirror enable Bit 1: 0 - no flip, 1 - vertical flip enable
0x0103		software_reset	8UI	00	RW	Software reset. Setting this register to 1 resets the sensor to its power up defaults. The value of this bit is also reset. 0x00: normal 0x01: soft reset Refer to *Section 3.3: Device operating modes on page 25*.
0x0104		grouped_parameter_hold	8UI	00	RW	The grouped parameter hold register disables the consumption of integration, gain and video timing parameters. 0x00: consume parameters as normal 0x01: hold parameters Refer to *Section 6.4.3: Integration and gain parameter re-timing on page 77*.
0x0105		mask_corrupted_frames	8UI	00	RW	Setting this register to 1 prevents the sensor outputting frames that have been corrupted by video timing parameter changes. 0x00: normal 0x01: mask corrupted frames
0x0120		gain_mode	8UI	00	RO	0x00: Global analogue gain. VD6803 supports only global gain modes.

4.3.5 Integration time and gain registers [0x0200 to 0x02FF]

These registers are used to control the image exposure. See *Section 6.4: Exposure and gain control on page 75* for more information.

Table 21. Integration time and gain registers [0x0200 to 0x02FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0200	Hi	fine_integration_time	16UI	01.5E	RW	Fine integration time (pixels).
0x0201	Lo					
0x0202	Hi	course_integration_time	16UI	00.00	RW	Coarse integration time (lines).
0x0203	Lo					
0x0204	Hi	analogue_gain_code_global	16UI	00.00	RW	Global analogue gain parameter (coded). See *Section 6.4.1: Analogue gain model on page 75* for details of how to use this parameter.
0x0205	Lo					
0x020E	Hi	digital_gain_greenr	16UR	01.00	RW	Gain code for greenr channel
0x020F	Lo					
0x0210	Hi	digital_gain_red	16UR	01.00	RW	Gain code for red channel
0x0211	Lo					
0x0212	Hi	digital_gain_blue	16UR	01.00	RW	Gain code for blue channel
0x0213	Lo					
0x0214	Hi	digital_gain_greenb	16UR	01.00	RW	Gain code for greenb channel
0x0215	Lo					

4.3.6 Video timing registers [0x0300 to 0x03FF]

For a full description of the video timing registers please refer to *Chapter 6: Video timing on page 68*.

Table 22. Video timing registers [0x0300 to 0x03FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0300	Hi	vt_pix_clk_div	16UI	00.08	RW	Number of system clocks per pixel clock.
0x0301	Lo					
0x0302	Hi	vt_sys_clk_div	16UI	00.01	RW	System clock divider value.
0x0303	Lo					
0x0304	Hi	pre_pll_clk_div	16UI	00.01	RW	Pre PLL clock divider value.
0x0305	Lo					
0x0306	Hi	pll_multiplier	16UI	00.6A	RW	PLL multiplier value. Value: 106
0x0307	Lo					
0x0340	Hi	frame_length_lines	16UI	06.40	RW	Frame length Value: 1600 Units: Lines
0x0341	Lo					
0x0342	Hi	line_length_pck	16UI	09.C4	RW	Line length Value: 2500 Units: Pixel clocks
0x0343	Lo					
0x0344	Hi	x_addr_start	16UI	00.00	RW	X-address of the top left corner of the visible pixel data Units: Pixels
0x0345	Lo					
0x0346	Hi	y_addr_start	16UI	00.00	RW	Y-address of the top left corner of the visible pixel data(1) Units: Lines
0x0347	Lo					
0x0348	Hi	x_addr_end	16UI	08.07	RW	X-address of the bottom right corner of the visible pixel data Units: Pixels
0x0349	Lo					
0x034A	Hi	y_addr_end	16UI	06.07	RW	Y-address of the bottom right corner of the visible pixel data Units: Lines
0x034B	Lo					
0x034C	Hi	x_output_size	16UI	08.08	RW	Width of image data output from the sensor module Units: Pixels
0x034D	Lo					
0x034E	Hi	y_output_size	16UI	06.08	RW	Height of image data output from the sensor module Units: Lines
0x034F	Lo					
0x0380	Hi	x_even_inc	16UI	00.01	RW	Increment for even pixels. x_even_inc must = 1 for focus_estimation to operate effectively. Units: Pixels
0x0381	Lo					

Table 22. Video timing registers [0x0300 to 0x03FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x0382	Hi	x_odd_inc	16UI	00.01	RW	Increment for odd pixels Units: Pixels
0x0383	Lo					
0x0384	Hi	y_even_inc	16UI	00.01	RW	Increment for even pixels. y_even_inc must = 1 for focus_estimation to operate effectively. Units: Pixels
0x0385	Lo					
0x0386	Hi	y_odd_inc	16UI	00.01	RW	Increment for odd pixels Units: Pixels
0x0387	Lo					

1. Has to be modulo 4 for correct operation of device

4.3.7 Image compression registers [0x0500 to 0x05FF]

Table 23. Image compression registers [0x0500 to 0x05FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0500	Hi	compression_mode	16UI	00.01	RO	1 – DPCM/PCM compression (simple predictor)
0x0501	Lo					

4.3.8 Test pattern registers [0x0600 to 0x06FF]

See *Section 7.2: Test cursors on page 80* for more information on the digital test pattern modes.

Table 24. Test pattern registers [0x0600 to 0x06FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0600	HI	test_pattern_mode_hi	8UI	00	RW	Enables manufacturer-specific test patterns. 0 = Enable SMIA test patterns 1 = Enable manufacturer-specific test patterns
0x0601	LO	test_pattern_mode_lo	8UI	00	RW	Test pattern selector (depends on test_pattern_mode_hi content): 0 = No pattern (0), Horizontal Grayscale (1) 1 = Solid Color (0), Vertical Grayscale (1) 2 = 100% color bar (0), Diagonal Grayscale (1) 3 = Fade-to-gray color bar (0), PN28 pseudo-random sequence (1) 4 = Pseudo random PN9 (0), Video-timing Horizontal Grayscale (1) 5 = No pattern (0), Video-timing Vertical Grayscale (1) 6 = No pattern (0), Video-timing PN28 pseudo-random sequence (1)
0x0602	Hi	test_data_red	16UI	00.00	RW	The test data used to replace red pixel data. Range 0 to 1023(1).
0x0603	Lo					
0x0604	Hi	test_data_greenR	16UI	00.00	RW	The test data used to replace green pixel data on rows that also have red pixels. Valid range 0 to 1023(1).
0x0605	Lo					
0x0606	Hi	test_data_blue	16UI	00.00	RW	The test data used to replace blue pixel data. Range 0 to 1023(1).
0x0607	Lo					
0x0608	Hi	test_data_greenB	16UI	00.00	RW	The test data used to replace green pixel data on rows that also have blue pixels. Range 0 to 1023(1).
0x0609	Lo					
0x060A	Hi	horizontal_cursor_width	16UI	00.00	RW	Defines the width of the horizontal cursor (in pixels).
0x060B	Lo					
0x060C	Hi	horizontal_cursor_position	16UI	00.00	RW	Defines the top edge of the horizontal cursor.
0x060D	Lo					
0x060E	Hi	vertical_cursor_width	16UI	00.00	RW	Defines the width of the vertical cursor (in pixels).
0x060F	Lo					

Table 24. Test pattern registers [0x0600 to 0x06FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x0610	Hi	vertical_cursor_position	16UI	00.00	RW	Defines the left hand edge of the vertical cursor. A value of 0xFFFF switches the vertical cursor into automatic mode where it automatically advances every frame.
0x0611	Lo					

1. Note that some clipping of these values may occur to prevent false sync codes being generated

4.3.9 Integration time and gain parameter limit registers [0x1000 to 0x10FF]

These registers are used to define exposure limits for the integration control registers (0x200 to 0x203). See *Section 6.4: Exposure and gain control on page 75* for more information.

Table 25. Integration time and gain parameter limit registers [0x1000 to 0x10FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1000	Hi	integration_time_capability	16UI	00.01	RO	0x0001: Course and smooth (1 pixel) fine integration.
0x1001	Lo					
0x1004	Hi	course_integration_time_min	16UI	00.00	RO	Minimum course integration time. Line periods.
0x1005	Lo					
0x1006	Hi	course_integration_time_max_margin	16UI	00.03	RO	Current frame length – current max course exposure. Line periods.
0x1007	Lo					
0x1008	Hi	fine_integration_time_min	16UI	01.5E	RO	Minimum fine integration time. Pixel periods.
0x1009	Lo					
0x100A	Hi	fine_integration_time_max_margin	16UI	07.6E	RO	Current line length – current max fine exposure. Pixel periods.
0x100B	Lo					
0x1080	Hi	digital_gain_capability	16UI	00.01	RO	0x01: supports digital gain.
0x1081	Lo					
0x1084	Hi	digital_gain_min	16UR	01.00	RO	1.00000 minimum
0x1085	Lo					
0x1086	Hi	digital_gain_max	16UR	01.F8	RO	1.96875 maximum
0x1087	Lo					
0x1088	Hi	digital_gain_step_size	16UR	00.08	RO	0.03125 step size
0x1089	Lo					

4.3.10 Video timing parameter limit registers [0x1100 to 0x11FF]

For a full description of the video timing parameter limit registers please refer to *Chapter 6: Video timing on page 68*.

Table 26. Video timing parameter limit registers [0x1100 to 0x11FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1100	Hi	min_ext_clk_freq_mhz	32SF	40.C0 00.00	RO	Minimum external clock frequency Units: MHz Value: 6.0
0x1101	3rd					
0x1102	2nd					
0x1103	Lo					
0x1104	Hi	max_ext_clk_freq_mhz	32SF	41.D8 00.00	RO	Maximum external clock frequency Units: MHz Value: 27.0
0x1105	3rd					
0x1106	2nd					
0x1107	Lo					
0x1108	Hi	min_pre_pll_clk_div	16UI	00.01	RO	Minimum Pre PLL divider value Value: 1
0x1109	Lo					
0x110A	Hi	max_pre_pll_clk_div	16UI	00.04	RO	Maximum Pre PLL divider value Value: 4
0x110B	Lo					
0x110C	Hi	min_pll_ip_freq_mhz	32SF	40.C0 00.00	RO	Minimum PLL input clock frequency Units: MHz
0x110D	3rd					
0x110E	2nd					
0x110F	Lo					
0x1110	Hi	max_pll_ip_freq_mhz	32SF	41.40 00.00	RO	Maximum PLL input clock frequency Units: MHz
0x1111	3rd					
0x1112	2nd					
0x1113	Lo					
0x1114	Hi	min_pll_multiplier	16UI	00.19	RO	Minimum PLL multiplier Value: 25
0x1115	Lo					
0x1116	Hi	max_pll_multiplier	16UI	00.6A	RO	Maximum PLL multiplier Value: 106
0x1117	Lo					
0x1118	Hi	min_pll_op_freq_mhz	32SF	43.96 00.00	RO	Minimum PLL output clock frequency Units: MHz Value: 300.0
0x1119	3rd					
0x111A	2nd					
0x111B	Lo					

Table 26. Video timing parameter limit registers [0x1100 to 0x11FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x111C	Hi	max_pll_op_freq_mhz	32SF	44.20 00.00	RO	Maximum PLL output clock frequency Units: MHz Value: 640.0
0x111D	3rd					
0x111E	2nd					
0x111F	Lo					
0x1120	Hi	min_vt_sys_clk_div	16UI	00.01	RO	Minimum video-timing system clock divider value Value: 1 In data/clock mode the minimum value is 2.
0x1121	Lo					
0x1122	Hi	max_vt_sys_clk_div	16UI	00.04	RO	Maximum video-timing system clock divider value Value: 4
0x1123	Lo					
0x1124	Hi	min_vt_sys_clk_freq_mhz	32SF	43.96 00.00	RO	Minimum video-timing system clock frequency Units: MHz Value: 300.0
0x1125	3rd					
0x1126	2nd					
0x1127	Lo					
0x1128	Hi	max_vt_sys_clk_freq_mhz	32SF	44.20 00.00	RO	Maximum video-timing system clock frequency Units: MHz Value: 640.0
0x1129	3rd					
0x112A	2nd					
0x112B	Lo					
0x112C	Hi	min_vt_pix_clk_freq_mhz	32SF	42.18 00.00	RO	Minimum video-timing pixel clock frequency Units: MHz Value: 38.0
0x112D	3rd					
0x112E	2nd					
0x112F	Lo					
0x1130	Hi	max_vt_pix_clk_freq_mhz	32SF	42.A0 00.00	RO	Maximum video-timing pixel clock frequency Units: MHz Value: 80.0
0x1131	3rd					
0x1132	2nd					
0x1133	Lo					
0x1134	Hi	min_vt_pix_clk_div	16UI	00.08	RO	Minimum video-timing pixel clock divider Value: 8
0x1135	Lo					
0x1136	Hi	max_vt_pix_clk_div	16UI	00.0A	RO	Maximum video-timing pixel clock divider Value: 10
0x1137	Lo					
0x1140	Hi	min_frame_length_lines	16UI	00.A2	RO	Minimum Frame Length allowed. Units: Lines
0x1141	Lo					

Table 26. Video timing parameter limit registers [0x1100 to 0x11FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x1142	Hi	max_frame_length_lines	16UI	FF.FF	RO	Maximum possible number of lines per Frame. Value = 65535 Units: Lines
0x1143	Lo					
0x1144	Hi	min_line_length_pck	16UI	09.C4	RO	Minimum line length allowed. Value = 2500 Units: Pixel Clocks
0x1145	Lo					
0x1146	Hi	max_line_length_pck	16UI	3F.FF	RO	Maximum possible number of pixel clocks per line. Value = 16383 Units: Pixel Clocks
0x1147	Lo					
0x1148	Hi	min_line_blanking_pck	16UI	01.A8	RO	Minimum line blanking time in pixel clocks Value = 424 Units: Pixel Clocks
0x1149	Lo					
0x114A	Hi	min_frame_blanking_lines	16UI	00.20	RO	Minimum frame blanking in video lines = 32
0x114B	Lo					
0x1180	Hi	x_addr_min	16UI	00.00	RO	Minimum X-address of the addressable pixel array Value: Always 0
0x1181	Lo					
0x1182	Hi	y_addr_min	16UI	00.00	RO	Minimum Y-address of the addressable pixel array Value: Always 0
0x1183	Lo					
0x1184	Hi	x_addr_max	16UI	08.07	RO	Maximum X-address of the addressable pixel array Value = 2055
0x1185	Lo					
0x1186	Hi	y_addr_max	16UI	06.07	RO	Maximum Y-address of the addressable pixel array Value = 1543
0x1187	Lo					
0x1188	Hi	min_x_output_size	16UI	01.00	RO	Minimum x output size in pixels. Value: 256
0x1189	Lo					
0x118A	Hi	min_y_output_size	16UI	00.80	RO	Minimum y output size in pixels.
0x118B	Lo					
0x118C	Hi	max_x_output_size	16UI	08.08	RO	Maximum x output size in pixels. Value: 2056
0x118D	Lo					
0x118E	Hi	max_y_output_size	16UI	06.08	RO	Maximum y output size in pixels: Value: 1544
0x118F	Lo					
0x11C0	Hi	min_even_inc	16UI	00.01	RO	Minimum increment for even pixels used in digital subsampling
0x11C1	Lo					

Table 26. Video timing parameter limit registers [0x1100 to 0x11FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x11C2	Hi	max_even_inc	16UI	00.0F	RO	Maximum increment for even pixels used in digital subsampling
0x11C3	Lo					
0x11C4	Hi	min_odd_inc	16UI	00.01	RO	Minimum increment for odd pixels used in digital subsampling
0x11C5	Lo					
0x11C6	Hi	max_odd_inc	16UI	00.0F	RO	Maximum increment for odd pixels used in digital subsampling
0x11C7	Lo					

4.3.11 Image scaling parameter limit registers [0x1200 to 0x12FF]

Table 27. Image scaling parameter limit registers [0x1200 to 0x12FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1200	Hi	scaling_capablility	16UI	00.00	RO	0x0000: No scaling.
0x1201	Lo					
0x1204	Hi	scale_m_min	16UI	00.10	RO	Down scale factor: Minimum M value = 16
0x1205	Lo					
0x1206	Hi	scale_m_max	16UI	00.10	RO	Down scale factor: Maximum M value = 16
0x1207	Lo					
0x1208	Hi	scale_n_min	16UI	00.10	RO	Down scale factor: Minimum N value = 16
0x1209	Lo					
0x120A	Hi	scale_n_max	16UI	00.10	RO	Down scale factor: Maximum N value = 16
0x120B	Lo					

4.3.12 Image compression parameter registers [0x1300 to 0x13FF]

Table 28. Image compression parameter limit registers [0x1300 to 0x13FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1300	Hi	compression_capablility	16UI	00.01	RO	0x0001: DPCM/PCM compression
0x1301	Lo					

4.3.13 Color matrix registers [0x1400 to 0x14FF]

For more information on these matrix parameters see *Chapter 8: Color matrix on page 82*.

Table 29. Color matrix registers [0x1400 to 0x14FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1400	Hi	matrix_element_RedInRed	16SR	01.00	RO	Color matrix parameter for Red in Red
0x1401	Lo					
0x1402	Hi	matrix_element_GreenInRed	16SR	00.00	RO	Color matrix parameter for Green in Red
0x1403	Lo					
0x1404	Hi	matrix_element_BlueInRed	16SR	00.00	RO	Color matrix parameter for Blue in Red
0x1405	Lo					
0x1406	Hi	matrix_element_RedInGreen	16SR	00.00	RO	Color matrix parameter for Red in Green
0x1407	Lo					
0x1408	Hi	matrix_element_GreenInGreen	16SR	01.00	RO	Color matrix parameter for Green in Green
0x1409	Lo					
0x140A	Hi	matrix_element_BlueInGreen	16SR	00.00	RO	Color matrix parameter for Blue in Green
0x140B	Lo					
0x140C	Hi	matrix_element_RedInBlue	16SR	00.00	RO	Color matrix parameter for Red in Blue
0x140D	Lo					
0x140E	Hi	matrix_element_GreenInBlue	16SR	00.00	RO	Color matrix parameter for Green in Blue
0x140F	Lo					
0x1410	Hi	matrix_element_BlueInBlue	16SR	01.00	RO	Color matrix parameter for Blue in Blue
0x1411	Lo					

4.3.14 Manufacturer specific registers [0x3000 to 0x3FFF]

Table 30. Manufacturer specific registers [0x3000 to 0x3FFF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x3000	Hi	dark_average	16UI	00.00	RO	Average value of dark lines
0x3001	Lo					
0x3002		dark_flags	8B	00	RO	Bit_0 = 1 if dark value is stable Bit_1 = 1 if dark value exceeds 512
0x3003		dark_setup	8B	01	RW	Bit_0 = 0 : Do not apply any offset. 1 : Apply an offset. Offset used is determined by bits_2:1 Bits_2:1 = 0: Internally calculated 1: From registers [0x3004 to 0x3005] 2: The sum of internal and manual values 3: Internally calculated without leaky integration.
0x3004	Hi	dark_offset	16SI	00.00	RW	Fixed, signed offset that can be applied to the digitized pixel values in the output coding block. The offset is subtracted from the pixel data. The value can be as large as the maximum pixel data range.
0x3005	Lo					
0x3006	Hi	dark_pedestral	16UI	00.04	RW	Programmable pedestal value used by the dark calibration.
0x3007	Lo					
0x31F0		bruce_enable	8UI	00	RW	0 - Disable couplet correction (Bruce Off) 1 - Enable couplet correction (Bruce On)
0x3300		bayer_average_enable	8UI	0	RW	0 - Bayer averager off 1 - Bayer averager on
0x3328		EDOF_Enable	8UI	00	RW	0 - Disable EDOF 1 - Enable EDOF
0x322A		EDOF_HW_Enable	8UI	00	RO	EDOF associated HW (borders/crop) enable request and status: Bit_0 = 1 if request enable EDOF HW Bit_1 = 1 if status enable EDOF HW
0x3330		EDOF_Status	8UI	11	RW	Status of Defcore on EDOF disable: Bit_0 = 1 if Defcore enable Status of noise reduction on EDOF disable: Bit_1 = 1 if noise reduction enable.

Table 30. Manufacturer specific registers [0x3000 to 0x3FFF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x3331		EDOF_Mode	8UI	00	RW	Selects DCF table to apply or auto mode to automatically select general purpose and low light DCFs 0 = Auto* 1 = General Purpose 2 = Macro 3 = Barcode 4 = Low Light 2 (extreme conditions) 5 = Low Light 1 (mid conditions)
0x3332		SLP_Selected	8UI	01	RW	Report selected SLP configuration 1 = General Purpose 2 = Macro 3 = Barcode 4 = Low Light 2 5 = Low Light 1
0x3333		Active_management_state	8UI	00	RW	Reflects the current state of EDOF active management state machine 0 = EDOF_Disable 1 = EDOF_waiting_for_enable 2 = EDOF_waiting_for_disable 3 = EDOF_manual 4 = EDOF_auto_current 5 = EDOF_auto_request_new
0x3334		Active_management_ hysteresis_count	8UI	00	RW	Count of number of consecutive frames where the same optimum DCF has been found.
0x3335		Active_management_ hysteresis_ctrl	8UI	03	RW	Number of consecutive frames required where the same optimum DCF has been found to trigger a change of selected DCF.
0x3336		Active_management_DCF_ pending	8UI	00	RW	Optimum DCF as calculated by active management firmware which may trigger a new DCF to be selected depending on hysteresis control.
0x3337		Active_management_ processing_result	8UI	00	RW	Reflects the most recently calculated optimum DCF.
0x3338		Low_light_ctrl_mechanism	8UI	01	RW	Determines control mechanism for low-light estimation: 0 = Host provides low-light estimation 1 = Gain control

Table 30. Manufacturer specific registers [0x3000 to 0x3FFF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x3339		Host_low_light_estimate	8UI	01	RW	Binary flag from host to tell firmware is the scene is low-light or normal light (low-light SLP selected depending on value in EDOF_Spare_3) 0 = Low light 1 = Normal light
0x333f		EDOF_Spare_3	8UI	00	RW	Control of low-light SLP selection. When low-light switching is controlled by gain mechanism and Low Light 1 is selected, then Low Light 1 is selected above low gain threshold and Low Light 2 is selected above high gain threshold 4 = Low Light 2 5 = Low Light 1
0x3340	Hi	Low_Light_Gain_Threshold	16UI	08.00	RW	Low gain switching threshold 8.8UR
0x3341	Lo					
0x3350		DMA_En	8UI	01	RW	Enable the DCF DMA controller 0 = DMA OFF 1 = DMA enabled
0x3351		DMA_Auto	8UI	01	RW	Enable the DCF DMA controller auto mode 0 = DMA initiated by write to dma_sel_req 1 = DMA initiated by hardware.
0x3352		DMA_Sel_Req	8UI	01	RW	Requested DCF table 1 = DCF table 1 = Normal/General Purpose (pwr up) 2 = DCF table 2 = Macro 3 = DCF table 3 = Barcode 4 = DCF table 4 = Transition (N/A)
0x3353		DMA_Sel_Status	8UI	00	RO	Current DCF table loaded 0 = no DCF selected (pwr up status) 1 = DCF table 1 = Normal/General Purpose 2 = DCF table 2 = Macro 3 = DCF table 3 = Barcode 4 = DCF table 4 = Transition (N/A)
0x3354		DMA_Start	8UI	00	RW	Kick off transfer manually when DMA_Auto is low 0 = disabled 1 = update DCF tables instantly (when auto disabled)

Table 30. Manufacturer specific registers [0x3000 to 0x3FFF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x3355		DMA_Status	8UI	00	RO	DMA status 0 = DMA inactive 1 = DMA active
0x3874		av_filter_disable	8UI	00	RW	Disable the Anti-vignette (lens shading correction) filter
0x399E	Hi	Gain_Gr	16UI	01.00	RW	Host provided channel gain (Gr)
0x399F	Lo					
0x39A0	Hi	Gain_R	16UI	01.00	RW	Host provided channel gain (R)
0x39A1	Lo					
0x39A2	Hi	Gain_B	16UI	01.00	RW	Host provided channel gain (B)
0x39A3	Lo					
0x39A4	Hi	Gain_Gb	16UI	01.00	RW	Host provided channel gain (Gb)
0x39A5	Lo					

Table 31. Parallel interface control registers [0x3380 to 0x3393]

Index	Byte	Register name	Data type	Default	Type	Comment
0x3380		Sync_Clk_Setup	8UI	03	R/W	Bit 0: Enable active low hsync Bit 1: Enable active low vsync Bit 2: Enable clks during interline Bit 3: Enable continuous clk during interframe
0x3381		Enable	8UI	00	R/W	Enable Parallel Coder Logic
0x3383		Automatic_Mode_En	8UI	01	R/W	VSYNC and HSYNC envelopes 0 - Manual 1 - Automatic
0x3384	Hi	Hsync_Start	16UI	00.03	R/W	Start position for HSYNC in PCLKs
0x3385	Lo					
0x3386	Hi	Hsync_Stop	16UI	08.0B	R/W	Stop position for HSYNC in PCLKs
0x3387	Lo					
0x3388	Hi	Vsync_Coarse_Start	16UI	00.02	R/W	Start position for VSYNC in lines
0x3389	Lo					
0x338A	Hi	Vsync_Coarse_Stop	16UI	06.09	R/W	Stop position for VSYNC in lines
0x338B	Lo					
0x338C	Hi	Vsync_Fine_Start	16UI	00.03	R/W	Start position for VSYNC in PCLKs
0x338D	Lo					

Table 31. Parallel interface control registers [0x3380 to 0x3393] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x338E	Hi	Vsync_Fine_Stop	16UI	08.0B	R/W	Stop position for VSYNC in PCLKs
0x338F	Lo					
0x3390	Hi	Blanking_Data	16UI	00.1C	R/W	Programmable line/frame blanking value
0x3391	Lo					
0x3395		Auto_Startup	8UI	00	R/W	Select output interface when streaming requested 0 = auto CCP2 startup 1 = auto Parallel startup

4.3.15 NVM programming

The VD6803 has 1 Kbits of non-volatile storage (NVRAM) organized as 32 x 32 bits. The NVM is used to store system parameters during manufacture. The NVM provides a specific location named “Part Numbering”: the module maker can use the corresponding 2 bytes to identify its product. The “Part Numbering” area is located at the following address: NVM address “0” (NVM Byte “0”) and NVM address “1” (NVM Byte “3”). Contact STMicroelectronics for ID assignment.

A logic “0” corresponds to a virgin antifuse; a logic “1” corresponds to a blown antifuse. A logic “1” on any bit cell is permanent and cannot be erased.

In order to program the NVM, VANA must be elevated to 3.7 V and 7.9 V applied to the HV pin. The HV pin should be left floating when programming is complete. To ensure NVM reliability, a high voltage should not be applied to the HV pin for longer that a cumulative total of five minutes over the product lifetime.

Table 32 describes the I²C registers used to access the NVM.

Table 32. NVM registers

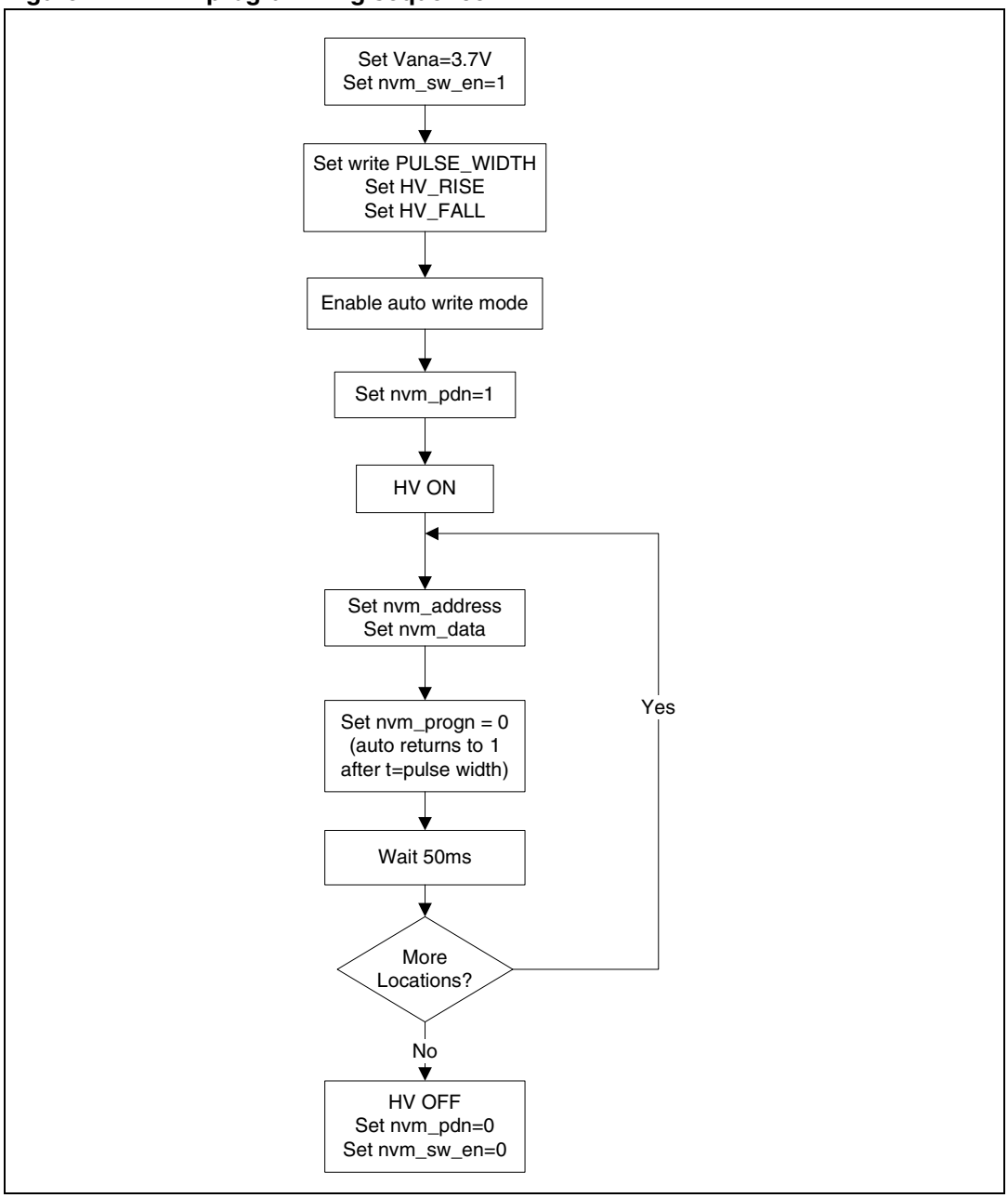
Addr	Register name	Type	SIgnal name	Bit	Func	Def	Comment
3400	T1_PAGE	8UI	nvm_page	7:0	R	00	T1 address decode
3480	CTRL	8UI	nvm_wr_en	0	PRW	00	Enable write mode 0x0 = Disabled 0x1 = Enabled
			nvm_pulse_en	1	PRW	01	Enable pulse mode 0x0 = Manual PROGN control 0x1 = Auto PROGN pulse control
3481	PDN	8UI	nvm_pdn	0	PRW	00	NVM power down. Active Low
3482	PROGN	8UI	nvm_prog	0	PRWC	01	Auto pulse control to program NVM
			nvm_progn_man	1	PRW	01	Manual pulse control to program NVM
			nvm_progn	4	PR	01	progn status

Table 32. NVM registers (continued)

Addr	Register name	Type	SIgnal name	Bit	Func	Def	Comment
3483	READN	8UI	nvm_read	0	PRWC	01	Auto pulse control to read NVM
			nvm_readn_man	1	PRW	01	Manual pulse control to read NVM
			nvm_readn	4	PR	01	readn status
3485	TESTREAD	8UI	nvm_testread	0	PRW	00	
			nvm_hvon	1	PRW	00	
3486	ADDR	8UI	nvm_addr_reg	4:0	PRW	00	Manual NVM address
3488	DATAIN_3	32UI	nvm_datain	31:0	PRW	00	Data to NVM
3489	DATAIN_2					00	
348A	DATAIN_1					00	
348A	DATAIN_0					00	
348C	PULSE_WIDTH_HI	16UI	nvm_pulse_width	15:0	PRW	00	Pulse width, defaults to read width
348D	PULSE_WIDTH_LO					0c	
3490	DATAOUT_3	32UI	nvm_dataout	31:0	PR	00	Data from NVM
3491	DATAOUT_2					00	
3492	DATAOUT_1					00	
3493	DATAOUT_0					00	
3494	HV_RISE_HI	16UI	nvm_hv_rise	15:0	PRW	00	Point at which HV rises
3495	HV_RISE_LO					be	
3496	HV_FALL_HI	16UI	nvm_hv_fall	15:0	PRW	1e	Point at which HV falls
3497	HV_FALL_LO					29	
3498	DATAIN_ECC	8UI	nvm_datain_ecc	5:0	PRW	00	Data to NVM - EEC 6-bit width extension
3499	DATAOUT_ECC	8UI	nvm_dataout_ecc	5:0	PR	00	Data from NVM - EEC 6-bit width extension

Figure 21 represents the flowchart of the NVM programming operation.

Figure 21. NVM programming sequence



An example of code to program the first four addresses of NVM is shown below.

```
// Example script to program NVM for VD6803
// ExtClock=12MHz. Pulse_Width=reg_value*16/extclk (for write
cycle)
// Pulse_Width=reg_value/extclk (for read cycle)

$USB2CCISCRIPT
SetBank( 0x10 );

WriteByte( 0x3508, 0x04 ); // PRIVATE_POWER_CTRL (nvm_sw_en)
WriteByte( 0x348C, 0x75 ); // MAN_SPEC_NVM_PULSE_WIDTH_HI (40ms)
WriteByte( 0x348D, 0x7b ); // MAN_SPEC_NVM_PULSE_WIDTH_LO
WriteByte( 0x3494, 0x00 ); // MAN_SPEC_NVM_HV_RISE_HI
WriteByte( 0x3495, 0x25 ); // MAN_SPEC_NVM_HV_RISE_LO
WriteByte( 0x3496, 0x75 ); // MAN_SPEC_NVM_HV_FALL_HI
WriteByte( 0x3497, 0x55 ); // MAN_SPEC_NVM_HV_FALL_LO
WriteByte( 0x3480, 0x03 ); // MAN_SPEC_NVM_CTRL
WriteByte( 0x3481, 0x01 ); // MAN_SPEC_NVM_PDN

//-------------------------------------------------------------
//Program address 0
//-------------------------------------------------------------
WriteByte( 0x3486, 0x00 ); // MAN_SPEC_NVM_ADDR
WriteByte( 0x3488, 0x01 ); // MAN_SPEC_NVM_DATAIN_3
WriteByte( 0x3489, 0x00 ); // MAN_SPEC_NVM_DATAIN_2
WriteByte( 0x348A, 0x00 ); // MAN_SPEC_NVM_DATAIN_1
WriteByte( 0x348B, 0x00 ); // MAN_SPEC_NVM_DATAIN_0
WriteByte( 0x3482, 0x00 ); // MAN_SPEC_NVM_PROGN
Wait(50); // wait while NVM programmed

//-------------------------------------------------------------
//Program address 1
//-------------------------------------------------------------
WriteByte( 0x3486, 0x01 ); // MAN_SPEC_NVM_ADDR
WriteByte( 0x3488, 0x00 ); // MAN_SPEC_NVM_DATAIN_3
WriteByte( 0x3489, 0x01 ); // MAN_SPEC_NVM_DATAIN_2
WriteByte( 0x348A, 0x00 ); // MAN_SPEC_NVM_DATAIN_1
WriteByte( 0x348B, 0x00 ); // MAN_SPEC_NVM_DATAIN_0
WriteByte( 0x3482, 0x00 ); // MAN_SPEC_NVM_PROGN
Wait(50); // wait while NVM programmed

//-------------------------------------------------------------
//Program address 2
//-------------------------------------------------------------
WriteByte( 0x3486, 0x02 ); // MAN_SPEC_NVM_ADDR
WriteByte( 0x3488, 0x00 ); // MAN_SPEC_NVM_DATAIN_3
WriteByte( 0x3489, 0x00 ); // MAN_SPEC_NVM_DATAIN_2
WriteByte( 0x348A, 0x01 ); // MAN_SPEC_NVM_DATAIN_1
WriteByte( 0x348B, 0x00 ); // MAN_SPEC_NVM_DATAIN_0
WriteByte( 0x3482, 0x00 ); // MAN_SPEC_NVM_PROGN
Wait(50); // wait while NVM programmed
```

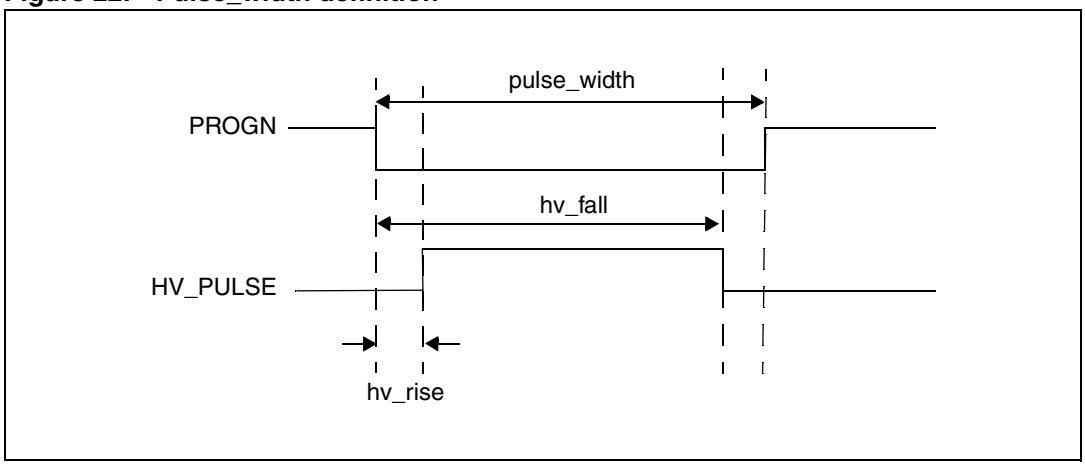
```
//-------------------------------------------------------------
//Program address 3
//-------------------------------------------------------------
WriteByte( 0x3486, 0x03 ); // MAN_SPEC_NVM_ADDR
WriteByte( 0x3488, 0x00 ); // MAN_SPEC_NVM_DATAIN_3
WriteByte( 0x3489, 0x00 ); // MAN_SPEC_NVM_DATAIN_2
WriteByte( 0x348A, 0x00 ); // MAN_SPEC_NVM_DATAIN_1
WriteByte( 0x348B, 0x01 ); // MAN_SPEC_NVM_DATAIN_0
WriteByte( 0x3482, 0x00 ); // MAN_SPEC_NVM_PROGN
Wait(50); // wait while NVM programmed

//-------------------------------------------------------------
//Post Programming
//-------------------------------------------------------------
WriteByte( 0x3481, 0x00 ); // nvm_pdn=0, circuit pwr dwn
WriteByte( 0x3508, 0x00 ); // nv_sw_en disabled
```

Pulse_width definition

NVM data/address are latched on the falling edge of progn. Typically a hv_pulse width of 20 ms to 40 ms is suitable for programming. For a write cycle, the register values for pulse_width, hv_rise and hv_fall are calculated as follow:

$$\text{reg\_value} = (\text{duration in ms}) \times \text{extclk} / 16$$

Figure 22. Pulse_width definition



Reading the NVM

The NVM is read with the usual 2.8 V VANA supply. The HV pin is not required. The NVM register values can be read from the T1_page registers 0x3400 to 0x347F. The NVM can only be accessed after setting nvm_sw_en = 4 [0x3508] and powering up the NVM,

nvm_pdn = 1[0x3481].

The read pulse width is also determined by the PULSE_WIDTH register. For a read cycle, this is calculated as:

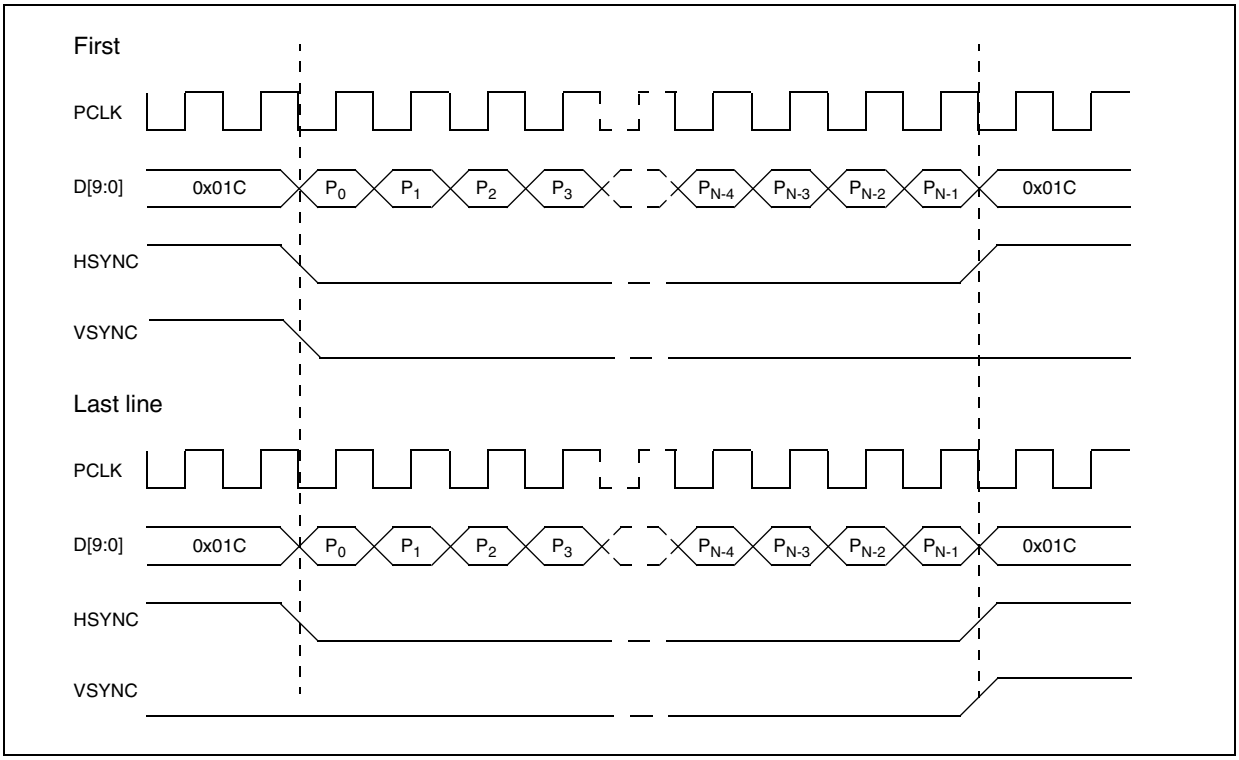
$$\text{reg\_value} = (\text{duration in ms}) \times \text{extclk}$$

Typically, a read pulse width of 1 to 2 µs is sufficient.

5 Parallel 10-bit port

PCLK, HSYNC and VSYNC output polarities are programmable; the description and the figures in this section assume the default (reset) positions and polarity. The host uses the rising edge of PCLK to sample both the data and the synchronization lines. Upon reset, the parallel data interface is disabled, that is, all outputs are high impedance.

Figure 23. 10-bit parallel data interface signals



5.1 Frame format

In addition to visible pixel image data, the VD6803 also outputs two lines of device configuration information (embedded data).

Figure 24. Parallel interface only visible data qualified

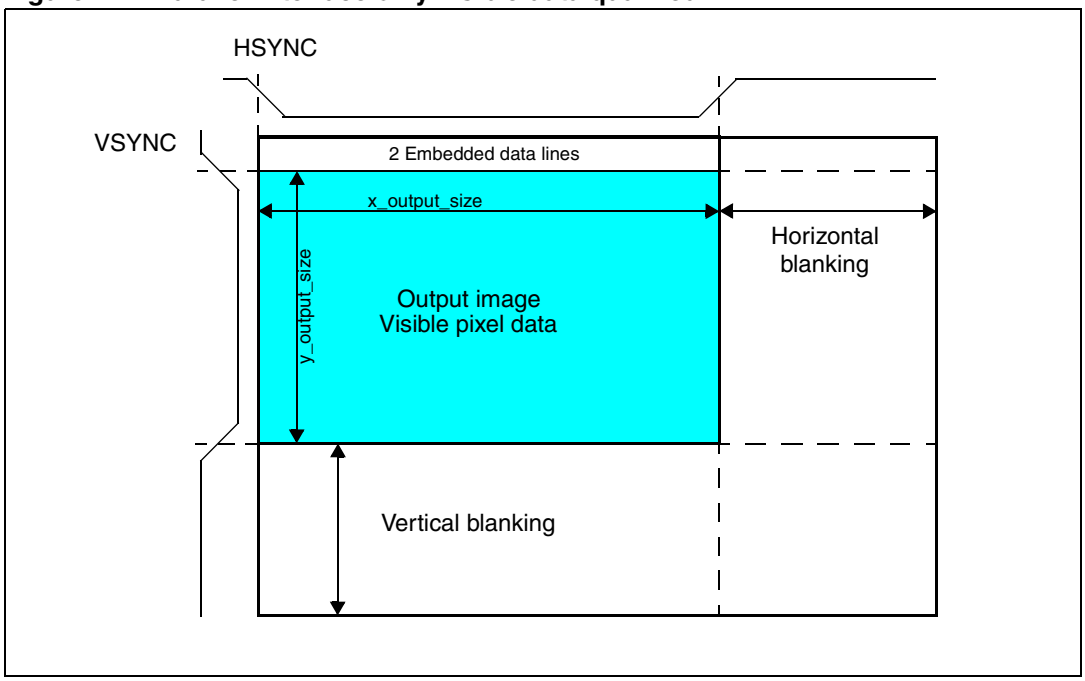
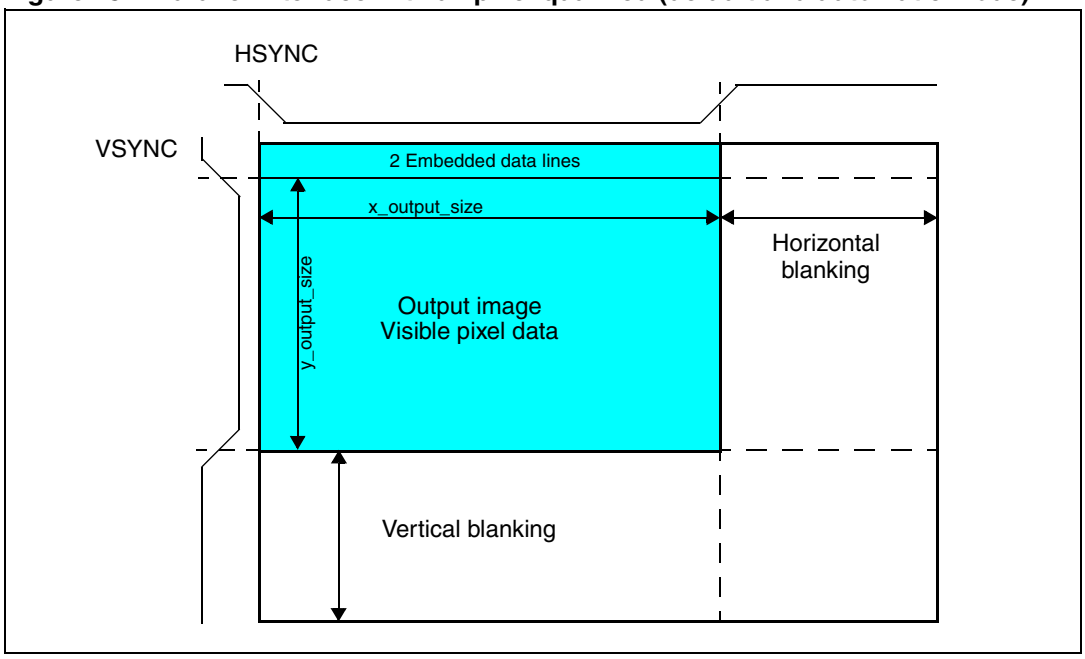


Figure 25. Parallel interface with all pixel qualified (default and automatic mode)



There are two synchronization modes:

- automatic
- manual

In automatic mode, the VSYNC and HSYNC envelopes automatically track any variation in output size.

In the manual mode, VSYNC and HSYNC envelopes are fully programmable. By default, the VSYNC and HSYNC envelopes all of the output pixel data including the embedded data and the visible image data.

Embedded data lines

The embedded data lines provide a mechanism to embed non-image data such as sensor configuration details and image statistics values with a frame. The minimum requirement is to have one embedded data line at the start of the frame. If the number of I^2C registers to be output is greater than the output line length allows, then more embedded data lines can be added at the start of the frame. The number of embedded data lines at the start and end of the frame is specified as part of the frame format description. VD6803 has two embedded data lines.

Visible pixel data

The visible pixels contain valid image data.The correct integration time and analogue gain for the visible pixels is specified in the embedded data lines at the start of the frame. The number of visible pixels can be varied.

Horizontal and vertical blanking

During line blanking, all bytes in the data stream are set to a specific value defined in the parallel interface control registers.

5.2 Automatic HSYNC and VSYNC mode

In the automatic mode, the HSYNC and VSYNC envelopes automatically track any changes in the output image size programmed (x_output_size and y_output_size). In this mode, the envelopes qualify all pixel data output including the embedded data and the visible pixel data. In this mode, the fine position of the start of VSYNC automatically tracks with the start of HSYNC position. In this mode, the fine position of the end of VSYNC automatically tracks with the end of HSYNC position.

5.3 Pixel clock (PCLK)

The PCLK output is a continuous clock with the same frequency as the internal video timing pixel clock. If a different HSYNC envelope is programmed, then the positions of where PCLK is gated does not change. The HSYNC envelope is independent of the gating of PCLK.

5.4 Manual HSYNC

The start and end positions of the HSYNC envelope are programmable in output pixels (PCLKs). The start and end positions are programmable relative to zero point which is a

fixed number of PCLKs (three pixels) prior to first pixel value output. As the width of the output size changes (x_output_size), the end position of the HSYNC envelope must be re-programmed. In the manual sync mode, the op_coder_hsync_start and op_coder_hsync_stop values do not automatically track changes in the x_output_size value.

If the required HSYNC envelope is the same as a visible pixel only data, then the rules are:

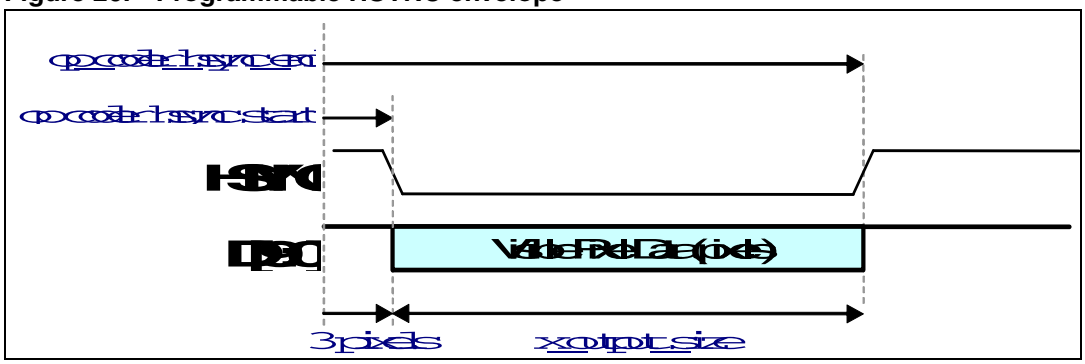
- op_coder_hsync_start = 3 pixels
- op_coder_hsync_stop = 3 + x_output_size

where:

256 pixels <= x_output_size<=2064 pixels

HSYNC is output on all lines including the lines during the frame blanking period.

Figure 26. Programmable HSYNC envelope



5.5 Manual VSYNC

The start and end positions of the VSYNC envelope are programmable at two levels.

- Coarse: The line within a frame VSYNC start and stops.
- Fine: The pixel within a line which VSYNC start and stops.

The coarse (line) start and end positions are programmable relative to the start of the first embedded data line. The fine (pixel) start and end positions are programmable relative to a zero point which is a fixed number of PCLKs (three pixels) prior to first pixel value output.

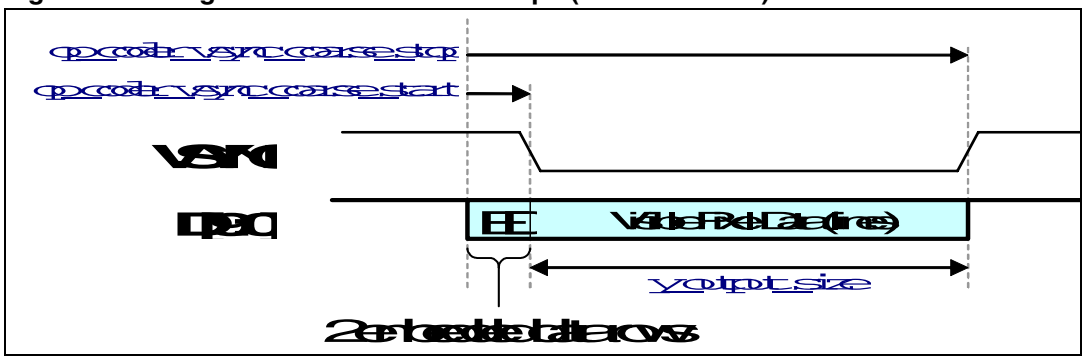
As the width of the output size changes (y_output_size) the end position of the VSYNC envelope must be re-programmed. In manual sync mode, the op_coder_vsync_coarse_start, op_coder_vsync_coarse_stop, op_coder_vsync_fine_start and op_coder_vsync_fine_stop values do not automatically track changes in the y_output_size value.

If the required VSYNC envelope is the same as a visible pixel data then the rules are:

- **Coarse control (line level)**:
  - op_coder_vsync_coarse_start = 2 lines
  - op_coder_vsync_coarse_stop = 2 + y_ output_size-1

  where:
  - 192 <= op_coder_vsync_coarse_stop < (y_output_size + 2)

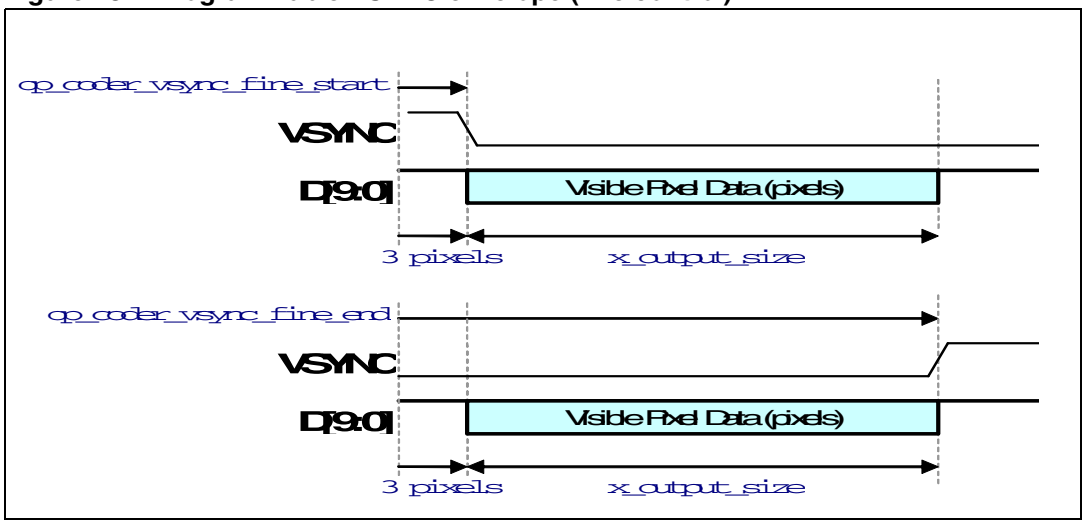
Figure 27. Programmable VSYNC envelope (coarse control)



- **Fine control (pixel level)**:
  - op_coder_vsync_fine_start = 3 pixels
  - op_coder_vsync_fine_end = 3 + x_ output_size

  where:
  - 256 pixels < x_output_size <= 2064 pixels

Figure 28. Programmable VSYNC envelope (fine control)



6 Video timing

6.1 Output size

The VD6803 has the following methods available to achieve the required output size, these can be used independently or in conjunction with any other:

- programmable addressable region of the pixel array, see *Section 6.1.1*
- programmable width and height for output image data, *Section 6.1.2 on page 69*
- subsampling, see *Section 6.1.3 on page 69*
- analog binning, see *Section 6.1.4 on page 71*

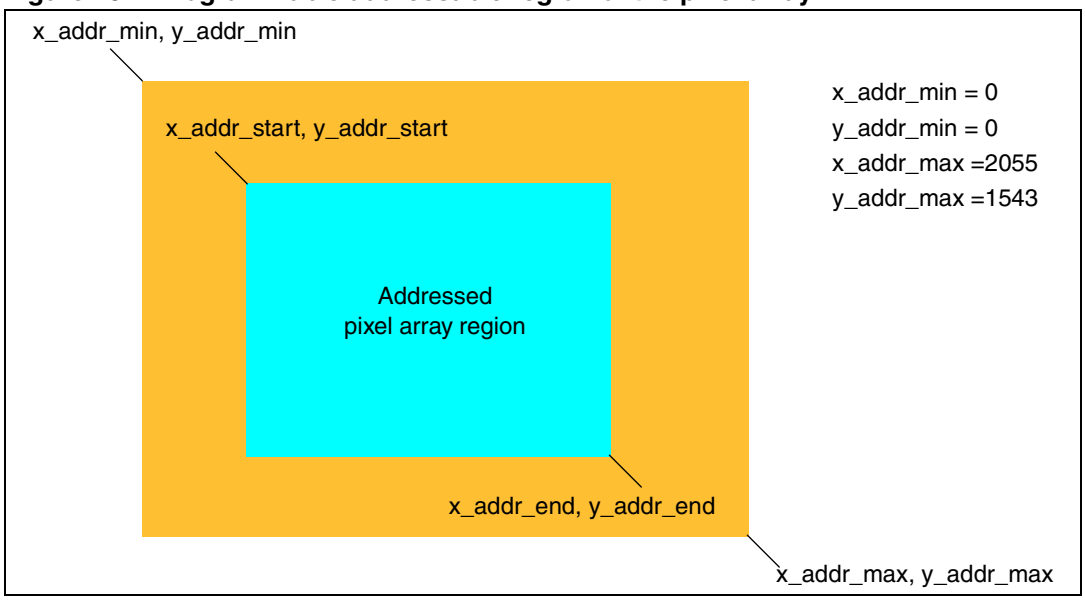
The programmable image size and output size are independent functions. It is the responsibility of the host to ensure that these functions are programmed correctly for the intended application. These functions also reduce the amount of data and therefore reduce the data rate of the parallel port.

6.1.1 Programmable addressable region of the pixel array

The native size for the VD6803 is 2048 x 1536, the maximum addressable array is 2056 x 1544 which gives border (outer four rows and four columns) pixels for the color reconstruction algorithms to use at the edges of the array.

By programming the x_addr_start, y_addr_start, x_addr_end and y_addr_end registers it is possible to use the full size of the array as you would do for a native size output or you can select a “window of interest”. The addressed region of the array is used in any subsequent sub-sampling.

Figure 29. Programmable addressable region of the pixel array



The host must ensure the following rules are kept;

- the end address must be greater than the start address
- the x and y start addresses are restricted to even numbers only, and the x and y end addresses are restricted to odd numbers only, to ensure that there is always a even number of pixels readout

6.1.2 Programmable width and height for output image data

The x_output_size and y_output_size registers are not intended as the primary cropping controls.

They are intended to define the length of the data to transmit so that the sensor does not need to calculate this based on region of interest and sub-sampling settings. It should be expected that the host will set the output sizes to exactly enclose the output image data. If the host should not do this, the VD6803 will treat the output sizes as being calculated from the top left hand corner of the output array. So in the case where output sizes are smaller than the output data, the data shall be cropped from its right hand and lower limits. In the case where larger than the output data, the lines shall be padded out to the defined output size with undefined data.

Note: The active line length must be a multiple of two.

6.1.3 Subsampling

Subsampling is achieved by programming the x _odd_inc, y_odd_inc, x_even_inc and y_even_inc registers.

If the pixel being readout has an even address then the address is incremented by the even increment value either x_even_inc or y_even_inc. If the pixel being readout has an odd address then the address is incremented by the odd increment value either x _odd_inc or y_odd_inc.

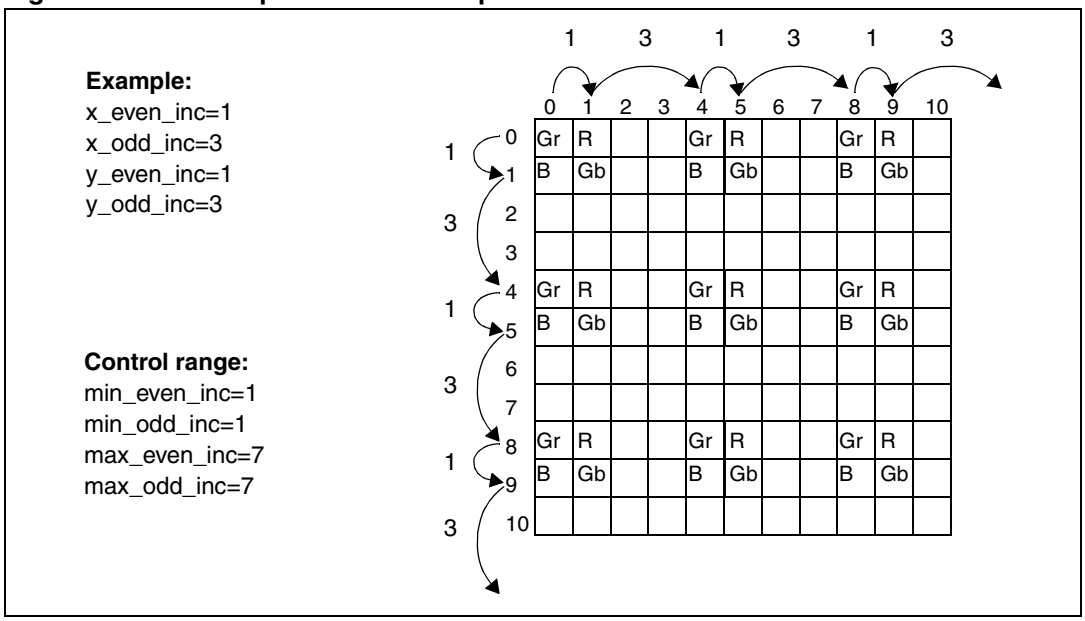
The subsampled readout is disabled by setting the odd and even increment values to 1.

Subsampling acts upon the addressed region of the array which is determined by the x_addr_start, y_addr_start, x_addr_end and y_addr_end registers.

The equation for the subsampling factor is given below:

$$\text{sub\_sampling\_factor} = \frac{\text{even\_inc} + \text{odd\_inc}}{2}$$

Figure 30. Subsample readout example



Subsampled example: VGA from the VD6803 sensor

Required output width = 640 pixels

- readout on parallel port requires the `output width` to be a multiple of 2
- `x_output_size` can remain at 640

Target scale factor = 2048/640 = 3.2

Target scale factor is round down to nearest even number = 3

x_even_inc = 1

x_odd_inc = 5

y_even_inc = 1

y_odd_inc = 5

Therefore using an addressed region of the array to crop,

addr_array_x_size = 640*3 = 1920

addr_array_y_size = 480*3 = 1440

For this to be centered on the array,

x_addr_start = 68

y_addr_start = 52

x_addr_end = 1987

y_addr_end = 1491

Beware that the two color pixels of each row/column must be equally distributed (even: Green, odd: Red/Blue). This is achieved by keeping the sum (even_inc + odd_inc) even in each dimension.

6.1.4 Analog pixel binning

The VD6803 also has an analog binning mode, sometimes also referred to as analogue Bayer scaling, that offers a reduced size full field of view image. The pixel binning mode averages row and column pixel data.

The analog binning mode results in a reduced number of lines and so can be used to give a higher image frame rate. Compared to sub-sampling, analog-binning makes use of the light gathered from the whole pixel array and it results in higher image quality.

The selection of the pixel binning mode is controlled using register MAN_SPEC_BAYER_AVERAGE (0x3300):

0: No analog pixel binning (default)

1: Pixel binning mode

The analog pixel binning mode will scale by x2 in the X-direction and x2 in the Y-direction.

Entering and exiting analog binning mode must be performed when the sensor is in software standby.

Contact STMicroelectronics for the timing for analog pixel binning.

6.2 Video timing

This section specifies the timing for the image data that is readout from the pixel array and the output image data, as we have seen these are not necessarily the same size.

The application of all of the video timing read/write parameters must be re-timed to the start of frame boundary to ensure that the parameters are consistent within a frame.

The video stream which is output from the VD6803 contains both video data and other auxiliary information.

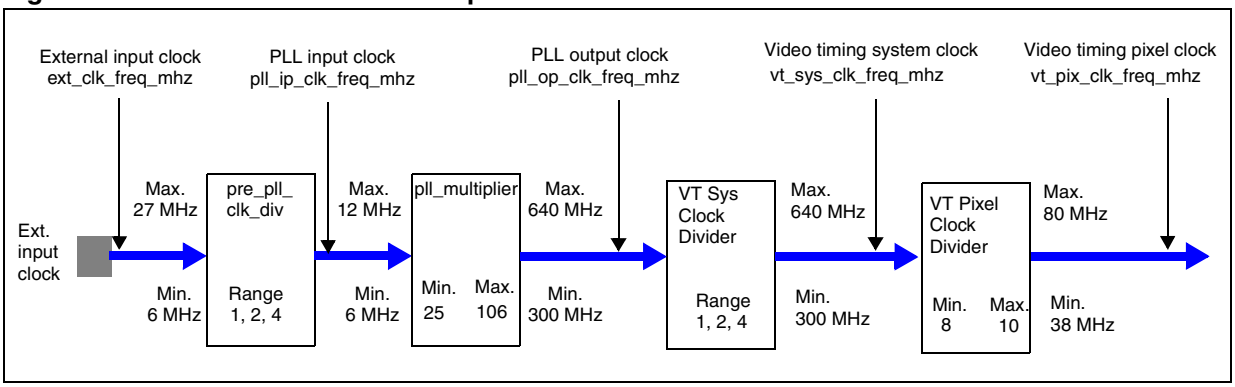
6.2.1 PLL block

The VD6803 contains a PLL (Phase Locked Loop) block, which generates all the necessary internal clocks from the external clock input. Changes to the PLL settings on the VD6803 will only be consumed on the software standby to streaming mode transition.

Figure 31 shows the internal functional blocks, which define the relationship between the external input clock frequency and the pixel clock frequency.

The majority of the logic within the device is clocked by vt_sys_clk however the I^2C block is clocked by the external input clock.

Figure 31. VD6803 clock relationships



The equation relating the input clock frequency to pixel clock frequencies are given below.

$$vt\_pix\_clk\_freq\_mhz = \frac{ext\_clk\_freq\_mhz \times pll\_multiplier}{pre\_pll\_clk\_div \times vt\_sys\_clk\_div \times vt\_pix\_clk\_div}$$

6.2.2 Framerate

The framerate of the array readout and therefore the output framerate is governed by the line length, frame length and the video timing pixel clock frequency.

- Line length is specified as a number of pixel clocks, line_length_pck.
- Frame length is specified as a number of lines, frame_length_lines.
- Video timing pixel clock is specified in MHz, vt_pix_clk_freq_mhz.

The equation relating the framerate to the Line length, frame length and the video timing pixel clock frequency is given below.

$$Framerate = \frac{vt\_pix\_clk\_freq\_mhz}{line\_length\_pck \times frame\_length\_lines}$$

Table 33 provides examples of frame timing for data/strobe mode for 20fps for a variety of external clock frequencies.

Table 33. External clock frequency examples - 3.15MP 10 bits // 20fps

Ext clk freq	Pre-PLL clk div	PLL multiplier	VT sys clk div	VT pixel clk div	Video timing pixel clk	Line length		Frame length
MHz	Integer	Integer (Dec)	Integer	Integer	MHz	Pixel clks	µs	Lines (Dec)
6.00	1	106	1	8	79.500	2500	31.45	1590
6.50	1	98	1	8	79.625	2500	31.40	1593
8.00	1	80	1	8	80.000	2500	31.25	1600
8.40	1	76	1	8	79.800	2500	31.33	1596
9.00	1	71	1	8	79.875	2500	31.30	1598
9.60	1	66	1	8	79.200	2500	31.57	1584
9.72	1	65	1	8	78.975	2500	31.66	1580

Table 33. External clock frequency examples - 3.15MP 10 bits // 20fps (continued)

Ext clk freq	Pre-PLL clk div	PLL multiplier	VT sys clk div	VT pixel clk div	Video timing pixel clk	Line length		Frame length
MHz	Integer	Integer (Dec)	Integer	Integer	MHz	Pixel clks	µs	Lines (Dec)
12.00	2	106	1	8	79.500	2500	31.45	1590
13.00	2	98	1	8	79.625	2500	31.40	1593
13.50	2	94	1	8	79.313	2500	31.52	1587
16.00	2	80	1	8	79.800	2500	31.25	1600
16.80	2	76	1	8	79.875	2500	31.33	1596
19.20	2	66	1	8	79.200	2500	31.57	1584
19.44	2	65	1	8	78.975	2500	31.66	1580
24.00	4	106	1	8	79.500	2500	31.45	1590
26.00	4	98	1	8	79.625	2500	31.40	1593
27.00	4	94	1	8	79.313	2500	31.52	1587

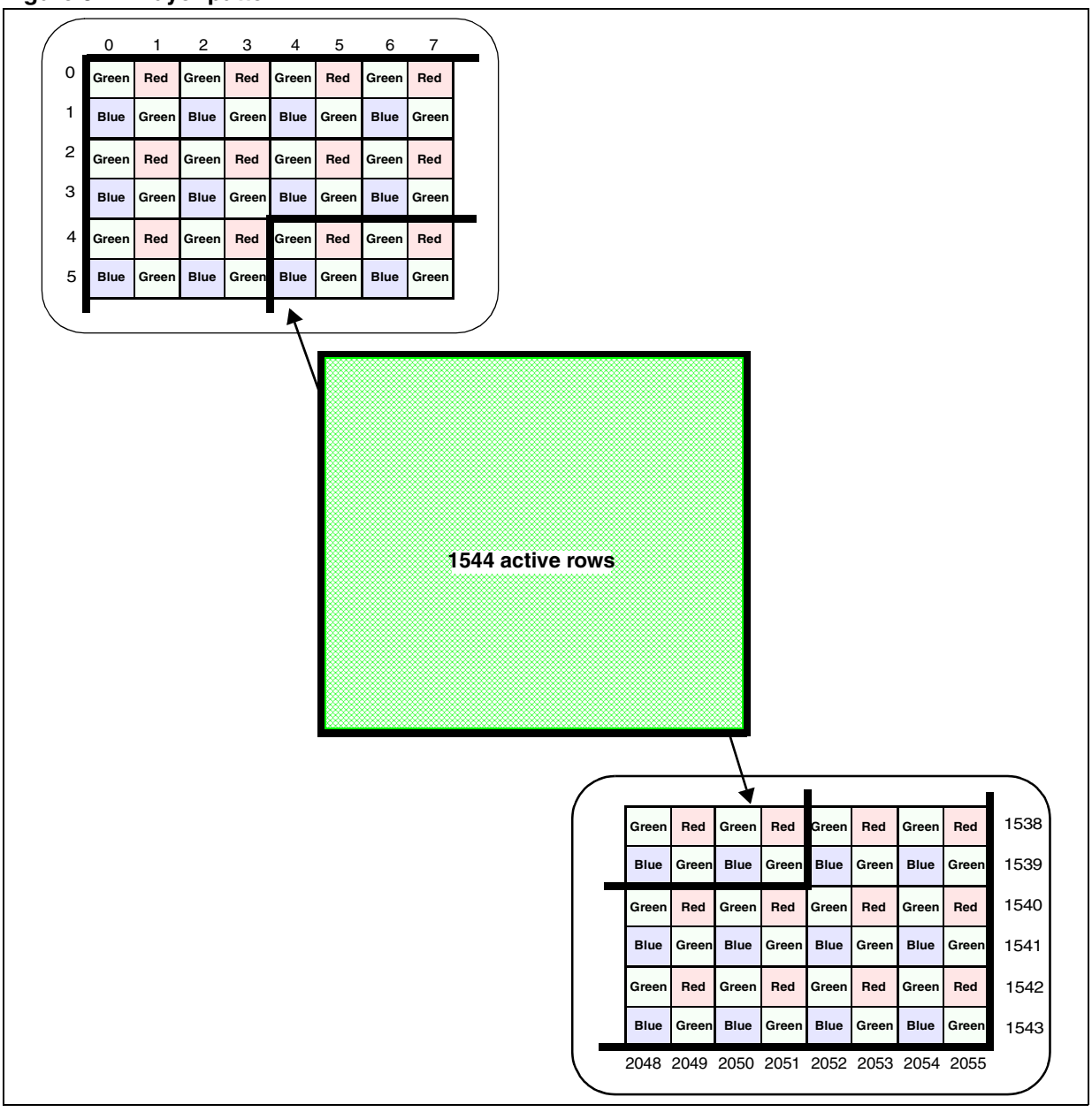
6.3 Bayer pattern

The three color (Red, Green, Blue) filters are arranged over the pixel array in a repeated 2x2 arrangement known as the Bayer pattern. When the sensor array is read, the output order of red, green, blue depends on the settings of vertical flip and horizontal mirror.

See *Figure 32* for read-out order for the default settings of vertical flip and horizontal mirror both turned off. Vertical flip will change the first line to be output from a green/red line to a blue/green line and horizontal mirror will change the sequence within a line, say, green/red to red/green.

As shown in *Figure 32*, the first pixel to be readout from the imaging array will be green followed by red.

Figure 32. Bayer pattern



6.4 Exposure and gain control

VD6803 does not contain any form of automatic exposure control. To produce a correctly exposed image the integration period and analogue gain for the pixels must be calculated by an exposure control algorithm implemented externally. The parameters are the written to the VD6803 through the I^2C interface.

The exposure control parameters available on VD6803 are:

- fine integration time
- coarse integration time
- analogue gain
- digital gain

The exposure control parameter registers are defined in *Section 4.3: Register map on page 40*.

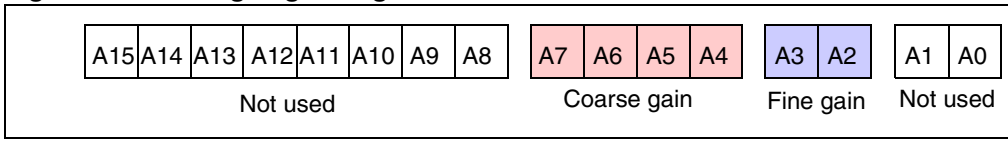
Integration time and analogue gain capability registers should be used to determine the exposure control parameter limits for a given video timing configuration. See Section 6.7 of the SMIA 1.0 part 1 specification for more information on how to interpret the integration and gain capability registers and how to calculate exposure and gain limits.

6.4.1 Analogue gain model

VD6803 only supports the single global analogue gain mode. VD6803 has a 16-bit register (0x0204 and 0x0205) to control analogue gain. However, only 4 bits are supported by the SMIA1.0 description. Two extra bits can be used for fine gain between values 8 and 16 but their description is not currently supported by SMIA1.0 specification.

Figure 33 shows the way the analogue gain bits are used for VD6803. Use only coarse gain bits for standard 1/x functionality.

Figure 33. Analogue gain register format



The following generic equation describes VD6803 coarse gain behavior specified by the analogue gain description registers 0x008A - 0x0093:

$$gain = c0 / (m1 \cdot x + c1)$$

where:

m1 = -1

c0 = 256

c1 = 256

Table 34 specifies the valid analogue gain values for VD6803.

Table 34. Analogue gain control

Gain value (0x0204/0x0205)	Coarse gain code [A7:A4]	Coarse analogue gain	Fine gain code [A3:A2]	Fine analogue gain
0x0000	0000	0.00 dB (x1.00)	00	N/A
0x0010	0001	0.56 dB (x 1.07)	00	N/A
0x0020	0010	1.16 dB (x1.14)	00	N/A
0x0030	0011	1.80 dB (x1.23)	00	N/A
0x0040	0100	2.50 dB (x1.33)	00	N/A
0x0050	0101	3.25 dB (x1.45)	00	N/A
0x0060	0110	4.10 dB (x1.60)	00	N/A
0x0070	0111	5.00 dB (x1.78)	00	N/A
0x0080	1000	6.00 dB(x2.00)	00	N/A
0x0090	1001	7.20 dB (x2.29)	00	N/A
0x00A0	1010	8.50 dB (x2.66)	00	N/A
0x00B0	1011	10.10 dB (x3.20)	00	N/A
0x00C0	1100	12.00 dB (x4.00)	00	N/A
0x00D0	1101	14.50 dB (x5.31)	00	N/A
0x00E0	1110	18.10 dB (x8.03)	00	N/A
0x00E4	1110	fine ctrl	01	19.20 dB (x9.12)
0x00E8	1110	fine ctrl	10	20.60 dB (x10.72)
0x00EC	1110	fine ctrl	11	22.10 dB (x12.74)
0x00F0	1111	24.10 dB (x16.03)	00	N/A

Please also refer to Section 6.3 of the SMIA1.0 specification document.

6.4.2 Digital gain

To help compensate for the relatively coarse analogue gain steps, VD6803 contains a digital multiplier to “fill” in the missing steps. By mixing analogue and digital gain it is possible to implement 3% gain steps across the full 1x to 16x gain range.

The details of the digital gain implementation are listed below:

- four individual 16-bit digital channel gains (one per Bayer channel):
  - digital_gain_greenR (0x020E and 0x020F)
  - digital_gain_red (0x0210 and 0x0211)
  - digital_gain_blue (0x0212 and 0x0213)
  - digital_gain_greenB (0x0214 and 0x0215)
- the digital gain range for each channel is 1.000 to 1.96875 in steps of 0.03125 (1/32) that is, five fractional bits:
  - digital_gain_min {0x1084:0x1085} = 0x0100 (1.00)
  - digital_gain_max {0x1086:0x1087} = 0x01F8 (1.96875)
  - digital_gain_step {0x1088:0x1089} = 0x0008 (0.03125)

6.4.3 Integration and gain parameter re-timing

The modification of exposure parameter (coarse, fine, clock division or gain) register values does not take effect immediately.

The exact time at which changes to certain parameters take effect is controlled both to ensure that each frame of image data produced has consistent settings and that changes in groups of related parameters can is synchronized.

To eliminate the possibility of the sensor array seeing only part of the new exposure and gain setting, if the serial interface communications extends over a frame boundary, the internal re-timing of exposure and gain data is disabled while writing data to the serial interface register map. Thus if the 5 bytes of exposure and gain data is sent as an auto-increment I^2C sequence, it is not possible for the sensor to consume only part of the new exposure and gain data.

However if it is not possible for the host to use auto-increment I^2C register accesses and only discrete register accesses are possible then the VD6803 has a mechanism to temporarily suspend the automatic application of updated exposure register values.

A group of parameter changes is marked by the host using a dedicated Boolean control parameter, grouped_parameter_hold (register 0x0104). Any changes made to ‘retimed’ parameters while the grouped_parameter_hold signal is in the ‘hold’ state will be considered part of the same group. Only when the grouped_parameter_hold control signal is moved back to the default ‘no-hold’ state should the group of changes be executed.

7 Test modes

To aid the debugging of systems that include ST sensors, VD6803 includes a number of test patterns.

Test modes can be set up that break various normal limits, it is up to the user of these test features to verify that the configuration that is being used is valid.

7.1 Full-frame deterministic test patterns

Two types of full-frame deterministic test patterns are defined. The Bayer test patterns are more suitable for some deterministic tests than real image data and are injected early in the sensor data path. The only exception to this is the PN9 test pattern that is intended to test sensor-host link integrity, the data in this pattern is not Bayer data and is injected into the data stream just prior to framing.

Use of these full-frame test patterns is controlled by the test_pattern_mode parameter (register 0x0600 and 0x0601). The VD6803/VD6803T provides SMIA test patterns and manufacturer specific test patterns. The SMIA available modes are:

- 0 - normal operation (default)
- 1 - solid color
- 2 - 100% color bars
- 3 - “fade to gray” color bars
- 4 - PN9

The manufacturer test patterns are:

- 0 - horizontal grayscale
- 1 - vertical grayscale
- 2 - diagonal grayscale
- 3 - PN28 pseudo-random sequence
- 4 - video-timing horizontal grayscale
- 5 - video-timing vertical grayscale
- 6 - video-timing PN28 pseudo-random sequence

The individual test patterns are described later in this chapter.

7.1.1 Solid color mode

In the solid colour test pattern mode, all active pixel data is replaced with fixed Bayer test data that is defined by the four 16-bit test data colour parameters registers (0x0602 to 0x609). These are 10-bit values.

7.1.2 100% color bars pattern mode

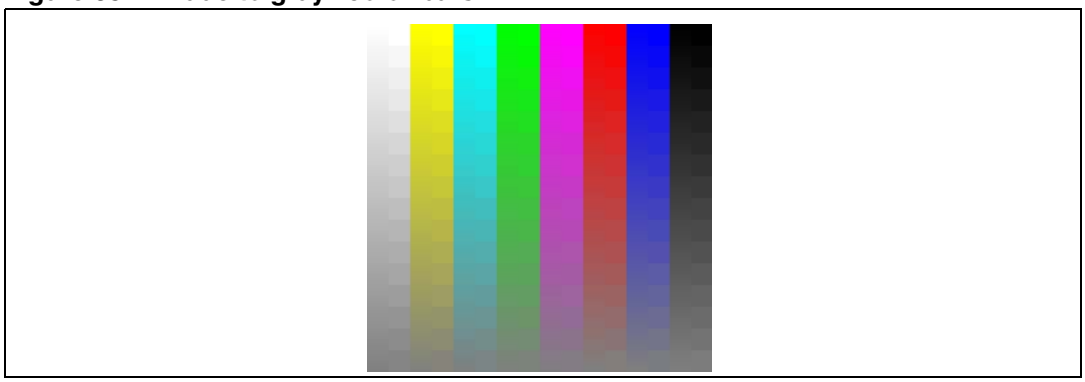
In the ‘100% color bar’ test pattern mode all pixel data is replaced with a Bayer version of an 8-bar color bar pattern. In each bar all pixels are either 0% or 100% full scale (for example, 100/0/100/0 bars).

Figure 34. 100% color bars

7.1.3 “Fade to gray” color bar mode

In the “fade to gray” color bar test pattern mode all pixel data is replaced with a color bar that fades vertically from 100% color bars to mid gray. The “fade to gray” color bar pattern is designed to exercise more of the color space than 100% bars whilst still requiring minimal hardware overhead. The following figure gives an indication of the pattern (although the pattern is generated as Bayer data).

Figure 35. “Fade to gray” color bars



The pattern is made up of eight vertical bars that fade vertically from one of the 100% color bar colors towards a mid-gray at the bottom. The bars follow the same order as standard color bars.

Each of the bars is sub-divided vertically into a left hand side that contains a smooth gradient and a right-hand size that contains a quantized version.

The aim of the quantized portion is to offer areas of flat-field Bayer data that should be large enough to result in known data values even after demosaic (independently of the demosaic algorithm). To ensure maximum dynamic range in the quantized data, the LSBs of the quantized data is generated by copying the MSBs of the unquantized data (rather than forcing them to 0). The pattern may roll over and repeat if the frames is long enough.

7.1.4 PN9 mode

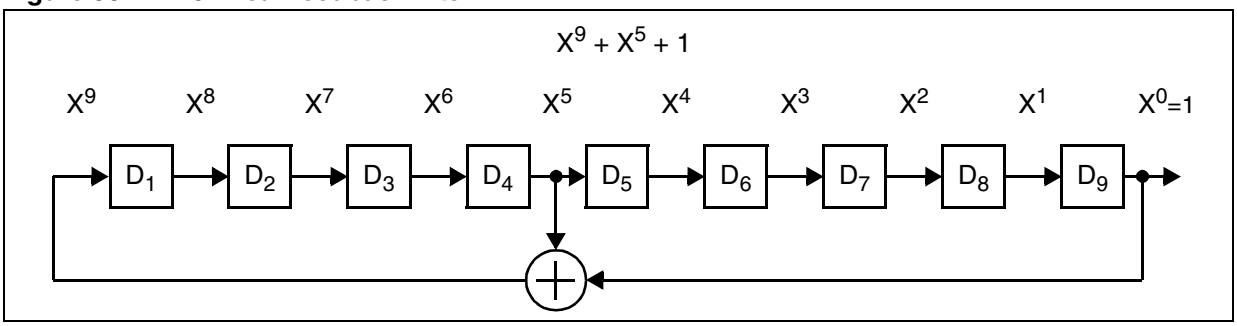
In PN9 test pattern mode, all pixel data is replaced with data from an internally generated 511-bit pseudo-random PN9 sequence.

The PN9 test pattern is included to ease testing of sensor-link integrity (measurement of bit error rate, for example). The standard PN9 linear feedback shift register with polynomial X^9+X^5+1 in Fibonacci-type notation is shown in *Figure 36*. The PN9 sequence generator is reset at the start of the frame, the sequence is then in a known state (0x1FF) at the first replaced pixel of each frame.

Note: The frame format descriptors do not correctly report the frame format in this mode.

Entering the PN9 test mode must be performed when the sensor is in software standby.

Figure 36. PN9 linear feedback filter



7.2 Test cursors

In addition to generation of full-frame deterministic test patterns, the VD6803 sensor can superimpose simple ‘cursors’ on the image. The cursors are generated by replacing Bayer pixel data with fixed Bayer data within narrow vertical and/or horizontal bands of the image. Injection of the test cursors must be arranged such that the cursors can be superimposed on top of the full-frame test patterns as well as array image data.

Two cursors are defined, one vertical cursor and one horizontal. The four parameters described in the following table are used to control the cursors. The position and width of each cursor can be controlled manually. Each cursor can be inhibited by setting its width parameter to zero. A value of 0x0FFFF in register vertical_cursor_position switches the vertical cursor into automatic mode where it automatically advances every frame (the initial position of the automatic cursor is undefined). The first pixel of the cursor replaces the pixel data at the horizontal_cursor_position-1 pixel. The width of the cursor can incremented in steps of one. The maximum valid value for horizontal_cursor_position and vertical_cursor_position is the associated x/ output size.

Table 35. Registers used to define the output data

Index	Byte	Register name
0x060A	Hi	horizontal_cursor_width
0x060B	Lo	
0x060C	Hi	horizontal_cursor_position
0x060D	Lo	
0x060E	Hi	vertical_cursor_width
0x060F	Lo	
0x0610	Hi	vertical_cursor_position
0x0611	Lo	

The four registers used to define the output data in solid colour mode also define the Bayer data used for the image cursors.

8 Color matrix

The sensor register map includes some static, read only parameters that define a recommended color space conversion matrix. As the parameters are static, a host only needs to read them once.

The matrix is specified so as to transform pixel data from the native sensor RGB color space to the color space of sRGB (ITU-R BT.709 reference primaries and a white point of D65, see http://www.srgb.com). *Figure 37* shows how the matrix can be used and how the nine elements of the 3x3 matrix are named.

Figure 37. Color matrix

$$\begin{bmatrix} r \\ g \\ b \end{bmatrix}_{sRGB} = \begin{bmatrix} RedInRed & GrnInRed & BluInRed \\ RedInGrn & GrnInGrn & BluInGrn \\ RedInBlu & GrnInBlu & BluInBlu \end{bmatrix} x \begin{bmatrix} r \\ g \\ b \end{bmatrix}_{sensor}$$

The matrix elements are included in the sensor register map (registers 0x1400 to 0x1411) as 16-bit signed iReal parameters The 16-bit signed iReal was chosen primarily so as to have a well-defined format that offered sufficient range and precision. It is expected that few hosts (hardware or software) will actually use all the elements at this precision.

Table 36. Color matrix parameters

Parameter	Description
RedInRed	The recommended amount of the sensor red signal to be included in the output red signal
GreenInRed	The recommended amount of the sensor green signal to be included in the output red signal
BlueInRed	The recommended amount of the sensor blue signal to be included in the output red signal
RedInGreen	The recommended amount of the sensor red signal to be included in the output green signal
GreenInGreen	The recommended amount of the sensor green signal to be included in the output green signal
BlueInGreen	The recommended amount of the sensor blue signal to be included in the output green signal
RedInBlue	The recommended amount of the sensor red signal to be included in the output blue signal
GreenInBlue	The recommended amount of the sensor green signal to be included in the output blue signal
BlueInBlue	The recommended amount of the sensor blue signal to be included in the output blue signal

9 Electrical characteristics

9.1 Absolute maximum ratings

Table 37. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DIGMAX}	Digital power supply	-0.5	2.9	V
V_{ANAMAX}	Analog power supply	-0.5	3.4	V
V_{IHMAX}	EXTCLK, XSHUTDOWN, SCL, SDA	-0.5	VDIG+0.5	V
V_{CAP}	VCAP analogue voltage	-0.3	4.2	V
T_{STO}	Storage temperature	-40	+ 85(1)	°C
V_{ESD}	Electrostatic discharge model Human body model(2) Charge device model(3)	 -2 -500	 2 500	 kV V

1. This is a maximum, long-term, standard storage temperature, see soldering profile for short-term, high temperature tolerance.
2. HBM tests have been performed in compliance with JESD22-A114D.
3. CDM tests have been performed in compliance with JESD22-C101A.

Caution: Stresses above those listed in *Table 37* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9.2 Operating conditions

Table 38. Operating conditions

Symbol	Parameter		Min.	Typ.	Max.	Unit
Voltage						
VDIG	Digital power supply	Parallel mode 1(1)	1.7	1.8	1.9	V
		Parallel mode 2(2)	2.5	2.8	2.9	V
VANA	Analog power supply		2.5	2.8	2.9	V
VIP(DIG)	Digital input voltage(3)		0	-	VANA	V
Temperature						
T_{AS}	Temperature (storage)(4)		-40	-	+85	°C
T_{AF}	Temperature (functional operating)(5)		-30		+70	°C
T_{AN}	Temperature (normal operating)(6)		-25		+55	°C
T_{AO}	Temperature (optimal operating)(7)		+5		+40	°C
T_{AT}	Temperature (test)(8)		+21		+25	°C

1. In Parallel Mode 1, the digital part operates from 1v7 to 1v9 and the analogue part operates from 2v5 to 2v9.
2. In Parallel Mode 2, the analogue and digital supplies are supplied by the same power supply. In the case where VDIG is not connected to VANA, VANA supply must be higher than VDIG supply
3. Digital input: EXTCLK, XSHUTDOWN, SCL, SDA
4. Storage temperature: Camera has no permanent degradation.
5. Functional operating temperature: Camera is electrically functional.
6. Normal operating temperature: Camera produces ‘acceptable’ images.
7. Optimum performance temperature: Camera produces optimal optical performance.
8. Test temperature: 100% tested parameters are measured at this temperature.

Note: The figures given in Table 38 will be qualified by environmental testing.

9.3 DC electrical characteristics

Typical values are quoted for nominal voltage, process and temperature. Maximum values are quoted for worst case conditions (process, voltage and functional temperature) unless otherwise specified.

9.3.1 Power supply (VDIG, VANA)

Table 39. Power supply (VDIG, VANA)

Parameter	Digital 1V8		Analogue		Unit
	Typ.	Max	Typ.	Max.	
Hardware standby(1)	2.5	80	2.5	10	µA
Software standby:					
Ext. clock not switching	1.0	7	0.0025	0.01	mA
Ext. clock switching(2)	1.5	8	0.0025	0.01	mA
Streaming, full resolution(3):					
EDOF OFF	115	126	41	45	mA
EDOF ON (Macro)	217	236	41	45	mA
EDOF ON (Infinity)	204	229	41	45	mA

1. Measured across process and voltage and at test temperature.
2. External clock active, 6 MHz. The digital current scales linearly with the external clock frequency used.
3. 20 fps.

9.3.2 System clock (EXTCLK)

Table 40. System clock (EXTCK)

Symbol	Parameter	Min.	Max.	Unit
	Leakage current	4(1)	30(2)	µA

1. With DC coupled square wave clock.
2. With DC VDIG applied.

9.3.3 Power down control (XSHUTDOWN)

Table 41. Power down control (XSHUTDOWN)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	0	-	0.3 VDIG	V
V_{IH}	High level input voltage	0.7 VDIG	-	2.9(1)	V

1. XSHUTDOWN is a 2V9 tolerant input.

9.3.4 I²C interface (SDA, SCL)

Table 42. I²C interface DC electrical characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	0	-	0.3*VDIG	V
V_{IH}	High level input voltage	0.7*VDIG	-	VDIG	V
V_{OL}	Low level output voltage(1) (2)	0	-	0.2*VDIG	V
I_{IL}	Low level input current	-	-	-10	µA
I_{IH}	High level input current	-	-	10	µA

1. V_{OH} not valid for I²C.
2. 1 mA drive strength.

9.3.5 Recommendations for module makers

The VD6803 module can be sensitive to the external clock noise. The noise on the input clock can cause the device to misclock. To solve this, it is recommended that noisy signal tracks are separated. An RC filter can also be placed close to the external clock input of the VD6803. This will make the pixel clock less susceptible to noise pick-up. Please, refer to the related Application Note from STMicroelectronics.

9.4 AC electrical and timing characteristics

Typical values are quoted for nominal voltage, process and temperature. Maximum values are quoted for worst case conditions (process, voltage and functional temperature) unless otherwise specified.

9.4.1 Power supply, peak current (VDIG, VANA)

Table 43. Power supply, peak current (VDIG, VANA)

Parameter	Peak current(1)		Unit
	Digital	Analogue	
Streaming, streaming EDOF Macro Mode	231	60	mA

1. The peak current consumption of the sensor module is defined as any current pulse >=10µs. Peak current is assumed to be <1.33 x max average current for the stated operating mode and worst case conditions. The duty cycle of the peak to the low part of the current profile is 33% with a worst-case period of 500 µs.

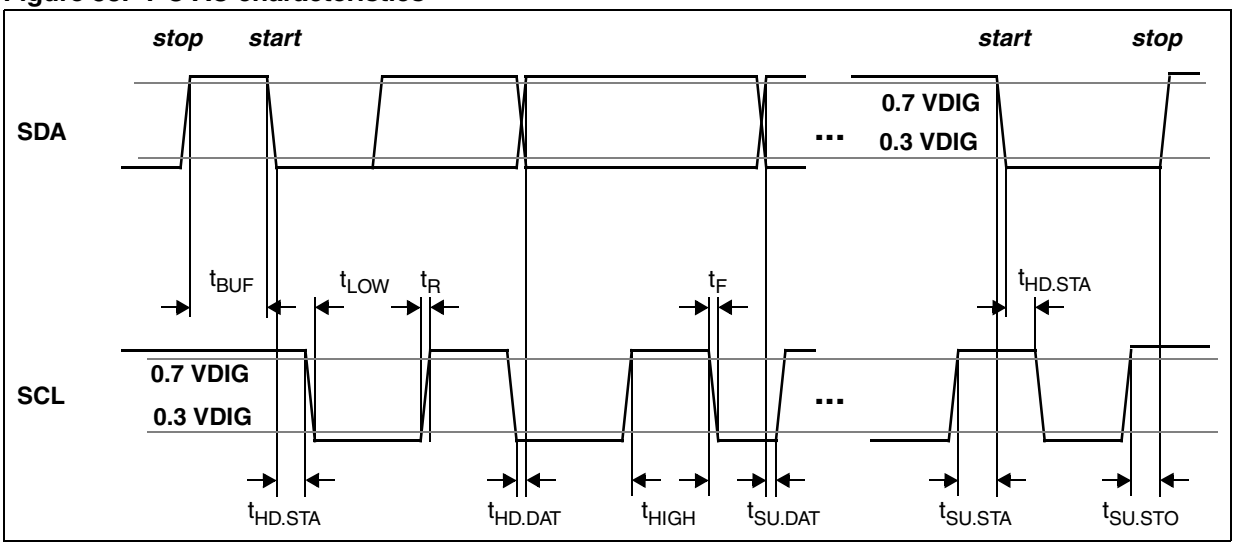
9.4.2 I²C interface, timing characteristics

Table 44. I²C interface, timing characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SCL}	SCL clock frequency	0	-	400	kHz
t_{LOW}	Clock pulse width low	1.3	-	-	µs
t_{HIGH}	Clock pulse width high	0.6	-	-	µs
t_{SP}	Pulse width of spikes which are suppressed by the input filter	0	-	50	ns
t_{BUF}	Bus free time between transmissions	1.3	-	-	µs
$t_{HD.STA}$	Start hold time	0.6	-	-	µs
$t_{SU.STA}$	Start set-up time	0.6	-	-	µs
$t_{HD.DAT}$	Data in hold time	0	-	0.9	µs
$t_{SU.DAT}$	Data in set-up time	100	-	-	ns
t_R	SCL/SDA rise time	20+0.1 Cb(1)	-	300	ns
t_F	SCL/SDA fall time	20+0.1 Cb(1)	-	300	ns
$t_{SU.STO}$	Stop set-up time	0.6	-	-	µs
Ci/o	Input/output capacitance (SDA)	-	-	8	pF
Cin	Input capacitance (SCL)	-	-	6	pF

1. Cb = total capacitance of one bus line in pF.

Figure 38. I²C AC characteristics



All timings are measured from either 0.3 VDIG or 0.7 VDIG.

For further information on the I²C interface, please refer to the SMIA 1.0 part 2: CCP Specification.

9.4.3 Parallel port interface

VD6803 contains a parallel data output port (D[9:0]) and associated qualification signals (HSYNC, VSYNC, PCLK). This port can be enabled and disabled (tri-stated) to facilitate multiple camera systems.

Figure 39. VD6803 10-bit parallel interface detailed timings

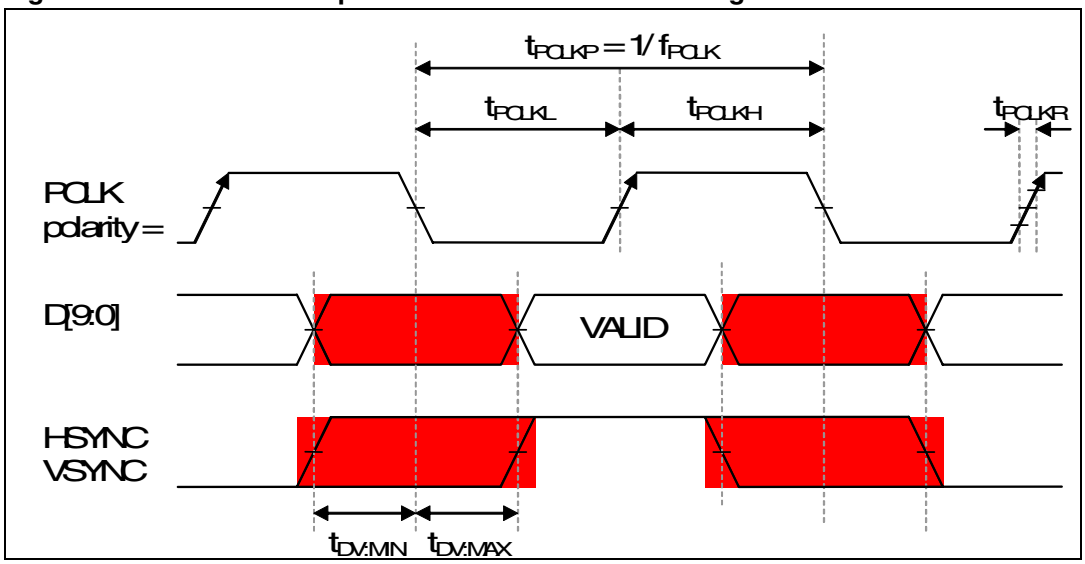


Table 45. VD6803 10-bit parallel interface detailed timings (up to 80 MHz)

Symbol	Description	Min.	Typ.	Max.	Units
1/ fPCLK	PCLK frequency(1)			80.0	MHz
tPCLKP	PCLK period(1)	12.5			ns
tPCLKL	PCLK low width(1)			5.0	ns
tPCLKH	PCLK high width(1)			5.2	ns
tPCLKR	PCLK rise time 20% - 80%(1)			3.0	ns
tDV	PCLK to output valid(1)	2.3	2.8	4.0	ns

1. With a 20 pF capacitive load.

Table 46. VD6803 10-bit parallel interface electrical characteristics

Symbol	Description	1V8	2V8	Unit
V_{OL}	Output low voltage	0.15	0.4	V
V_{OH}	Output high voltage	V_{SUPPLY} - 0.25	V_{SUPPLY} - 0.4	V
I_{OL}/I_{OH}	Output high/low current	4	16	mA

10 Digital auto focus control

10.1 Operating modes

The digital auto focus (DAF) operates in two modes:

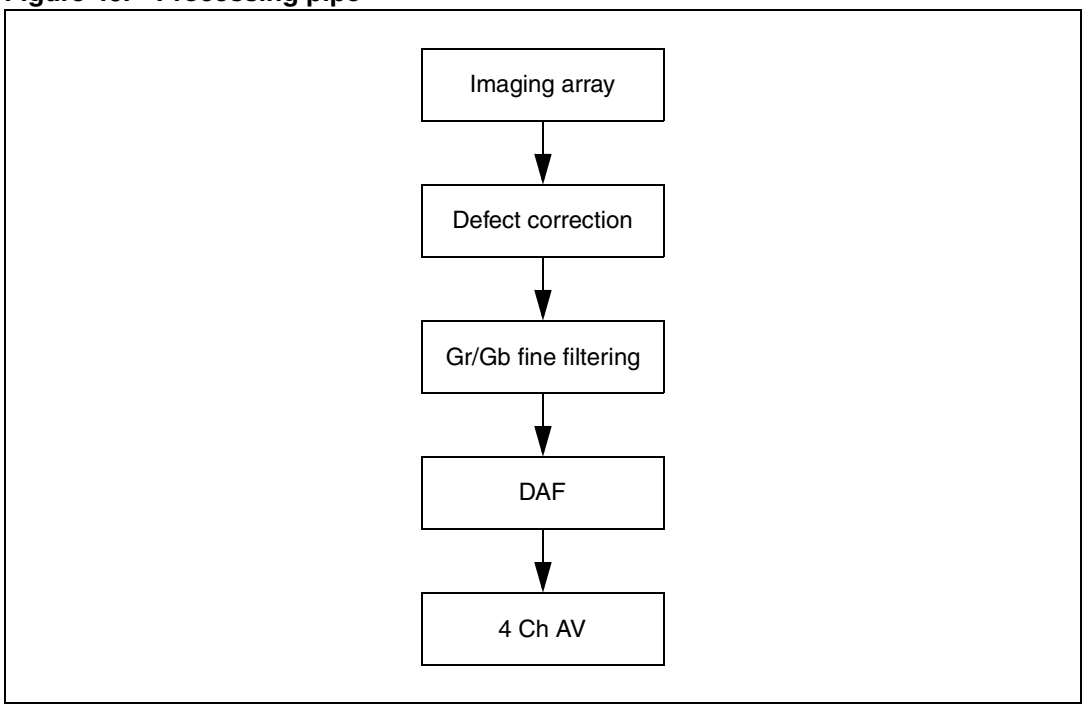
- Preview mode

  In this mode the DAF engine keeps the original images and does not correct them.

- Still capture mode

  This mode corrects the image, according to the characteristics of the selected scene type. Different renderings depending on the distance can be applied: for instance sharp saturated rendering for General Purpose mode, soft rendering for Low Light mode and sharp contrasted rendering for Macro mode.

Figure 40. Processing pipe



10.2 Tuning parameters (capture mode)

The EDOF functionality is disabled by default. It can be enabled by the host system in either software standby or streaming using the EDOF_Enable register (0x3328). The EDOF IP embeds a defect correction block and a noise reduction block which can be used stand-alone even if the EDOF is inactive. The EDOF_Status register (0x3330) is used to control whether or not the defect correction and noise reduction blocks are active when EDOF is disabled.

10.2.1 EDOF Software Lens™ Parameter (SLP) control

When the EDOF is active, there are two distinct operation modes: auto or manual. The selection is done using the EDOF_mode register (0x3331).

The following operating modes are available in capture.

- **General Purpose** is suitable for most picture taking scenes (default mode).
- **Low-Light** softens the image to reduce the noise in low light conditions. There are two low-light modes to handle low-light treatment. These are **Low-Light 1** for mild low-light and **Low-Light 2** for more extreme conditions. This mode can be automatically or manually selected.
- **Macro** uses sharpening for capturing objects in the range of 15 to 25 cm. This mode can only be selected manually.
- **Barcode** is the best mode used for machine vision algorithms like barcode reading (1D, 2D like QR-Codes). This mode can only be selected manually.

The VD6803/VD6803T embeds dedicated Software-Lens™ Parameter (SLP) configurations. The SLPs control the image-processing characteristics of the Software-Lens™. They are composed of deconvolution filters (DCFs) and processing registers. The DCF coefficients generally define spatially-dependent filters that are matched to the camera lens and can also be co-optimized with other filters from the camera system pipeline.

In manual mode, the selection of the SLP configuration is done using the SLP_Selected register (0x3332).

10.2.2 EDOF auto mode operation

In auto mode operation, the camera automatically selects between the General purpose SLP, Low-Light 1 SLP or Low-Light 2 SLP. The Macro and Barcode modes cannot be selected in auto mode (only in manual mode).

The method of selecting the SLP in auto mode varies depending on a number of control registers. The Low_Light_Ctrl_Mechanism register (0x3338) can be used to select between host-provided low-light mechanism and internal gain thresholds.

In the case of host-provided low-light mechanism, the embedded software uses the value written by the host in the Host_Low_Light_Estimate register (0x3339) to determine if the host is requesting a General Purpose or a Low-Light SLP. For a Low-Light SLP, the Spare_3 register (0x333F) determines whether Low-Light 1 or Low-Light 2 SLP is required.

In the case of gain thresholds selection, the camera calculates the current gain settings at the end of the frame and compares it to the gain thresholds. The Low-Light 1 SLP has been defined to relate to a gain setting of 4-6. The Low-Light 2 SLP relates to a gain setting greater than 6. Therefore, the gain thresholds are set to 4 and 6.

In auto mode operation, the last control relates to the hysteresis control of the switching between SLPs. The Active_Management_Hysteresis_Ctrl register (0x3335) allows a number of hysteresis frames to be specified. This means a number of consecutive frames with the same optimum DCF have been found before a change of SLP is selected. This avoids the situation where the SLP is continually switching frame by frame when the camera operation is close to a gain threshold.

10.2.3 Sharpness level

The sharpness level is controlled by a set of highly capable sharpening filters. The default filters suitable for the different operating modes are embedded in the sensor. However, the filters can be overwritten by the host to control the level and fine details of the sharpening filters.

10.2.4 Noise level

The noise level is detected using two programmable gain thresholds. By default, low-noise settings are selected for gains inferior to “4”, mid-noise settings for gain between “4” and “6” and high-noise settings for gain superior or equal to “6”. In auto mode, the firmware detects the noise region and selects the appropriate SLP.

10.3 Defect correction

The defect correction algorithm detects and corrects all defective pixels in the imaging array.

10.4 Gb/Gr fine filter

The Gb/Gr fine filter can be used to remove any GreenRed/GreenBlue mismatch.

10.5 Anti-vignette

This block can be used to correct any vignetting effect.

10.6 Example code

Contact STMicroelectronics for the latest application notes regarding reading the digital auto focus configuration.

11 Defect categorization

In this chapter, STMicroelectronics provides recommended test guidelines for the module manufacturer to perform.

11.1 Pixel defects

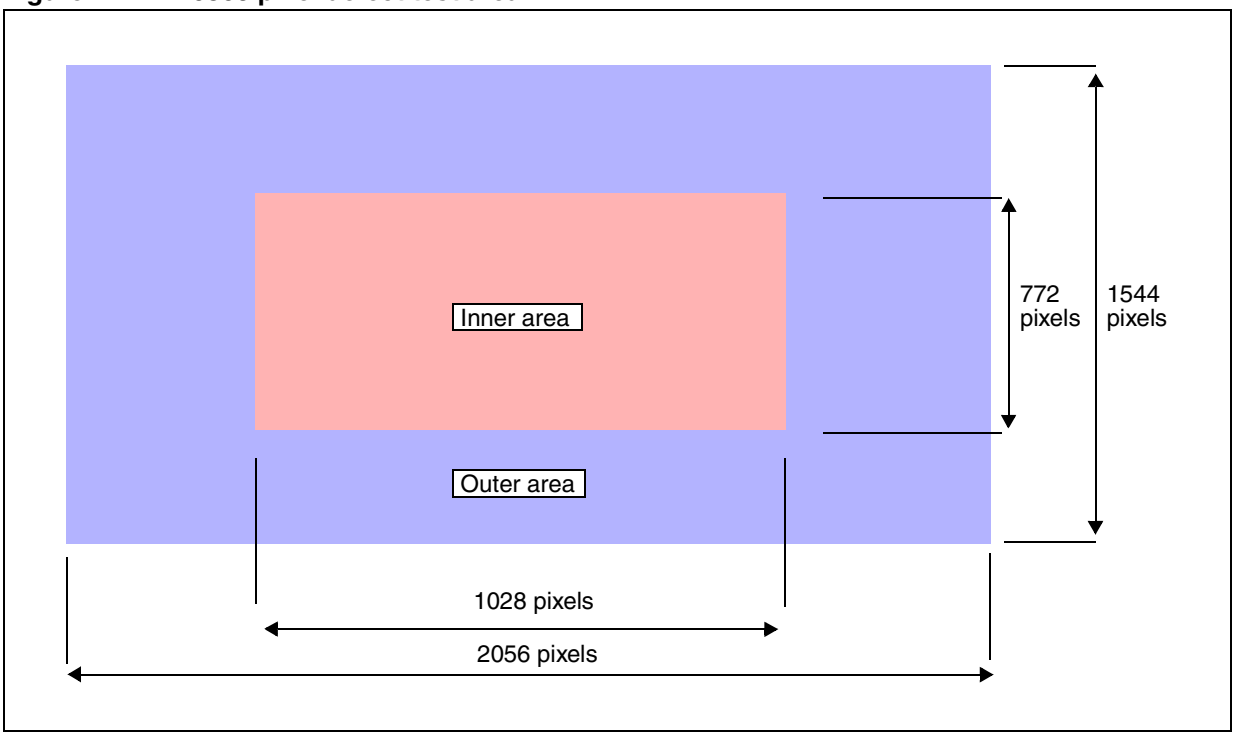
Illuminated defects are tested with a flat field illumination and a pass-fail criteria that is a percentage deviation from a local mean. In order for the sensor to be effectively tested in a reasonable test time, it is necessary to put the limits of gain error above the normal noise distribution of photon shot noise and sensor noise otherwise false single pixel fails will be detected. A typical defect criteria for single-pixel gain errors is ± 9%. In fact, any element in the array outside ±9% is a “minor” fail, and outside of ± 25% is a “major” fail.

Note: The defect detection method is applied to raw Bayer images.

11.2 Sensor array area definition

For specific aspects of pixel defect testing the image sensor array is subdivided into two regions as illustrated in *Figure 41*.

Figure 41. VD6803 pixel defect test area



The inner array in *Figure 41* is centre justified, in the x and y axis, with respect to the outer array. The inner array is 50% of the full width and 50% of the full height of the larger outer array, therefore the inner array is one quarter of the area of the outer array.

Note: The border pixels (outer four rows and columns) affect the image quality of the reconstructed picture to a lesser degree than the actual image pixels (2048 x 1536), due to their lower contribution within the reconstruction algorithm, BUT for simplicity we test them as the image pixels, therefore the test image size for defects is 2056 x 1544.

11.3 Pixel fault numbering convention

The pixel notation is described in *Figure 42*. For the purposes of the test the 3x3 array describes nine Bayer pixels of a common color, that is, **all the pixels are either Red, Green**[(b)] **or Blue**. The pixel under test is **X**. If a pixel under test is on the edge, the array is reduced to its existing neighbor pixels (that is, the 1st pixel uses only a 2x2 array).

Figure 42. Pixel numbering notation

[0]	[1]	[2]
[7]	**X**	[3]
[6]	[5]	[4]

11.4 Single pixel faults

STMicroelectronics defines a single pixel fail as a failing pixel with no adjacent failing same color neighbors. A single pixel fail can be:

- stuck at white where the output of the pixel is permanently saturated regardless of the level of incident light and exposure level
- stuck at black where the pixel output is zero regardless of the level of incident light and exposure level (major fail)
- a pixel that differs from its immediate neighbors by more than the test threshold (minor fail)

In the example in *Figure 43* we assume the pixel **X** is a fail. For this pixel to be a single pixel fail the pixels at positions [0], [1], [2], [3], [4], [5], [6] and [7] must be “good” pixels that pass final test. The implemented test program will pass a sensor with up to the defined limit of single pixel faults per color channel. Defect correction algorithms will correct the pixel faults in the final image.

Figure 43. Single pixel fault

[0]	[1]	[2]
[7]	**X**	[3]
[6]	[5]	[4]

b. The Green pixels are split over two common channels, Green1 and Green2.

11.5 Couplet definition

A failing pixel at **X** with a failing pixel at position [0], [1], [2], [3], [4], [5], [6] or [7] so that there is a maximum of two failing pixels from the group of nine pixels. The example shown in *Figure 44* has the centre pixel and the pixel at position [7] failing the test criteria.

Figure 44. General couplet example

[0]	[1]	[2]
[X]	**X**	[3]
[6]	[5]	[4]

The basic couplet definition is further subdivided into minor and major couplets. With respect to the example in *Figure 44*, a minor couplet is defined as a defect pixel pair where one pixel can be an extreme fail, that is a stuck at black or stuck at white, but the second pixel in the pair must differ from the local pixel average by less than 25% of that average value. If the second pixel in the couplet differs by more than 25% of the local pixel average value then this would be defined as a major couplet.

In addition, couplets are classified as being in the inner or outer area.

11.6 On-chip defect correction

The Bruce defect correction filter is designed to intelligently correct the first defect in a couplet thereby changing a couplet into a single pixel defect. Single pixel defects can then be corrected using the defect correction filter.

The Bruce filter requires exact coordinate information for each of the couplets to be repaired. The couplet coordinates are stored in non-volatile-memory (NVM) during production test.

The Bruce filter does not operate in analog binning mode or in sub sample mode and should be disabled.

The selection of the Bruce filter is controlled using register MAN_SPEC_BRUCE (0x31F0):

0 - Bruce filter off (default)

1 - Bruce Filter on

12 Acronyms and abbreviations

Table 47. Acronyms and abbreviations

Acronym/ abbreviation	Definition
CCP	Compact camera port
DAF	Digital auto-focus
DCF	Deconvolution filter
EDOF	Extended depth of field
EMI	Electromagnetic interference
EOF	End of frame
FE	Frame end
fps	Frames per second
FS	Frame start
HWA	Hardware accelerator
I^2C	Inter integrated circuit
ILP	In line processor
LE	Line end
LS	Line start
LSB	Least significant byte
LVDS	Low voltage differential signalling
Mbps	Megabits per second
MSB	Most significant byte
MSP	Manufacturer specific pixels
PCK	Pixel clock
PCM	Pulse code modulation
PLL	Phase locked loop
RO	Read only
RW	Read/write
SLP	Software Lens™ parameters
SMIA	Standard mobile imaging architecture
SOF	Start of frame
SubLVDS	Sub-low voltage differential signaling

13 Revision history

Table 48. Document revision history

Date	Revision	Changes
09-Oct-2008	A1	Initial release.
17-Oct-2008	A2	Added *Section 4.3.15: NVM programming on page 58*. Updated *Chapter 9: Electrical characteristics on page 83*.
24-Oct-2008	A3	Added *Section 2.5: Bond pad details for TSV package on page 15*.
06-Nov-2008	A4	Added *Section 2.9: Chief ray angle (CRA) on page 22*.
21-Nov-2008	A5	Added *Chapter 10: Digital auto focus control on page 89*. Updated *Section 4.3: Register map on page 40*.
30-Jun-2009	A6	*Section 2.3: Bond pad positions and numbers on page 10*: – Updated *Figure 1: Bond pad positions, optical centre and die orientation on page 10* and added following note. – Added *Table 5: Bond pad positions and names for COB package* and *Table 6: Bond pad positions and names for TSV package on page 15*. *Chapter 9: Electrical characteristics on page 83*: – Updated *Table 37: Absolute maximum ratings on page 83*. – Updated *Table 38: Operating conditions on page 84*. – Updated *Table 39: Power supply (VDIG, VANA) on page 85*. – Added *Section 9.3.5: Recommendations for module makers on page 86*
06-Dec-2010	B	Updated capacitance figures in *Section 2.8.1: Application circuit for COB (chip-on-board) on page 20*. Updated *Section 2.10: Delivery/shipping method on page 23*. Updated *Table 17: Status registers [0x0000 to 0x000F] on page 40*. Removed Data format description registers [0x00C0 to 0x00FF]. Updated *Section 4.3.15: NVM programming on page 58* including example code *on page 61*. Updated *Pulse_width definition* and *Reading the NVM on page 62*. Removed the table entitled “External clock frequency examples, 3.15MP Raw10, 15fps”. Removed “Image compression”. Updated *Section 7.2: Test cursors on page 80*. Updated *Table 38: Operating conditions on page 84*. Updated *Table 39: Power supply (VDIG, VANA) on page 85*. Updated *Section 9.4.1: Power supply, peak current (VDIG, VANA) on page 86*. Updated *Table 45: VD6803 10-bit parallel interface detailed timings (up to 80 MHz) on page 88*. Removed Section 11.6: Physical aberrations.
02-Feb-2011	C	Modified t3 and t4 in *Table 10: Power-up sequence timing constraints on page 27*.
27-Apr-2011	D	Updates to *Table 39: Power supply (VDIG, VANA) on page 85*.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com