MOTOROLA Semiconductors
Colvilles Road, Kelvin Estate - East Kilbridge/Glasgow - SCOTLAND-UK

MC54/74HC86
MC54/74HC266

Advance Information

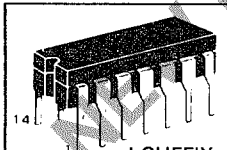
HIGH-PERFORMANCE
CMOS
(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT
EXCLUSIVE OR AND NOR GATES

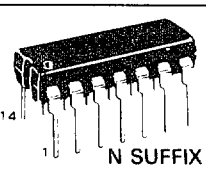
QUAD EXCLUSIVE OR AND NOR GATES

These gates utilize silicon-gate CMOS technology to achieve characteristics — including propagation delays — similar to the LSTTL 86 and 266 gates, with the low power consumption of standard CMOS integrated circuits. These gates have high noise immunity and buffered outputs. The 74HC device can drive ten LSTTL loads (eight LSTTL loads for 54HC). The MC54/74HC86 is functionally as well as pin compatible with the LSTTL counterpart. The MC54/74HC266 is pin compatible with the 74LS266, but has push-pull outputs rather than open collector.

- Expected Typical Propagation Delays: 12 ns
- Wide Operating Voltage Range: 3 to 6 volts
- Low Power Dissipation
- Low Input Current: 1 μA maximum
- Low Quiescent Current: 20 μA maximum (over full temperature range — 74 Series)
- Output Drive Capability: 10 LSTTL Loads (74HC Series)
  8 LSTTL Loads (54HC Series)



J SUFFIX
CERAMIC PACKAGE
CASE 632

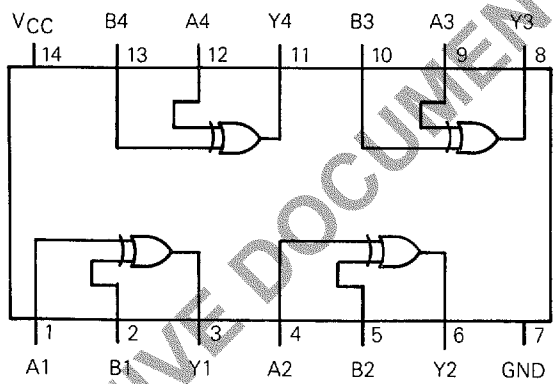


N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)
74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

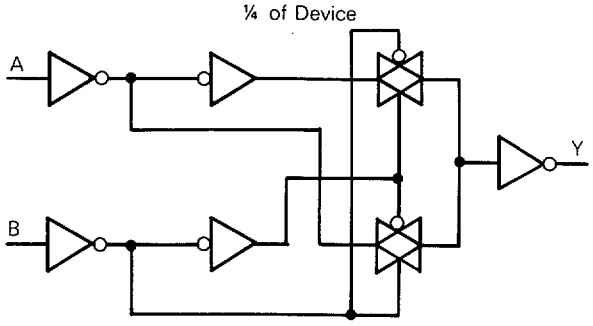
MC54HC86•MC74HC86
Quad Exclusive OR Gate



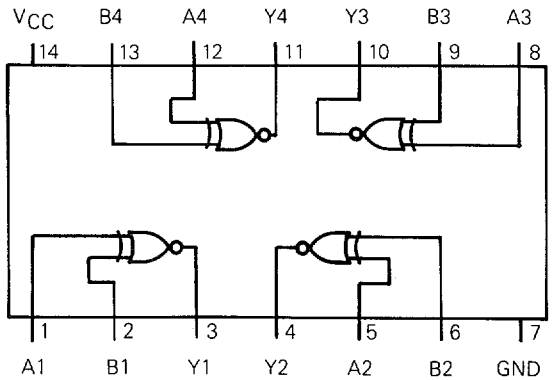
Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

$Y = A \oplus B = \overline{A}B + A\overline{B}$

Equivalent Circuit
¼ of Device



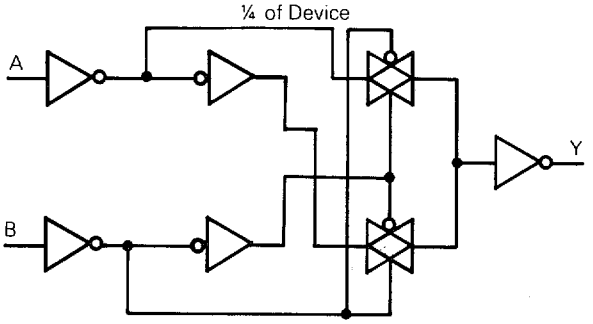
MC54HC266•MC74HC266
Quad Exclusive NOR Gate



Inputs		Outputs
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

$Y = \overline{A \oplus B} = AB + \overline{A}\,\overline{B}$

Equivalent Circuit
¼ of Device



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	−0.5 to 7.0	V
V_{in}, V_{out}	Input Voltage, Output Voltage	−0.5 to V_{CC}+0.5	V
I	DC Current Drain per Pin, Any Input or Output	25	mA
I	DC Current Drain, V_{CC} and GND Pins	50	mA
T_{stg}	Storage Temperature	−65 to +150	°C
P_D	Power Dissipation	500	mW
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Permanent device damage may occur if the Maximum Ratings are exceeded.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	3.0	6.0	V
V_{in}, V_{out}	Input Voltage, Output Voltage	0	V_{CC}	V
T_A	Operating Temperature — 74 Series 54 Series	−40 −55	+85 +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC}=5 V ±10%)

Symbol	Parameter	Test Conditions		Typ	Guaranteed Limit	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.5 V or V_{CC}−0.5 V, I_{out}≤1 μA	V_{CC}=4.5 V	–	3.15	V
			V_{CC}=5.5 V	–	3.85	
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.5 V or V_{CC}−0.5 V, I_{out}≤1 μA	V_{CC}=4.5 V	–	0.90	V
			V_{CC}=5.5 V	–	1.10	
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{CC} or GND, I_{out}≤1 μA		V_{CC}	V_{CC}−0.05	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{CC} or GND, I_{out}≤1 μA		0.0	0.05	V
I_{OH}	Minimum High-Level Output Current	V_{in}=V_{CC} or GND, V_{out}=V_{CC}−0.8 V	54 Series	–	−3.4	mA
			74 Series	–	−4.0	
I_{OL}	Minimum Low-Level Output Current	V_{in}=V_{CC} or GND, V_{out}=0.4 V	54 Series	–	3.4	mA
			74 Series	–	4.0	
I_{in}	Input Current	V_{in}=V_{CC} or GND		±0.00001	±1.0	μA
I_{CC}	Quiescent Current (Per Package)	V_{in}=V_{CC} or GND, I_{out}=0 μA	T_A=25°C	–	2	μA
			T_A=85°C	–	20	
			T_A=125°C	–	40	

*Unless otherwise specified, guaranteed limits are applicable over the full temperature range.

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r=t_f=6 ns)

Symbol	Parameter	Test Conditions	Typ	Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency	C_L=15 pF	40	30	MHz
		C_L=50 pF	30	20	
t_{PHL}/t_{PLH}	Maximum Propagation Delay	C_L=15 pF	9	25	ns
		C_L=50 pF	12	30	
t_{TLH}	Maximum Input Clock Rise Time		–	500	ns
C_{in}	Input Capacitance		5	10	pF
C_{PD}	Power-Dissipation Capacitance*		20	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption (per gate): $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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