

# NB2304A

## 3.3 V Zero Delay Clock Buffer

The NB2304A is a versatile, 3.3 V zero delay buffer designed to distribute high-speed clocks in PC, workstation, datacom, telecom and other high-performance applications. It is available in an 8 pin package. The part has an on-chip PLL which locks to an input clock presented on the REF pin. The PLL feedback is required to be driven to FBK pin, and can be obtained from one of the outputs. The input-to-output propagation delay is guaranteed to be less than 250 ps, and the output-to-output skew is guaranteed to be less than 200 ps.

The NB2304A has two Banks of two outputs each. Multiple NB2304A devices can accept the same input clock and distribute it. In this case, the skew between the outputs of the two devices is guaranteed to be less than 500 ps.

The NB2304A is available in two different configurations (Refer to NB2304A Configurations Table). The NB2304AI1 is the base part, where the output frequencies equal the reference if there is no counter in the feedback path. The NB2304AI1H is the high-drive version of the -1 and the rise and fall times on this device are much faster.

The NB2304AI2 allows the user to obtain REF, 1/2 X and 2X frequencies on each output Bank. The exact configuration and output frequencies depend on which output drives the feedback pin.

### Features

- Zero Input – Output Propagation Delay, Adjustable by Capacitive Load on FBK Input
- Multiple Configurations – Refer to NB2304A Configurations Table
- Input Frequency Range: 15 MHz to 133 MHz
- Multiple Low-Skew Outputs
- Output-Output Skew < 200 ps
- Device-Device Skew < 500 ps
- Two Banks of Four Outputs
- Less than 200 ps Cycle-to-Cycle Jitter (-1, -1H, -5H)
- Available in Space Saving, 8 pin 150 mil SOIC Package
- 3.3 V Operation
- Advanced 0.35  $\mu$  CMOS Technology
- Guaranteed Across Commercial and Industrial Temperature Ranges
- These are Pb-Free Devices



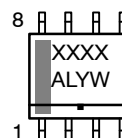
**ON Semiconductor®**

<http://onsemi.com>

### MARKING DIAGRAM\*



**SOIC-8  
D SUFFIX  
CASE 751**



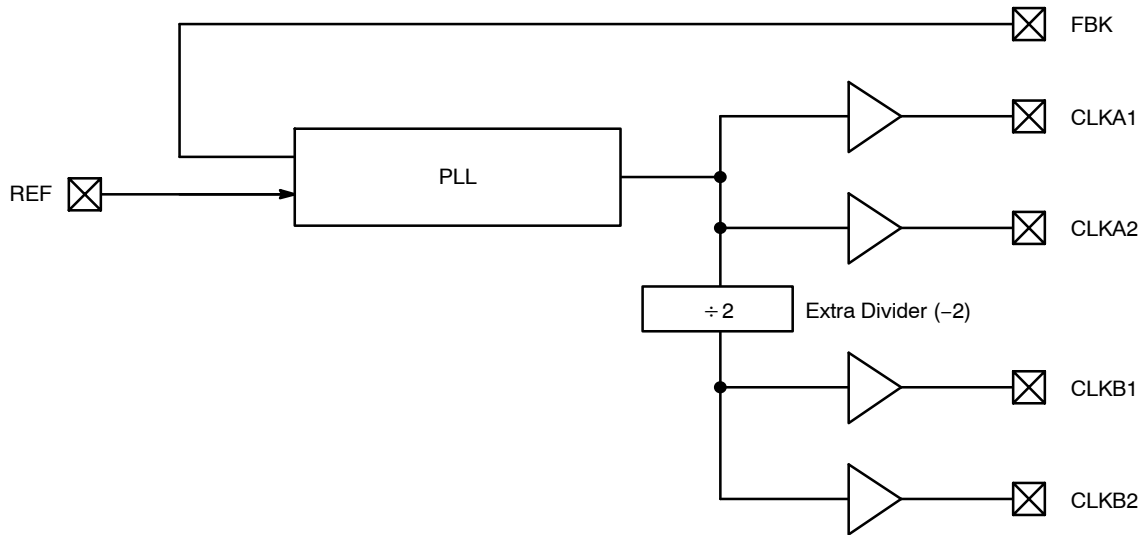
|      |                     |
|------|---------------------|
| XXXX | = Device Code       |
| A    | = Assembly Location |
| L    | = Wafer Lot         |
| Y    | = Year              |
| W    | = Work Week         |
| ▪    | = Pb-Free Package   |

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

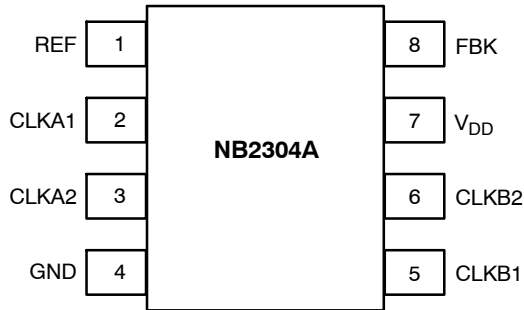
## NB2304A



**Figure 1. Basic Block Diagram**  
(see Figures 11 and 12 for device specific Block Diagrams)

**Table 1. CONFIGURATIONS**

| Device     | Feedback From    | Bank A Frequency | Bank B Frequency |
|------------|------------------|------------------|------------------|
| NB2304AI1  | Bank A or Bank B | Reference        | Reference        |
| NB2304AI1H | Bank A or Bank B | Reference        | Reference        |
| NB2304AI2  | Bank A           | Reference        | Reference ÷ 2    |
| NB2304AI2  | Bank B           | 2 X Reference    | Reference        |



**Figure 2. Pin Configuration**

**Table 2. PIN DESCRIPTION**

| Pin # | Pin Name        | Description                                    |
|-------|-----------------|------------------------------------------------|
| 1     | REF (Note 1)    | Input reference frequency, 5 V tolerant input. |
| 2     | CLKA1 (Note 2)  | Buffered clock output, Bank A.                 |
| 3     | CLKA2 (Note 2)  | Buffered clock output, Bank A.                 |
| 4     | GND             | Ground.                                        |
| 5     | CLKB1 (Note 2)  | Buffered clock output, Bank B.                 |
| 6     | CLKB2 (Note 2)  | Buffered clock output, Bank B.                 |
| 7     | V <sub>DD</sub> | 3.3 V supply.                                  |
| 8     | FBK             | PLL feedback input.                            |

1. Weak pulldown.

2. Weak pulldown on all outputs.

**Table 3. MAXIMUM RATINGS**

| Parameter                                               | Min  | Max            | Unit |
|---------------------------------------------------------|------|----------------|------|
| Supply Voltage to Ground Potential                      | -0.5 | +7.0           | V    |
| DC Input Voltage (Except REF)                           | -0.5 | $V_{DD} + 0.5$ | V    |
| DC Input Voltage (REF)                                  | -0.5 | 7              | V    |
| Storage Temperature                                     | -65  | +150           | °C   |
| Maximum Soldering Temperature (10 sec)                  |      | 260            | °C   |
| Junction Temperature                                    |      | 150            | °C   |
| Static Discharge Voltage (per MIL-STD-883, Method 3015) |      | > 2000         | V    |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 4. OPERATING CONDITIONS**

| Parameter | Description                                                             | Min      | Max      | Unit |
|-----------|-------------------------------------------------------------------------|----------|----------|------|
| $V_{DD}$  | Supply Voltage                                                          | 3.0      | 3.6      | V    |
| $T_A$     | Operating Temperature (Ambient Temperature)<br>Industrial<br>Commercial | -40<br>0 | 85<br>70 | °C   |
| $C_L$     | Load Capacitance, 15 MHz to 100 MHz                                     |          | 30       | pF   |
| $C_L$     | Load Capacitance, from 100 MHz to 133 MHz                               |          | 15       | pF   |
| $C_{IN}$  | Input Capacitance (Note 3)                                              |          | 7        | pF   |

3. Applies to both REF Clock and FBK.

**Table 5. ELECTRICAL CHARACTERISTICS**  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ 

| Parameter | Description         | Test Conditions                                                    | Min | Max   | Unit          |
|-----------|---------------------|--------------------------------------------------------------------|-----|-------|---------------|
| $V_{IL}$  | Input LOW Voltage   |                                                                    |     | 0.8   | V             |
| $V_{IH}$  | Input HIGH Voltage  |                                                                    | 2.0 |       | V             |
| $I_{IL}$  | Input LOW Current   | $V_{IN} = 0\text{ V}$                                              |     | 50.0  | $\mu\text{A}$ |
| $I_{IH}$  | Input HIGH Current  | $V_{IN} = V_{DD}$                                                  |     | 100.0 | $\mu\text{A}$ |
| $V_{OL}$  | Output LOW Voltage  | $I_{OL} = 8\text{ mA }(-1, -2)$<br>$I_{OL} = 12\text{ mA }(-1H)$   |     | 0.4   | V             |
| $V_{OH}$  | Output HIGH Voltage | $I_{OH} = -8\text{ mA }(-1, -2)$<br>$I_{OH} = -12\text{ mA }(-1H)$ | 2.4 |       | V             |
| $I_{DD}$  | Supply Current      | Unloaded outputs 100 MHz REF<br>Select inputs at $V_{DD}$ or GND   |     | 45    | mA            |
|           |                     | Unloaded outputs, 66 MHz REF (-1, -2)                              |     | 35    |               |
|           |                     | Unloaded outputs, 33 MHz REF (-1, -2)                              |     | 20    |               |

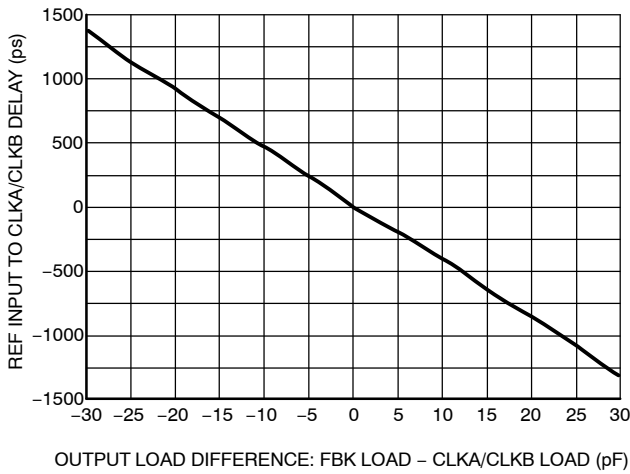
# NB2304A

**Table 6. SWITCHING CHARACTERISTICS**  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$   
(All parameters are specified with loaded outputs)

| Parameter  | Description                                       | Test Conditions                                                  | Min      | Typ  | Max          | Unit |
|------------|---------------------------------------------------|------------------------------------------------------------------|----------|------|--------------|------|
| $t_1$      | Output Frequency                                  | 30 pF load (all devices)<br>15 pF load (-1, -2)                  | 15<br>15 |      | 100<br>133.3 | MHz  |
| $t_1$      | Duty Cycle = $(t_2 / t_1) * 100$<br>(all devices) | Measured at 1.4 V, $F_{OUT} \leq 66.66\text{ MHz}$<br>30 pF load | 40.0     | 50.0 | 60.0         | %    |
|            |                                                   | Measured at 1.4 V, $F_{OUT} \leq 50\text{ MHz}$<br>15 pF load    | 45.0     | 50.0 | 55.0         |      |
| $t_3$      | Output Rise Time<br>(-1, -2)                      | Measured between 0.8 V and 2.0 V<br>30 pF load                   |          |      | 2.50         | ns   |
|            |                                                   | Measured between 0.8 V and 2.0 V<br>15 pF load                   |          |      | 1.50         |      |
|            | Output Rise Time<br>(-1H)                         | Measured between 0.8 V and 2.0 V<br>30 pF load                   |          |      | 1.50         |      |
| $t_4$      | Output Fall Time<br>(-1, -2)                      | Measured between 2.0 V and 0.8 V<br>30 pF load                   |          |      | 2.50         | ns   |
|            |                                                   | Measured between 2.0 V and 0.8 V<br>15 pF load                   |          |      | 1.50         |      |
|            | Output Fall Time<br>(-1H)                         | Measured between 2.0 V and 0.8 V<br>30 pF load                   |          |      | 1.25         |      |
| $t_5$      | Output-to-Output Skew on same Bank<br>(-1, -2)    | All outputs equally loaded                                       |          |      | 200          | ps   |
|            | Output-to-Output Skew<br>(-1H)                    | All outputs equally loaded                                       |          |      | 200          |      |
|            | Output Bank A-to-Output Bank B skew<br>(-1)       | All outputs equally loaded                                       |          |      | 200          |      |
|            | Output Bank A-to-Output Bank B skew<br>(-2)       | All outputs equally loaded                                       |          |      | 400          |      |
| $t_6$      | Delay, REF Rising Edge to FBK Rising Edge         | Measured at $V_{DD}/2$                                           |          | 0    | $\pm 250$    | ps   |
| $t_7$      | Device-to-Device Skew                             | Measured at $V_{DD}/2$ on the FBK pins of the device             |          | 0    | 500          | ps   |
| $t_8$      | Output Slew Rate                                  | Measured between 0.8 V and 2.0 V using Test Circuit #2           | 1        |      |              | V/ns |
| $t_J$      | Cycle-to-Cycle Jitter<br>(-1, -1H)                | Measured at 66.67 MHz, loaded outputs,<br>15 pF load             |          |      | 180          | ps   |
|            |                                                   | Measured at 66.67 MHz, loaded outputs,<br>30 pF load             |          |      | 200          |      |
|            |                                                   | Measured at 133.3 MHz, loaded outputs,<br>15 pF load             |          |      | 100          |      |
|            | Cycle-to-Cycle Jitter<br>(-2)                     | Measured at 66.67 MHz, loaded outputs,<br>30 pF load             |          |      | 400          | ps   |
|            |                                                   | Measured at 66.67 MHz, loaded outputs,<br>15 pF load             |          |      | 380          |      |
| $t_{LOCK}$ | PLL Lock Time                                     | Stable power supply, valid clock presented on REF and FBK pins   |          |      | 1.0          | ms   |

### Zero Delay and Skew Control

For applications requiring zero input-output delay, all outputs must be equally loaded.

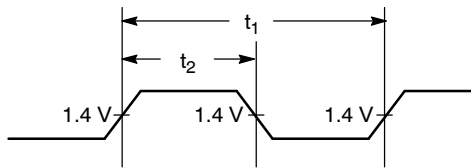


**Figure 3. REF Input to CLKA/CLKB Delay vs. Difference in Loading between FBK Pin and CLKA/CLKB Pins**

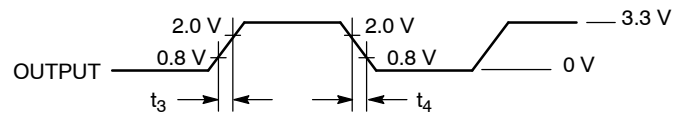
To close the feedback loop of the NB2304A, the FBK pin can be driven from any of the four available output pins. The output driving the FBK pin will be driving a total load of 7 pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input output delay. This is shown in Figure 3.

For applications requiring zero input-output delay, all outputs including the one providing feedback should be equally loaded. If input-output delay adjustments are required, use Figure 3 to calculate loading differences between the feedback output and remaining outputs. For zero output-output skew, be sure to load outputs equally.

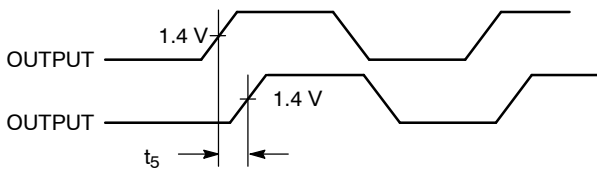
### SWITCHING WAVEFORMS



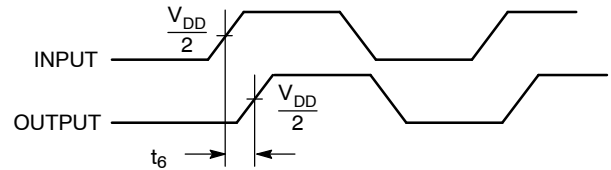
**Figure 4. Duty Cycle Timing**



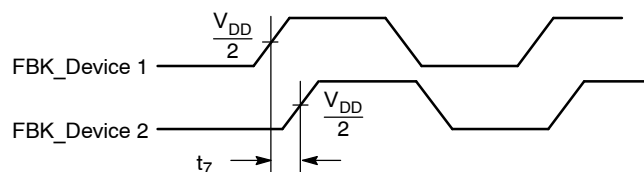
**Figure 5. All Outputs Rise/Fall Time**



**Figure 6. Output - Output Skew**



**Figure 7. Input - Output Propagation Delay**



**Figure 8. Device - Device Skew**

# NB2304A

## TEST CIRCUITS

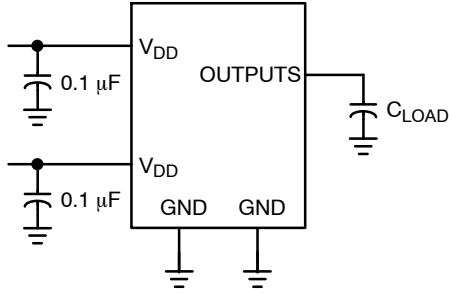


Figure 9. Test Circuit #1

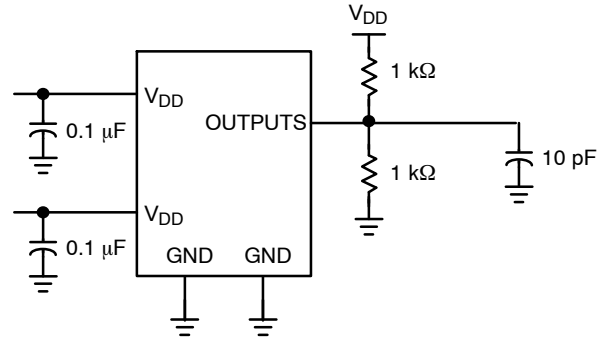


Figure 10. Test Circuit #2  
For parameter  $t_b$  (output slew rate) on -1H devices

## BLOCK DIAGRAMS

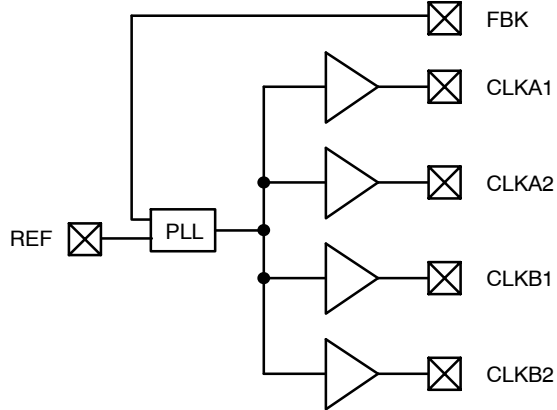


Figure 11. NB2304AI1 and NB2304AI1H

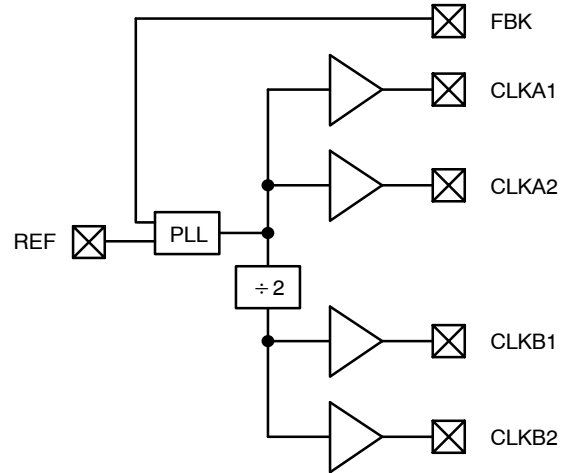


Figure 12. NB2304AI2

## ORDERING INFORMATION

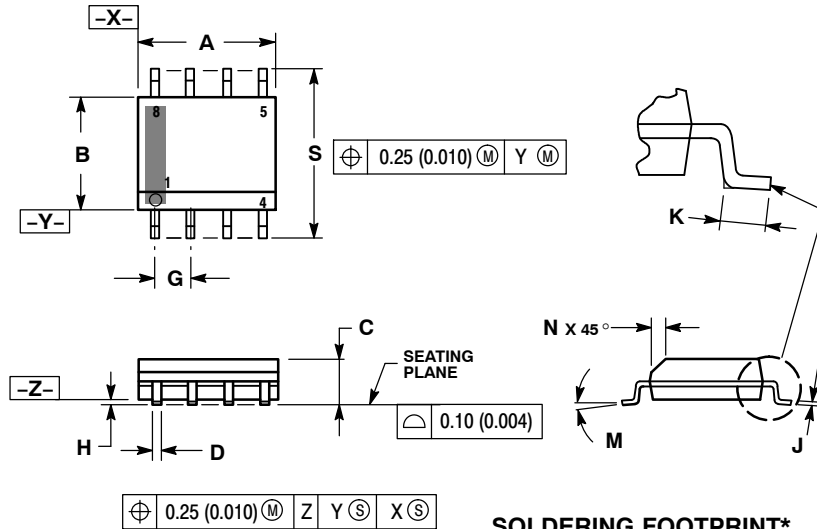
| Device         | Marking | Operating Range         | Package          | Shipping <sup>†</sup> | Availability |
|----------------|---------|-------------------------|------------------|-----------------------|--------------|
| NB2304AI1DG    | 4I1     | Industrial & Commercial | SOIC-8 (Pb-Free) | 98 Units / Rail       | Now          |
| NB2304AI1DR2G  | 4I1     | Industrial & Commercial | SOIC-8 (Pb-Free) | 2500 Tape & Reel      | Now          |
| NB2304AI1HDG   | 4I1H    | Industrial & Commercial | SOIC-8 (Pb-Free) | 98 Units / Rail       | Now          |
| NB2304AI1HDR2G | 4I1H    | Industrial & Commercial | SOIC-8 (Pb-Free) | 2500 Tape & Reel      | Now          |
| NB2304AI2DG    | 4I2     | Industrial & Commercial | SOIC-8 (Pb-Free) | 98 Units / Rail       | Now          |
| NB2304AI2DR2G  | 4I2     | Industrial & Commercial | SOIC-8 (Pb-Free) | 2500 Tape & Reel      | Now          |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NB2304A

## PACKAGE DIMENSIONS

### SOIC-8 NB CASE 751-07 ISSUE AJ

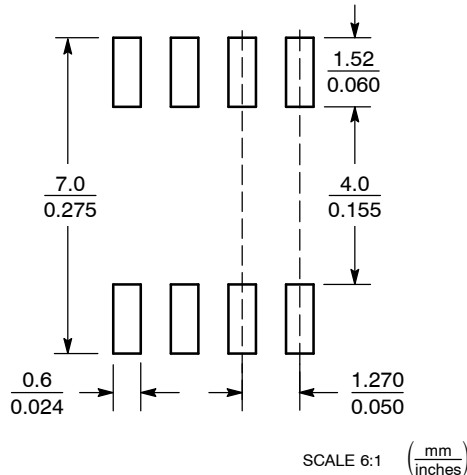


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

#### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Licensed under US patent Nos 5,488,627, 6,646,463 and 5,631,920.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative