Rev 0; 4/06

Dual, 64-Position Nonvolatile Digital Potentiometer with Buffered Outputs

General Description

The DS3908 contains two nonvolatile digital potentiometers with programmable-gain amplifiers buffering the wiper outputs. The potentiometer position and amplifier gain are controlled through an I²C-compatible serial bus. The DS3908 operates in both 3.3V and 5V systems and features a write-protect pin that locks the position of the potentiometers and gain registers. Up to eight DS3908s can be placed on a single I²C bus.

Features

- **Two 64-Position Linear Taper Potentiometers**
- **Integral Wiper Buffering Amplifiers with Selectable Gains of 1V/V, 2V/V, or 4V/V**
- **100kΩ Potentiometer End-to-End Resistance**
- **Low Potentiometer Temperature Coefficient**
- **Nonvolatile Wiper and Gain Storage**
- **I²C-Compatible Interface**
- **Write-Protect Pin Prevents Accidental Field Reprogramming**
- **3V to 5.5V Supply Voltage Range**
- **-40°C to +85°C Operating Temperature Range**
- **14-Pin TDFN Package**

Applications

Pin-Diode Biasing

Power-Supply Calibration

Cell Phones and PDAs

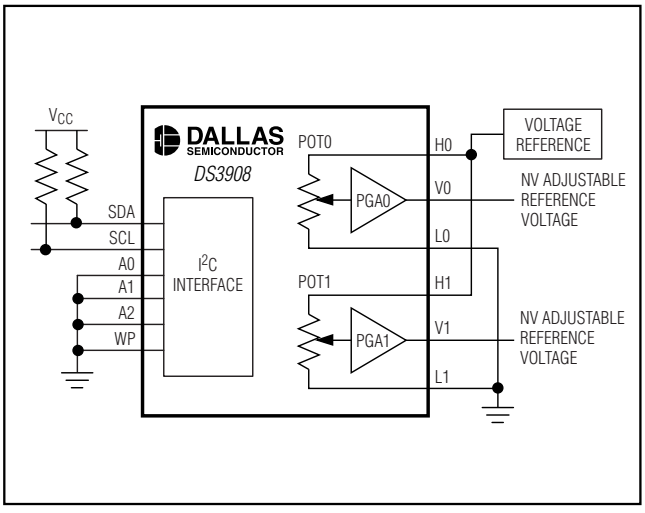
Portable Electronics

Ordering Information

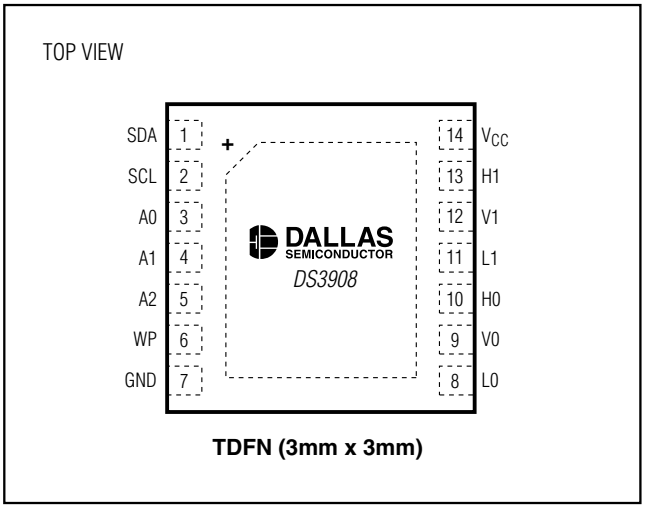
PART	TEMP RANGE	PIN-PACKAGE
DS3908N+	-40°C to +85°C	14 TDFN

+Denotes lead-free package.

Typical Operating Circuit



Pin Configuration



TDFN (3mm x 3mm)

Dual, 64-Position Nonvolatile Digital Potentiometer with Buffered Outputs

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC}, SDA, and SCL Relative to GND .....-0.5V to +6.0V
Voltage on A0, A1, A2, L0, L1, H0, H1, and WP Relative to GND.....-0.5V to (V_{CC} + 0.5V) (not to exceed +6.0V)
Operating Temperature Range .....-40°C to +85°C
Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....Refer to J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	+3.0		+5.5	V
Input Logic 1 (SCL, SDA, A0, A1, A2, WP)	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0 (SCL, SDA, A0, A1, A2, WP)	V_{IL}		-0.3		0.3 x V_{CC}	V
Potentiometer Voltage (L0, L1, H0, H1)		V_{CC} = +3.0V to +5.5V	-0.3		V_{CC} + 0.3V	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage	I_L		-1		+1	µA
Standby Supply Current	I_{STBY}	V_{CC} = 5.5V (Note 2)			2	mA
Low-Level Output Voltage (SDA)	V_{OL1}	3mA sink current	0		0.4	V
	V_{OL2}	6mA sink current	0		0.6	
I/O Capacitance	$C_{I/O}$				10	pF
WP Internal Pullup Resistance	R_{WP}		40	65	100	kΩ

ANALOG POTENTIOMETER CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
End-to-End Resistance		+25°C	79	100	121	kΩ
Absolute Linearity	INL	(Notes 3, 4)	-0.6		+0.6	LSB
Relative Linearity	DNL	(Notes 4, 5)	-0.25		+0.25	LSB
End-to-End Temperature Coefficient				50		ppm/°C

PROGRAMMABLE-GAIN AMPLIFIER CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Input Voltage	CMV_{IN}		0		V_{CC} - 1.5	V
Gain	G	$R_L \geq 2k\Omega$, G = 1V/V	0.975	1	1.025	V/V
		$R_L \geq 2k\Omega$, G = 2V/V	1.925	2	2.05	
		$R_L \geq 2k\Omega$, G = 4V/V	3.850	4	4.10	
Output Voltage Range	V_{OUT}	$R_L = 2k\Omega$, -1mA < I_{OUT} < 1mA	0.3		V_{CC} - 0.3	V
Power-Supply Rejection Ratio	PSRR		60	90		dB
Output Source Current	$I_{OUT:SOURCE}$	V_{OUT} = 0V, Hx = Lx = 1V			-15	mA
Output Sink Current	$I_{OUT:SINK}$	V_{OUT} = 1V, Hx = Lx = 0V	15			mA
Unity-Gain Frequency	f_T	Gain = 1V/V, position 3Fh		3.5		MHz
Amplifier Capacitive Loading	C_L				100	pF
Input Offset Voltage	V_{OS}		-9		+9	mV
Load Regulation		-1mA < I_{OUT} < 1mA		800	2200	µV/mA
Output-Voltage Slew Rate		R_L = 10kΩ, C_L = 10pF	270		840	V/ms

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V, T_A = -40°C to +85°C.) (See Figure 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 6)			400	kHz
Bus Free Time between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Start Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 7)	20 + 0.1C_B		300	ns
SDA and SCL Fall Time	t_F	(Note 7)	20 + 0.1C_B		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitance	C_B	(Note 7)			400	pF
EEPROM Write Time	t_W	(Note 8)		10	17	ms
Startup Time	t_{ST}	V_{CC} = 3.0V			40	µs

Dual, 64-Position Nonvolatile Digital Potentiometer with Buffered Outputs

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
EEPROM Write Cycles		At +70°C	50,000		

Note 1: All voltages are referenced to ground.

Note 2: I_{STBY} specified assuming control pins are connected as follows: WP must be disconnected or connected high. H terminal connected to V_{CC}, L terminal connected to GND, potentiometer position 1Dh, PGA is at 2V/V, A0 to A2 connected to V_{CC}, SDA and SCL connected to V_{CC}, with no load.

Note 3: Absolute linearity is used to measure expected wiper voltage as determined by wiper position in a voltage-divider configuration.

Note 4: This specification only refers to the potentiometers, and does not include the gain and offset error due to the PGA.

Note 5: Relative linearity is used to determine the change of wiper voltage between two adjacent wiper positions in a voltage-divider configuration.

Note 6: I^2C interface timing shown is for fast-mode (400kHz) operation. This device is also backward-compatible with I^2C standard-mode timing.

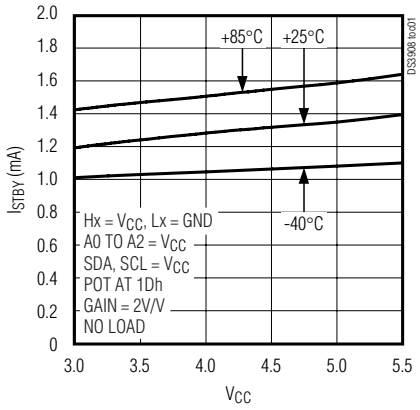
Note 7: C_B—total capacitance of one bus line in picofarads, timing referenced to 0.9 x V_{CC} and 0.1 x V_{CC}.

Note 8: EEPROM write begins after a stop condition occurs.

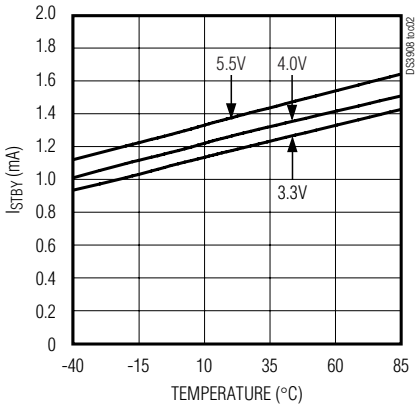
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

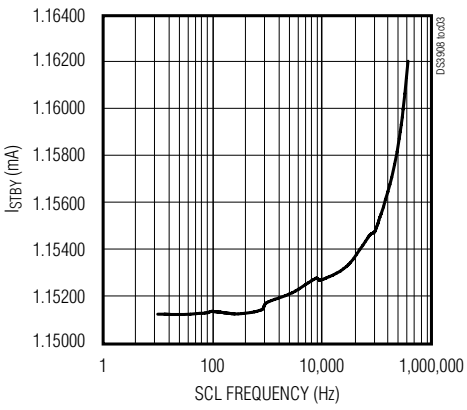
STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE



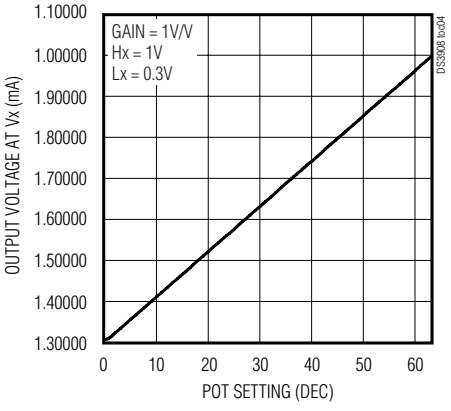
STANDBY SUPPLY CURRENT vs. TEMPERATURE



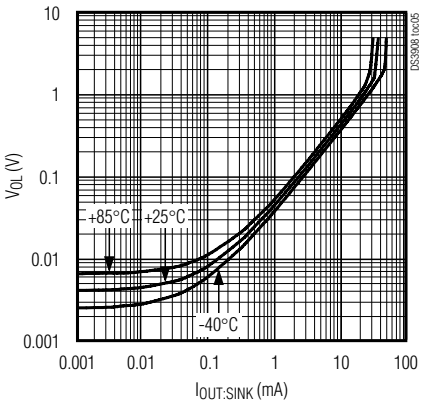
STANDBY SUPPLY CURRENT vs. SCL FREQUENCY



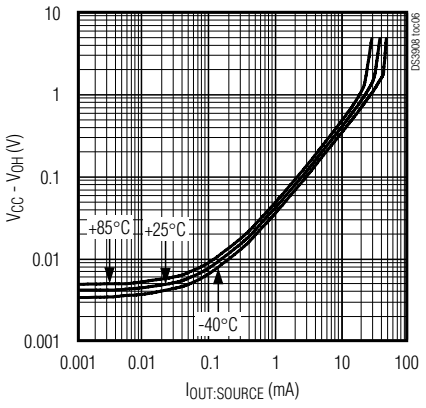
OUTPUT VOLTAGE vs. POT SETTING



VOL vs. IOUT:SINK



VCC - VOH vs. IOUT:SOURCE

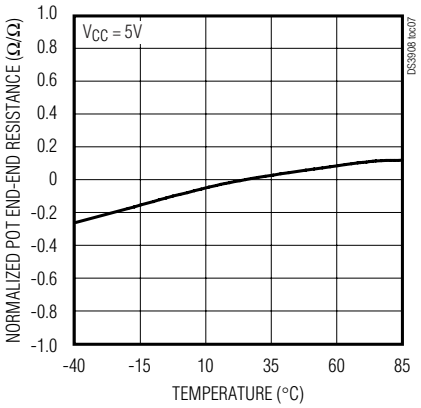


Dual, 64-Position Nonvolatile Digital Potentiometer with Buffered Outputs

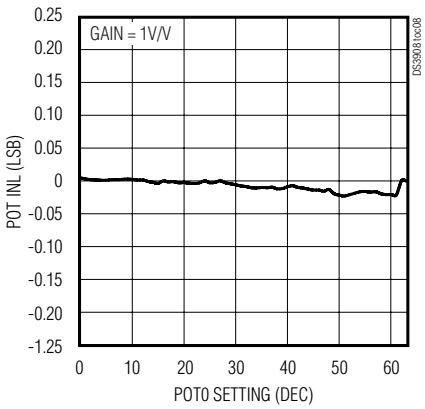
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

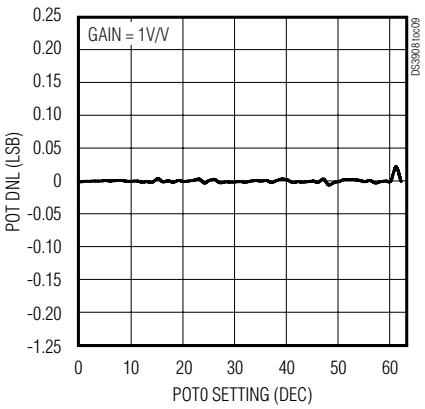
NORMALIZED POT END-END RESISTANCE vs. TEMPERATURE



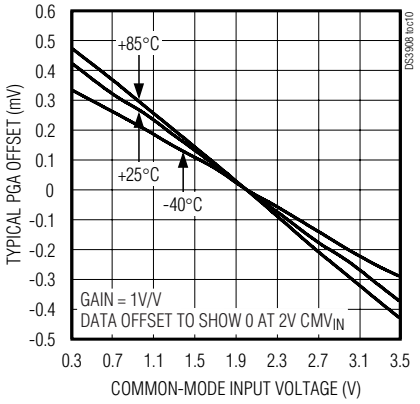
POT INL vs. SETTING



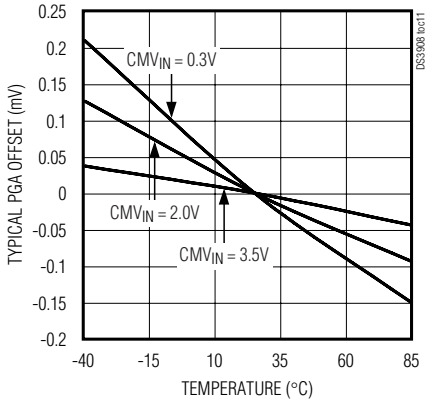
POT DNL vs. SETTING



TYPICAL PGA OFFSET vs. COMMON-MODE INPUT VOLTAGE



TYPICAL PGA OFFSET vs. TEMPERATURE

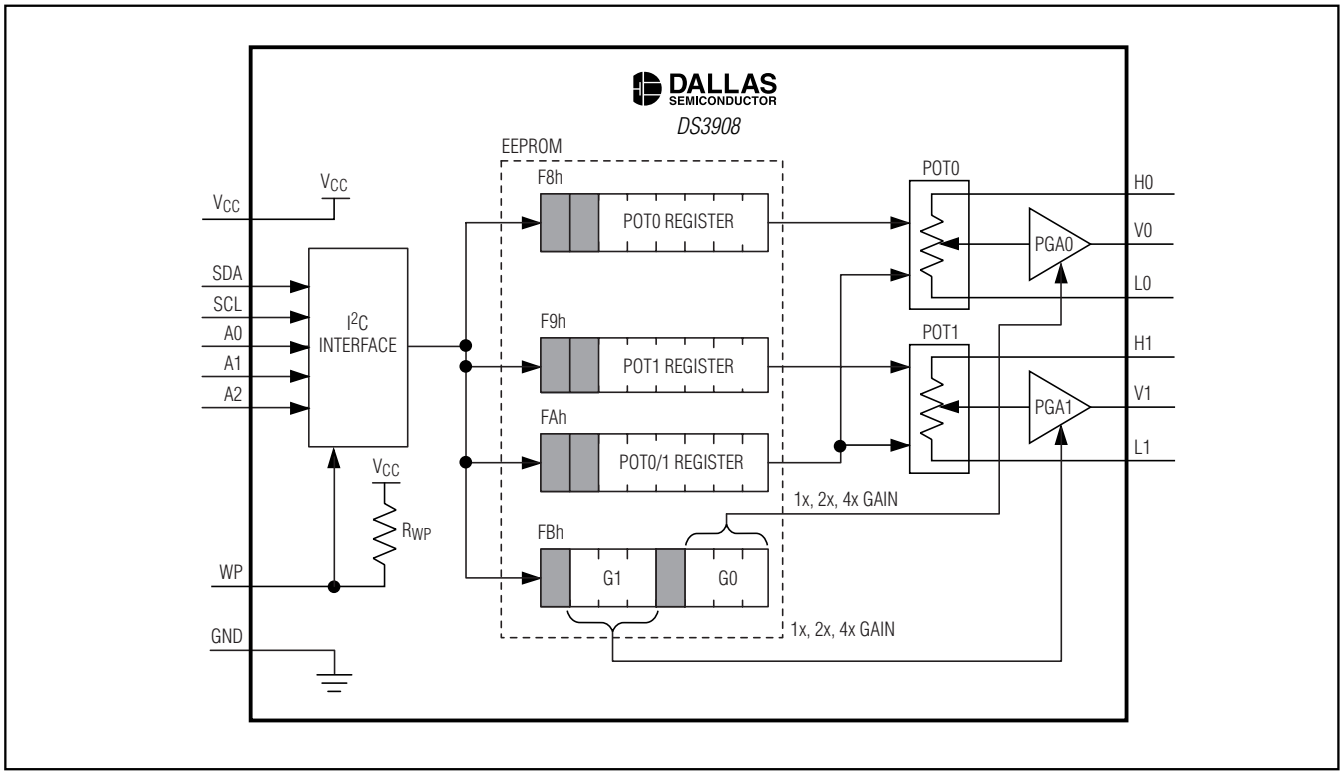


Pin Description

TDFN PIN	NAME	FUNCTION
1	SDA	I²C Serial Data. Input/output for I²C data.
2	SCL	I²C Serial Clock. Input for I²C clock.
3, 4, 5	A0, A1, A2	Address-Select Inputs. Determines I²C address. Device address is $1010A_2A_1A_0$. (See the *I²C Slave Address and Address Pins* section for more details.)
6	WP	Write-Protect Input. Must be grounded to write to the registers. An internal pullup will lock the register values if this pin is not connected.
7	GND	Ground Terminal
8, 11	L0, L1	Potentiometer Low Terminals. Voltages on these pins should remain between GND and V_{CC}.
9, 12	V0, V1	Amplifier Outputs
10, 13	H0, H1	Potentiometer High Terminals. Voltages on these pins should remain between GND and V_{CC}.
14	V_{CC}	Supply Voltage Terminal

Dual, 64-Position Nonvolatile Digital Potentiometer with Buffered Outputs

Functional Diagram



Detailed Description

The DS3908 contains two nonvolatile digital potentiometers with programmable-gain amplifiers buffering the wiper outputs.

The potentiometers have 63 equally weighted (linear-taper) resistive elements, for a total of 64 taps. The resistive elements are built using a low-temperature-drift material, and have a typical 100kΩ end-to-end resistance. This produces an output that is highly linear, with the highest and lowest taps connected to high (Hx) and low (Lx) terminals, respectively. The potentiometers are independently controlled using an I²C-compatible interface. Three address pins allow one of eight slave addresses to be selected. The eight slave addresses allow the DS3908 address to be customized for applications with multiple I²C devices, and allow up to eight DS3908s to be placed on the same I²C bus. The potentiometer positions are saved in EEPROM, and are recalled during each power-up to provide nonvolatile position settings. Once the settings are written, the write-protect pin prevents accidental writes to the potentiometers. The write-protection function is ideal for analog factory calibration because it prevents errant transactions on the I²C bus from corrupting the settings of the device. The WP pin contains an internal pullup resistor that must be pulled low to write to the device.

The programmable-gain amplifiers can be independently set to one of three different gains—1V/V, 2V/V, or 4V/V. The amplifiers' common-mode input range is from ground to 1.5V below V_{CC}, and the output is rail-to-rail and capable of driving 1mA loads, 300mV from each supply rail. The outputs are stable driving 100pF loads for applications that require output filtering.

The addition of the amplifier to buffer the potentiometer wiper offers distinct advantages over standard digital potentiometers. The buffer provides a high-impedance load for the potentiometer and a low-impedance voltage output. This improves the linearity of the output voltage for systems that load the potentiometer by eliminating the changes in current through both the potentiometer and the wiper impedance. It also allows voltage gain from the potentiometer input to the output. Because the amplifiers are integrated into the DS3908, this is done without increasing the footprint of the design or the complexity of the PC board.

I²C Slave Address and Address Pins

The DS3908's I²C slave address is determined by the state of the A0, A1, and A2 address pins as shown in the pin configuration (see Figure 1). Address pins connected to GND result in a '0' in the corresponding bit position in the slave address. Conversely, address pins connected to V_{CC} result in a '1' in the corresponding bit positions. I²C communication is described in detail in the *I²C Serial Interface Description* section.

Potentiometer Control

The potentiometers of the DS3908 have 64 taps with 63 resistive elements separating them. Thus, the most and least significant wiper positions connect the amplifier to the voltages at the high and low terminals of the potentiometer, respectively.

The potentiometers of the DS3908 are controlled by communicating with the following registers:

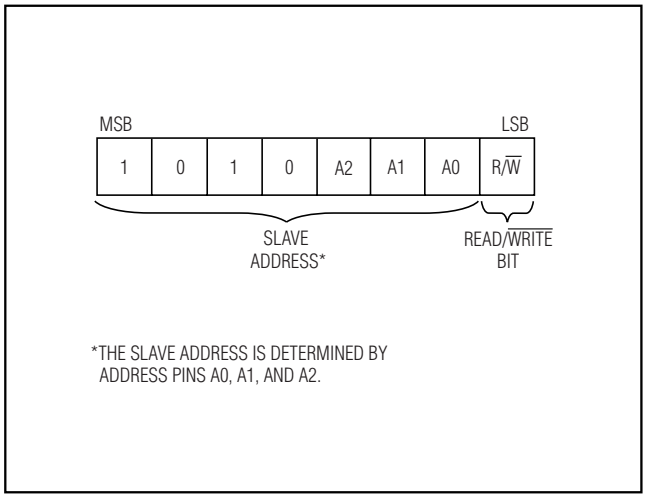


Figure 1. DS3908 Slave Address Byte

Table 1. Potentiometer Registers

ADDRESS	POTENTIOMETER	I²C FUNCTIONS	NUMBER OF POSITIONS*	DEFAULTS
F8h	Pot 0	Read/Write	64 (00h to 3Fh)	1Fh
F9h	Pot 1	Read/Write	64 (00h to 3Fh)	1Fh
FAh	Pot 0 and Pot 1	Write Only	64 (00h to 3Fh)	—

**The two most significant bits of each potentiometer position register are ignored. Writing values greater than 3Fh to any of the potentiometer registers will result in a valid 6-bit position, without regard to the value of the most significant two bits. Example: Register values C2h, 82h, 42h, and 02h are all potentiometer position 2.*

Dual, 64-Position Nonvolatile Digital Potentiometer with Buffered Outputs

When writing to the DS3908, the potentiometer will adjust to the new setting once it has acknowledged the new data that is being written, and the EEPROM (used to make the setting nonvolatile) will be written following the stop condition at the end of the write command. To change the setting without changing the EEPROM, terminate the write with a repeated start condition before the next stop condition occurs. Using a repeated start condition prevents the 20ms (maximum) delay required for the EEPROM write cycle to finish.

Programmable Amplifier Control

The gain of both DS3908 amplifiers is controlled by writing to register address FBh. The most significant nibble of the FBh address controls the PGA1 gain, and the least significant nibble controls the PGA0 gain. The format of each nibble is shown in the tables below:

Table 2. Programmable Amplifier Register

ADDRESS	REGISTER FORMAT (BINARY)							
	PGA1				PGA0			
FBh	R*	$G1_2$	$G1_1$	$G1_0$	R*	$G0_2$	$G0_1$	$G0_0$
	bit7							bit0

Default value = 11h.
**Reserved for future use, write to zeros.*

Table 3. Programmable Amplifier Gain Codes

$Gx_2Gx_1Gx_0$	AMPLIFIER GAIN (V/V)
00X	1
01X	2
1XX	4

X = Don't care.

Writes to this register are similar to writes to the potentiometer register. A stop condition must follow the write to ensure that the EEPROM is modified. A repeated start condition before a stop condition following a write operation will prevent the settings from being stored in EEPROM. (See the *I^2C Communication* section for more details.)

Write Protection

The write-protect pin has an internal pullup resistor. To adjust the potentiometers' position, this pin must be grounded. This pin can be left floating or connected to V_{CC} to write protect the EEPROM memory. All registers can be read when the device is write protected.

I²C Serial Interface Description

I²C Definitions

The following terminology is commonly used to describe I²C data transfers:

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses, and start and stop conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or not Busy: Time between stop and start conditions when both SDA and SCL are inactive and in their logic-high states. When the bus is idle it often initiates a low-power mode for slave devices.

Start Condition: A start condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a start condition. See the timing diagram for applicable timing.

Stop Condition: A stop condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a stop condition. See the timing diagram for applicable timing.

Repeated Start Condition: The master can use a repeated start condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated starts are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated start condition is issued identically to a normal start condition. See the timing diagram for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold-time requirements (see Figure 2). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time (see Figure 2) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An Acknowledgement (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing (Figure 2) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

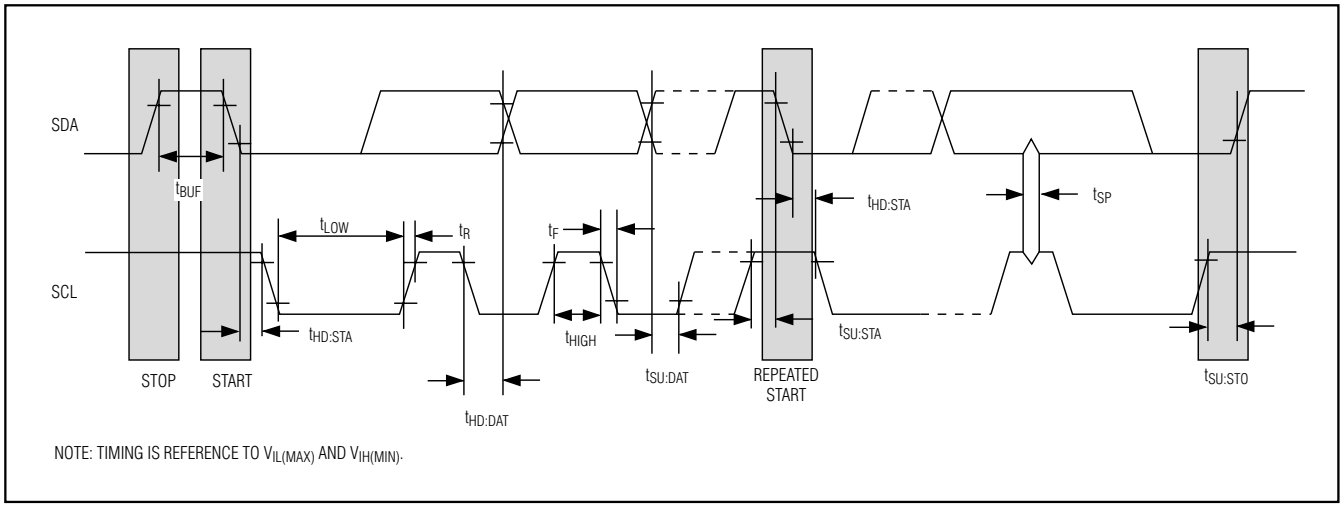


Figure 2. I²C Timing Diagram

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Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition above, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminated communication so the slave will return control of SDA to the master.

Slave Address Byte: Each slave on the I^2C bus responds to a slave address byte sent immediately following a start condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The DS3908's slave address is determined by the state of the A0, A1, and A2 address pins as shown in Figure 1. Address pins connected to GND result in a '0' in the corresponding bit position in the slave address. Conversely, address pins connected to V_{CC} result in a '1' in the corresponding bit positions.

When the R/$\overline{W}$ bit is 0 (such as in A0h), the master is indicating it will write data to the slave. If R/$\overline{W}$ = 1, (A1h in this case), the master is indicating it wants to read from the slave.

If an incorrect slave address is written, the DS3908 will assume the master is communicating with another I^2C device and ignore the communication until the next start condition is sent.

Memory Address: During an I^2C write operation to the DS3908, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I^2C Communication

Writing a Single Byte to a Slave: The master must generate a start condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a stop condition. The master must read the slave's acknowledgement during all byte write operations.

When writing to the DS3908, the potentiometer will adjust to the new setting once it has acknowledged the new data that is being written, and the EEPROM (used to make the setting nonvolatile) will be written following the stop condition at the end of the write command. To change the setting without changing the EEPROM, terminate the write with a repeated start condition before the next stop condition occurs. Using a repeated start condition prevents the 20ms (maximum) delay required for the EEPROM write cycle to finish.

If the master continues to write data to the DS3908, without generating a stop condition, then the same register will be overwritten.

Acknowledge Polling: Any time an EEPROM byte is written, the DS3908 requires the EEPROM write time (t_W) after the stop condition to write the contents of the byte to EEPROM. During the EEPROM write time, the device will not acknowledge its slave address because it is busy. It is possible to take advantage of this phenomenon by repeatedly addressing the DS3908, which allows communication to continue as soon as the DS3908 is ready. The alternative to acknowledge polling is to wait for a maximum period of t_W to elapse before attempting to access the device.

EEPROM Write Cycles: The DS3908's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table. The specification shown is at the worst-case temperature. It is capable of handling many additional writes at room temperature.

Reading a Single Byte from a Slave: Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address pointer. To read a single byte from the slave, the master generates a start condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a stop condition.

Manipulating the Address Pointer for Reads: A dummy write cycle can be used to force the address pointer to a particular value. To do this, the master generates a start condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated start condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a stop condition.

See Figure 3 for a read example using the repeated start condition to specify the memory location.

Applications Information

Power-Supply Decoupling

To achieve the best results when using the DS3908, decouple the power supply with a 0.01µF or 0.1µF capacitor. Use a high-quality, ceramic, surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

Dual, 64-Position Nonvolatile Digital Potentiometer with Buffered Outputs

Total Error

The total error in a reading from the DS3908 can be calculated using the following formula:

$PotVoltage = (PotCode / 63) \times (V_H - V_L) + V_L$

$Error_{POT} = (INL_{ERR} / 63) \times (V_H - V_L)$

$Error_{OFFSET} = Gain \times V_{OFF}$

$Error_{GAIN} = PotVoltage \times Gain_{ERR}$

$Total\ Output\ Error = Error_{POT} + Error_{OFFSET} + Error_{GAIN}$

where:

PotCode = Potentiometer Setting (dec)

$Gain_{ERR}$ = Amplifier Gain Deviation from Desired (V/V)

V_{OFF} = PGA Input Voltage Offset Voltage (V)

INL_{ERR} = Potentiometer Integral Non-Linearity (LSB)

For example, the worst-case error for V_H = 2V, V_L = 0.5V, PGA Gain = 2V/V, PotCode = 31d (1Fh), is given by:

$PotVoltage = 31 / 63 \times (2.0V - 0.5V) + 0.5V = 1.238V$

$Error_{POT} = (0.6 / 63) \times (2.0V - 0.5V) = 0.014V$

$Error_{OFFSET} = 2.0V/V \times 9mV = 0.018V$

$Error_{GAIN} = PotVoltage \times Gain_{ERR} = 0.0929V$

$Total\ Output\ Error = Error_{POT} + Error_{OFFSET} + Error_{GAIN}$

$= 0.014V + 0.018V + 0.0929V = 0.125V$

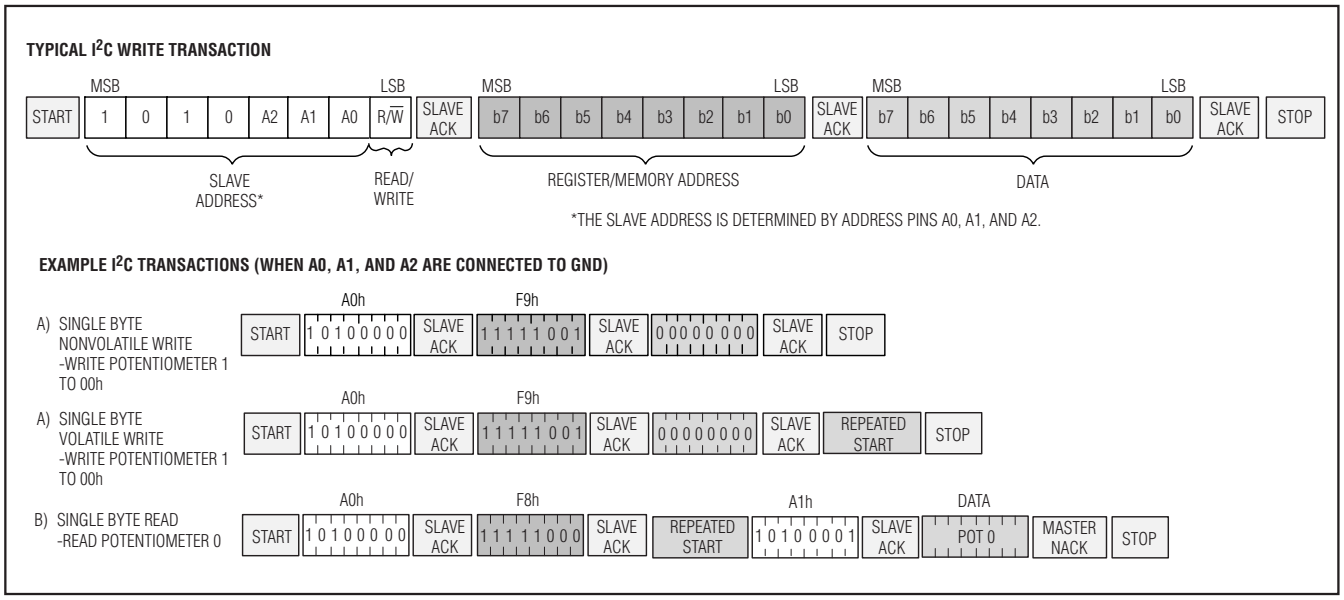

Figure 3. I²C Communication Examples

Chip Topology

TRANSISTOR COUNT: 9950

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.