

## ULTRA LOW CAPACITANCE TVS ARRAY

### APPLICATIONS

- ✓ Sensor & Control Circuits
- ✓ FireWire
- ✓ Ethernet - 10/100/1000 Base T
- ✓ Handheld Electronics
- ✓ RF Applications

### IEC COMPATIBILITY (EN61000-4)

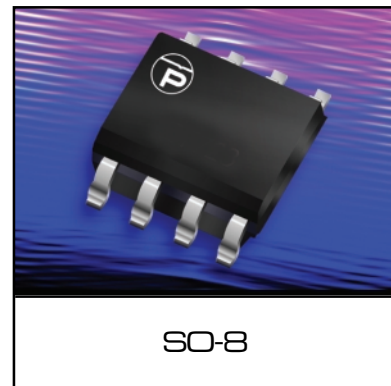
- ✓ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
- ✓ 61000-4-4 (EFT): 40A - 5/50ns
- ✓ 61000-4-5 (Surge): 24A, 8/20 $\mu$ s - Level 2(Line-Ground) & Level 3(Line-Line)

### FEATURES

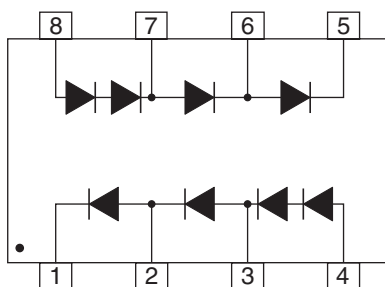
- ✓ 500 Watts Peak Pulse Power per Line ( $t_p = 8/20\mu$ s)
- ✓ Bidirectional Configuration
- ✓ ESD Protection > 40 kilovolts
- ✓ Low Clamping Voltage < 5 Volts
- ✓ **ULTRA LOW CAPACITANCE: 1.25pF**

### MECHANICAL CHARACTERISTICS

- ✓ Molded JEDEC SO-8
- ✓ Weight 0.6 grams (Approximate)
- ✓ Flammability rating UL 94V-0
- ✓ 12mm Tape and Reel Per EIA Standard 481
- ✓ Device Marking: Marking Code, Logo, Date Code & Pin One Defined By DOT on Package



### PIN CONFIGURATION



## DEVICE CHARACTERISTICS

MAXIMUM RATINGS @ 25°C Unless Otherwise Specified			
PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power - $t_p = 8/20\mu s$ (See Figure 1)	$P_{PP}$	500	W
Operating Temperature	$T_J$	-55°C to 150°C	°C
Storage Temperature	$T_{STG}$	-55°C to 150°C	°C

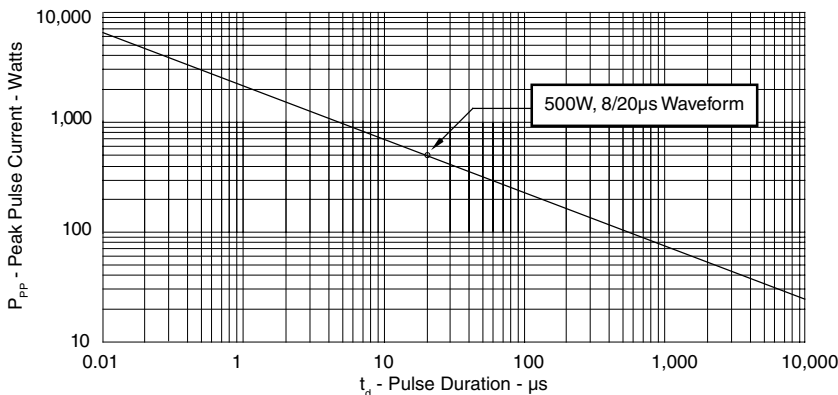
ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified								
PART NUMBER	DEVICE MARKING CODE	RATED STAND-OFF VOLTAGE	MINIMUM BREAKDOWN VOLTAGE (See Note 1)	MAXIMUM REVERSE LEAKAGE CURRENT (See Note 1)	MAXIMUM CLAMPING VOLTAGE (See Note 1) (See Fig. 2)	WORKING INVERSE BLOCKING VOLTAGE (See Note 2)	INVERSE BLOCKING LEAKAGE CURRENT (See Note 2)	MAXIMUM CAPACITANCE (See Note 3)
		$V_{WM}$ VOLTS	@1mA $V_{(BR)}$ VOLTS	@ $V_{WM}$ $I_D$ $\mu A$	@8/20 $\mu s$ $V_C @ I_{PP}$	$V_{WB}$ VOLTS	@ $V_{WB} I_R$ $\mu A$	@0V, 1MHz C pF
PLC496	VEC	1.0	2.5	20	12.5V @ 30A	75	1.0	1.25

**Note 1:** Apply positive voltage from pin 4 to 1 and pin 8 to 5.

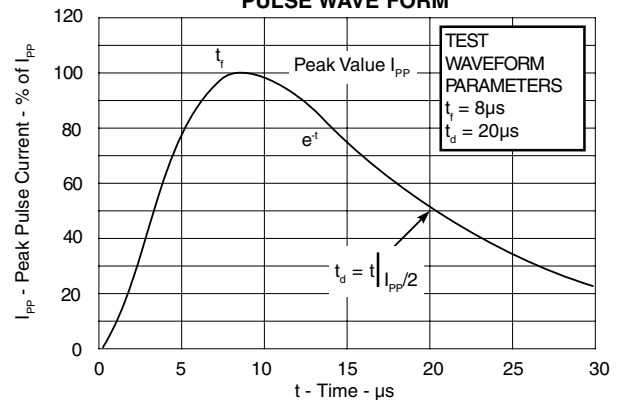
**Note 2:** Apply positive voltage from pin 1 to 4 and pin 5 to 8.

**Note 3:** Capacitance from pin 1 to 4 < 1.25pF. Capacitance from pin 8 to 5 < 1.25pF.

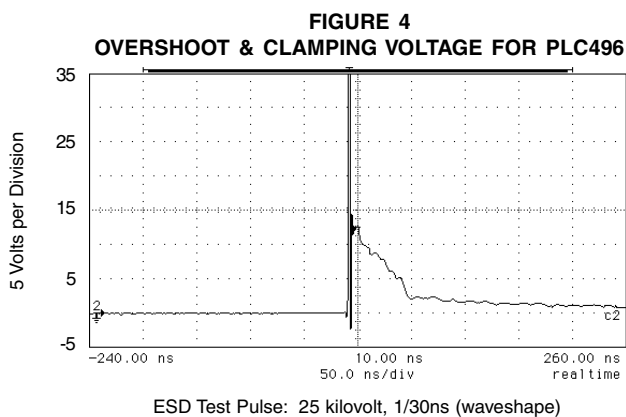
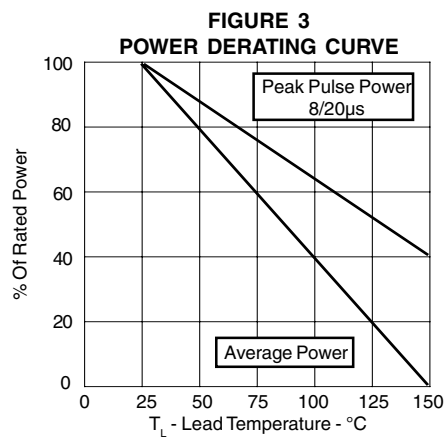
**FIGURE 1**  
PEAK PULSE POWER VS PULSE TIME



**FIGURE 2**  
PULSE WAVE FORM



## GRAPHS



## APPLICATION NOTE

The PLC496 is an ultra low capacitance, bidirectional array that is designed to protect I/O or high speed data lines from the damaging effects of ESD or EFT. This product has a surge capability of 500 Watts  $P_{PP}$  per line for an 8/20 $\mu$ s waveshape and offers ESD protection > 40kV.

### DIFFERENTIAL-MODE CONFIGURATION (Figure 1)

The PLC496 is designed to protect one bidirectional line where the normal signal voltage is both positive and negative. Figure 1 shows a typical differential-mode (line to line) I/O port protection circuit application.

Circuit connectivity is as follows:

- ✓ Pins 1, 4, 5 and 8 are connected to the data lines
- ✓ Pins 2, 3, 7 and 6 are not connected.

### COMMON-MODE CONFIGURATION (Figure 2)

The PLC496 can provide protection for sensor circuit applications. Figure 2, is a typical common-mode (line to ground) sensor circuit application.

Circuit connectivity is as follows:

- ✓ Pins 1 and 8 connected to the dataline
- ✓ Pins 4 and 5 connected to ground
- ✓ Pins 2, 3, 6, and 7 are not connected

### CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✓ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✓ The path length between the TVS device and the protected line should be minimized.
- ✓ All conductive loops including power and ground loops should be minimized.
- ✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✓ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

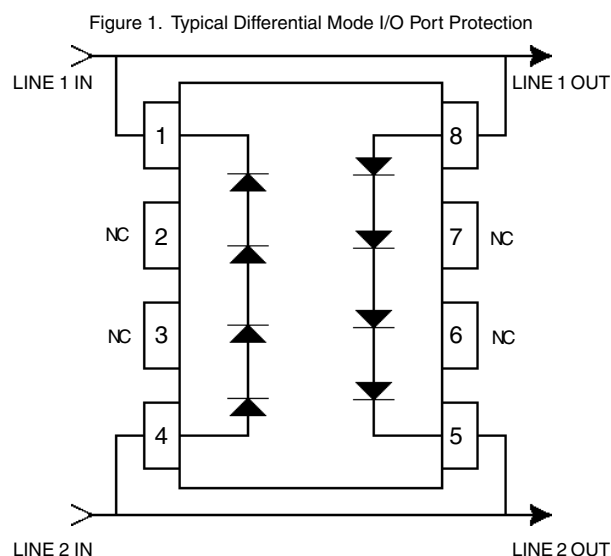
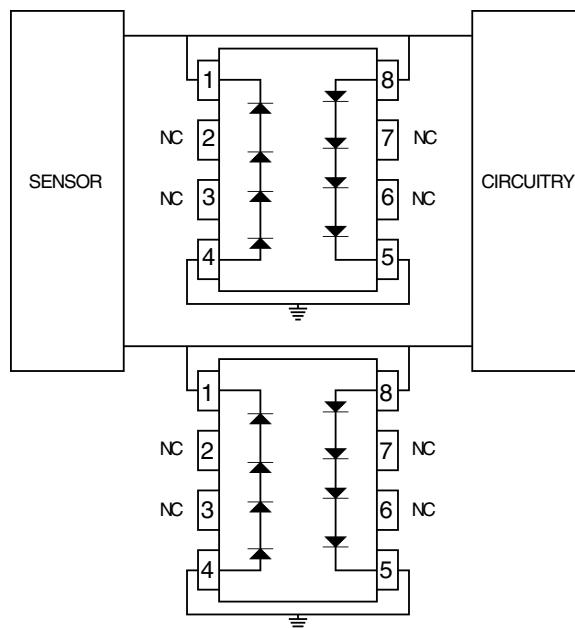
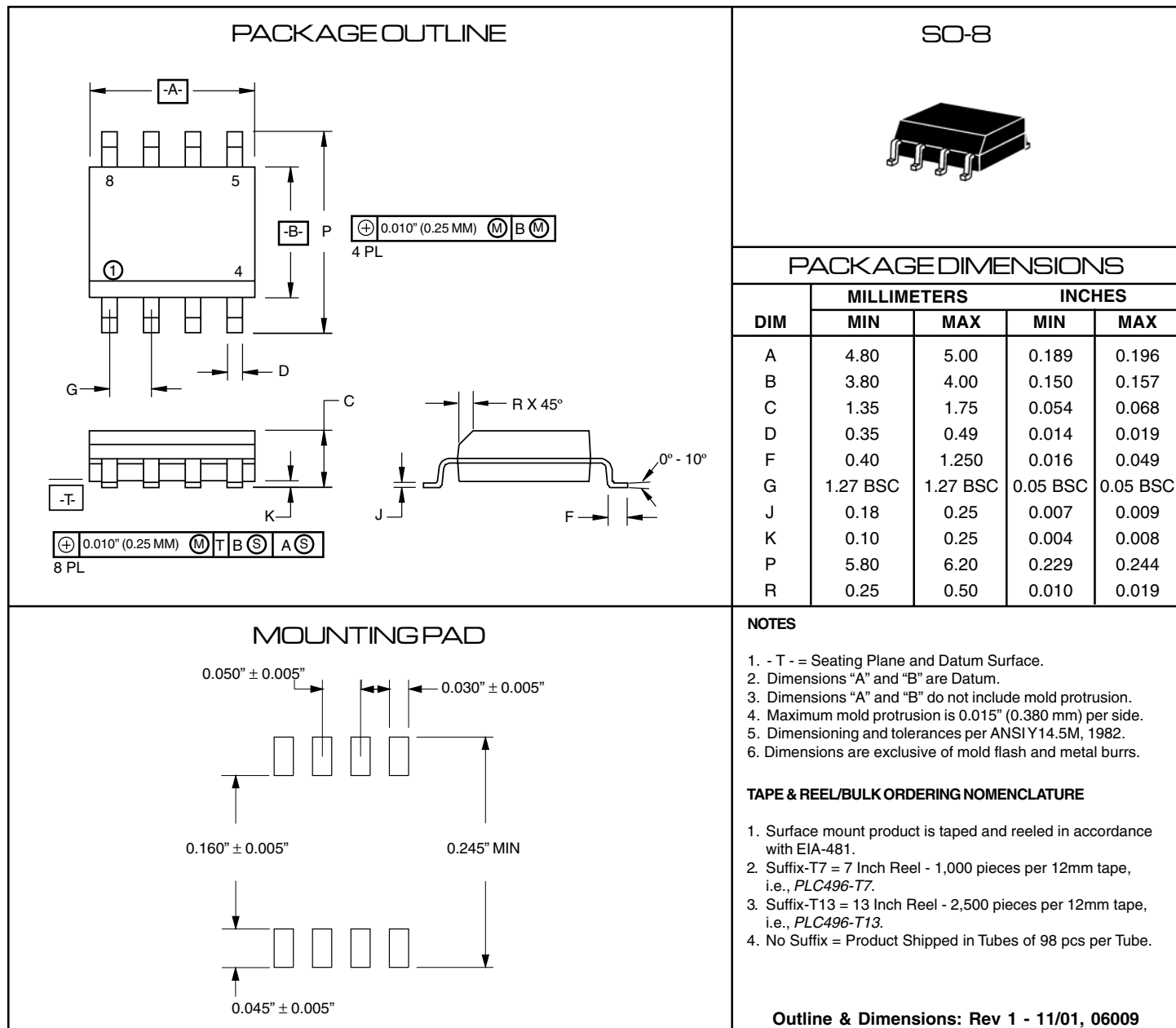


Figure 2. Typical Common Mode Sensor Protection Circuit



## PACKAGE OUTLINE & DIMENSIONS



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