MJB6488, MJB6491

Product Preview

Complementary Silicon Plastic Power Transistors

. . . designed for use in general−purpose amplifier and switching applications.

- DC Current Gain Specified to 15 A −
  h_{FE} = 20 − 150 @ I_C = 5.0 Adc
  = 5.0 (Min) @ I_C = 15 Adc
- Collector−Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 80 Vdc (Min)
- Epoxy Meets UL 94 V−0 @ 0.125 in
- ESD Ratings: Human Body Model; 3B, >8000 V,
  Machine Model; C, >400 V

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Collector−Base Voltage	V_{CB}	90	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous	I_C	15	Adc
Base Current	I_B	5.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	W W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.8 0.014	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	70	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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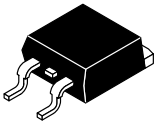
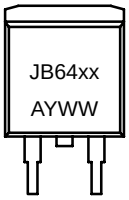
15 A
COMPLEMENTARY SILICON
POWER TRANSISTORS
80 V, 75 W



D²PAK
CASE 418B
STYLE 1

MARKING DIAGRAM



xx = 88 or 91
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
MJB6488	D²PAK	50 Units / Rail
MJB6488T4	D²PAK	800 / Tape & Reel
MJB6491	D²PAK	50 Units / Rail
MJB6491T4	D²PAK	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 1)	(I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	80	−	Vdc
Collector−Emitter Sustaining Voltage (Note 1)	(I_C = 200 mAdc, V_{BE} = 1.5 Vdc)	VCEX	90	−	Vdc
Collector Cutoff Current	(V_{CE} = 40 Vdc, I_B = 0)	I_{CEO}	−	1.0	mAdc
Collector Cutoff Current	(V_{CE} = 85 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	− −	100 5.0	μAdc mAdc
Emitter Cutoff Current	(V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	−	10	μA
ON CHARACTERISTICS					
DC Current Gain	(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 15 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 5.0	150 −	−
Collector−Emitter Saturation Voltage	(I_C = 5.0 Adc, I_B = 0.5 Adc) (I_C = 15 Adc, I_B = 5.0 Adc)	$V_{CE(sat)}$	− −	1.3 3.5	Vdc
Base−Emitter On Voltage	(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 15 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	− −	1.3 3.5	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (Note 2)	(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 MHz)	f_T	5.0	−	MHz
Small−Signal Current Gain	(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	25	−	−

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
2. $f_T = |h_{fe}| \bullet f_{test}$.

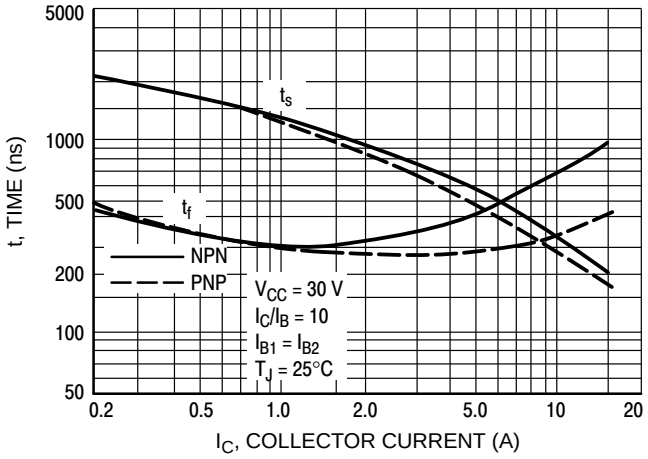


Figure 1. Turn−Off Time

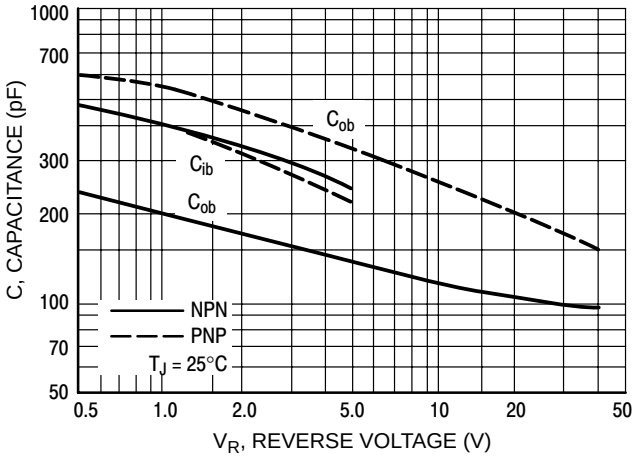


Figure 2. Capacitances

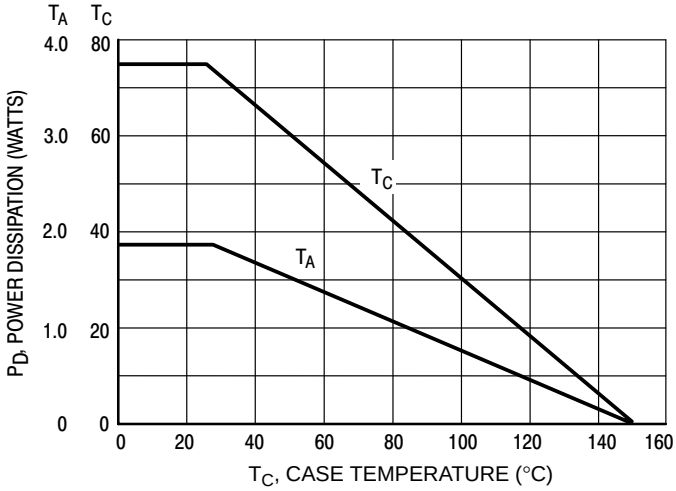
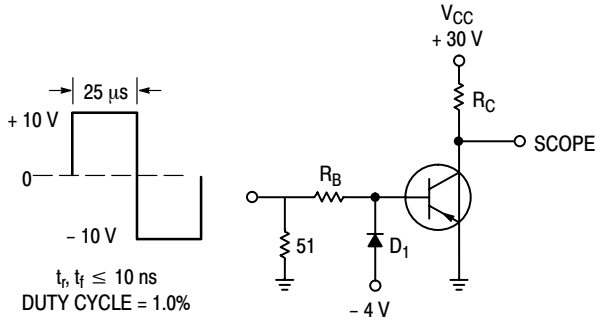


Figure 3. Power Derating



R_B AND R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS.
FOR PNP, REVERSE ALL POLARITIES.

D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

Figure 4. Switching Time Test Circuit

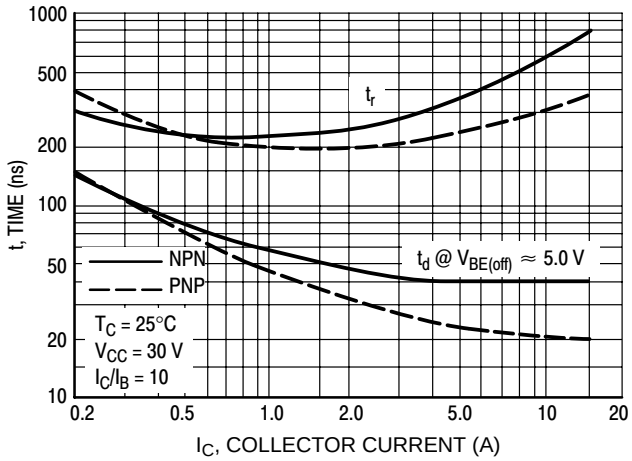


Figure 5. Turn−On Time

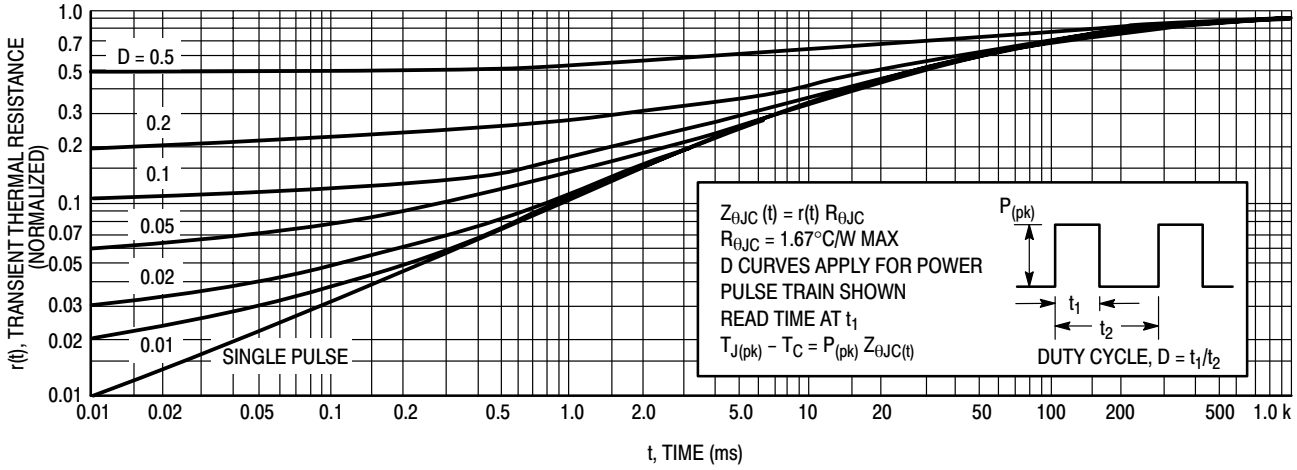


Figure 6. Thermal Response

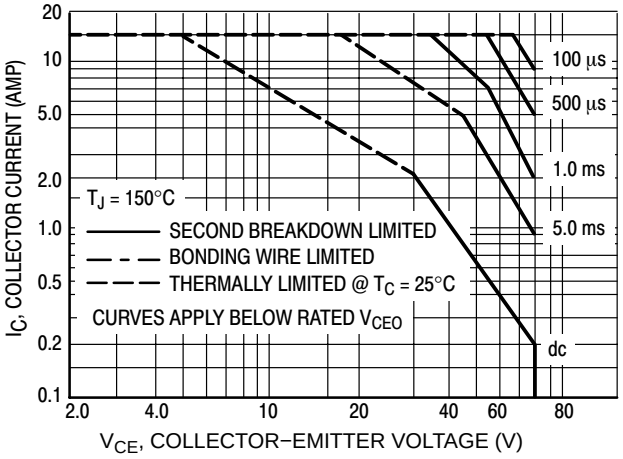


Figure 7. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistors average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

NPN − MJB6488 **PNP − MJB6491**

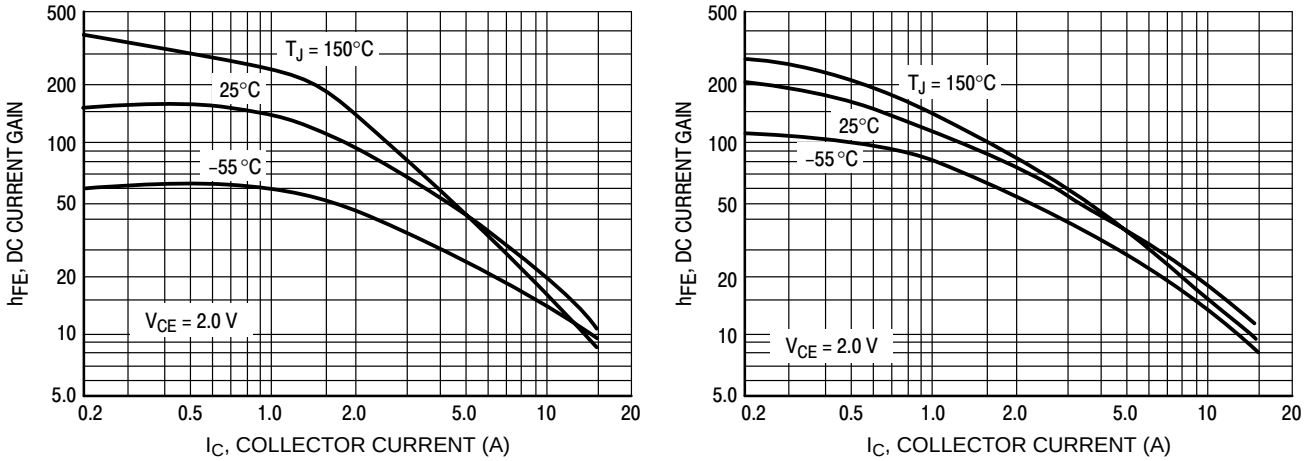


Figure 8. DC Current Gain

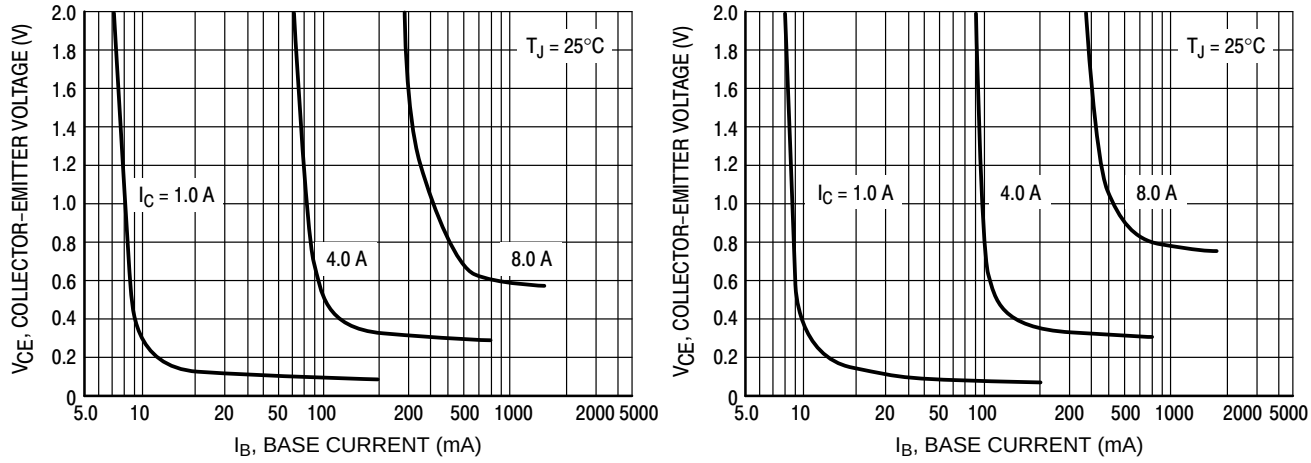


Figure 9. Collector Saturation Region

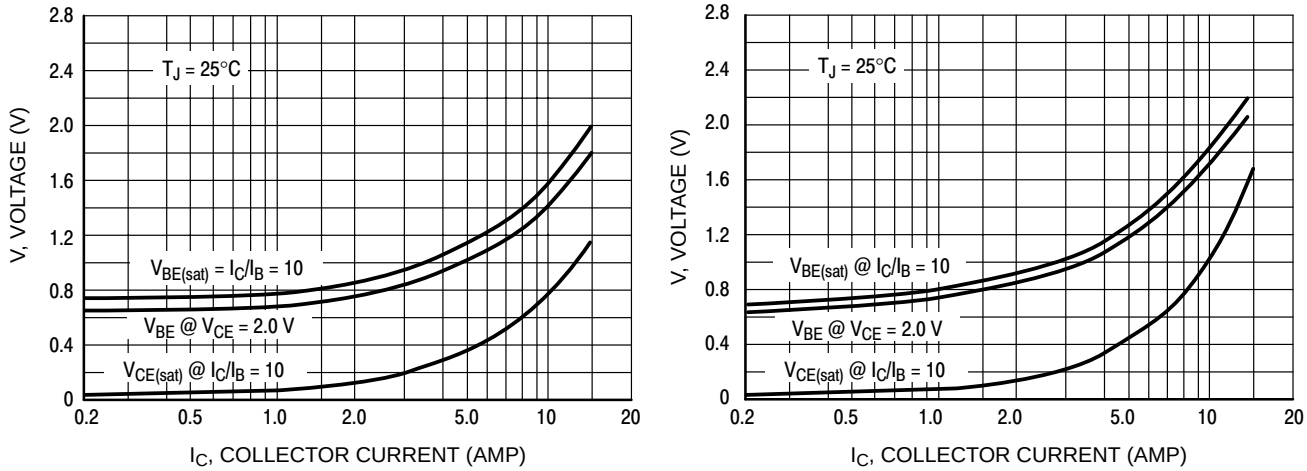
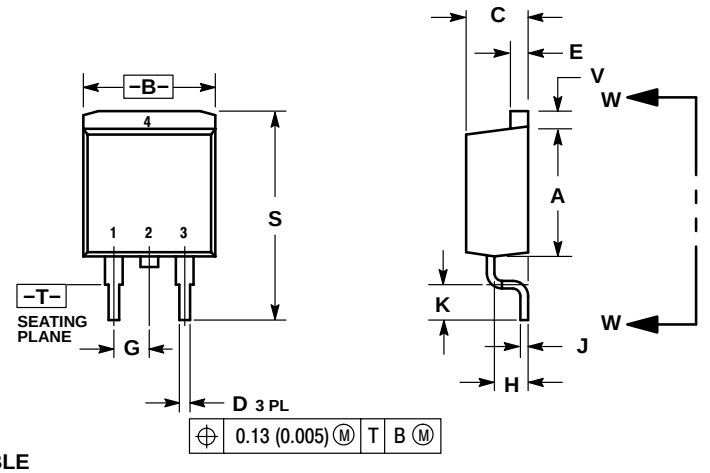


Figure 10. “On” Voltages

PACKAGE DIMENSIONS

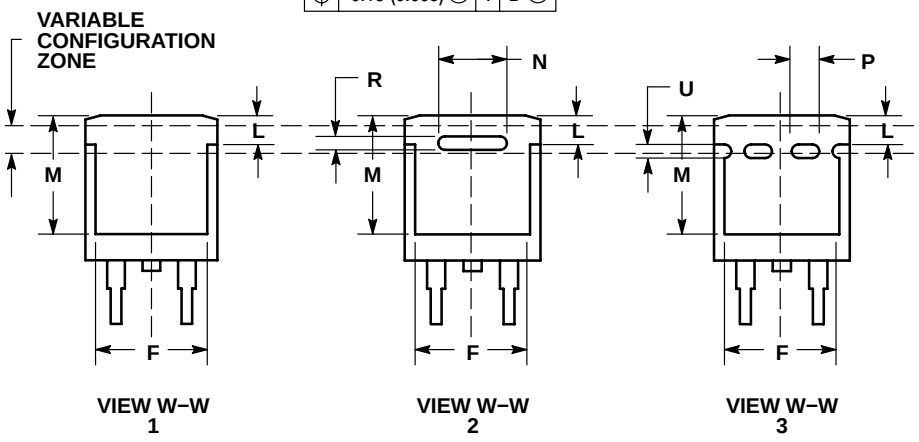
D²PAK
CASE 418B−04
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B−01 THRU 418B−03 OBSOLETE, NEW STANDARD 418B−04.

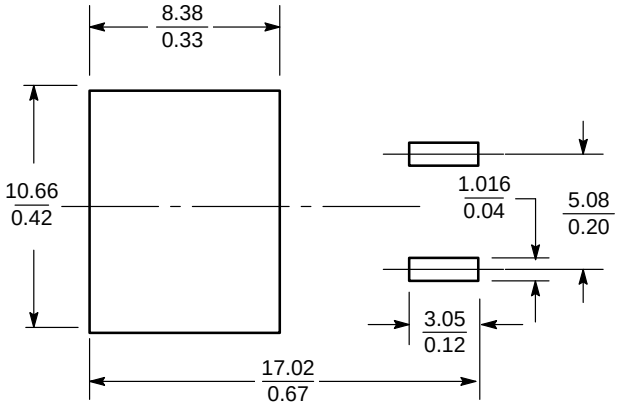
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



VIEW W−W 1 | VIEW W−W 2 | VIEW W−W 3

SOLDERING FOOTPRINT



SCALE 3:1 (mm / inches)

PUBLICATION ORDERING INFORMATION

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