EMIF02-USB01

2 LINES EMI FILTER INCLUDING ESD PROTECTION

IPAD™

MAIN APPLICATION

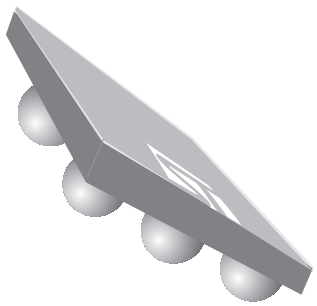
- ESD protection and EMI filtering for USB port.

DESCRIPTION

The EMIF02-USB01 is a highly integrated array designed to suppress EMI / RFI noise for USB port filtering.

The EMIF02-USB01 flip-chip packaging means the package size is equal to the die size. That's why EMIF02-USB01 is a very small device.

Additionally, this filter includes an ESD protection circuitry which prevents the protected device from destruction when subjected to ESD surges up to 15 kV.



Flip Chip package

BENEFITS

- 2 lines low-pass-filter + 2 lines ESD protection
- High efficiency in EMI filtering
- Very low PCB space consuming: 2.5 mm^2
- Very thin package: 0.65 mm
- High efficiency in ESD suppression (IEC61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.

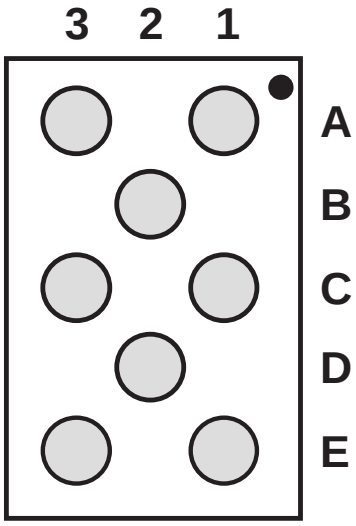
COMPLIES WITH THE FOLLOWING STANDARDS :

IEC61000-4-2 level 4

15kV (air discharge)
8 kV (contact discharge)

on input & output pins.

PIN CONFIGURATION



TM : ASD is trademark of STMicroelectronics.

SCHEMATIC

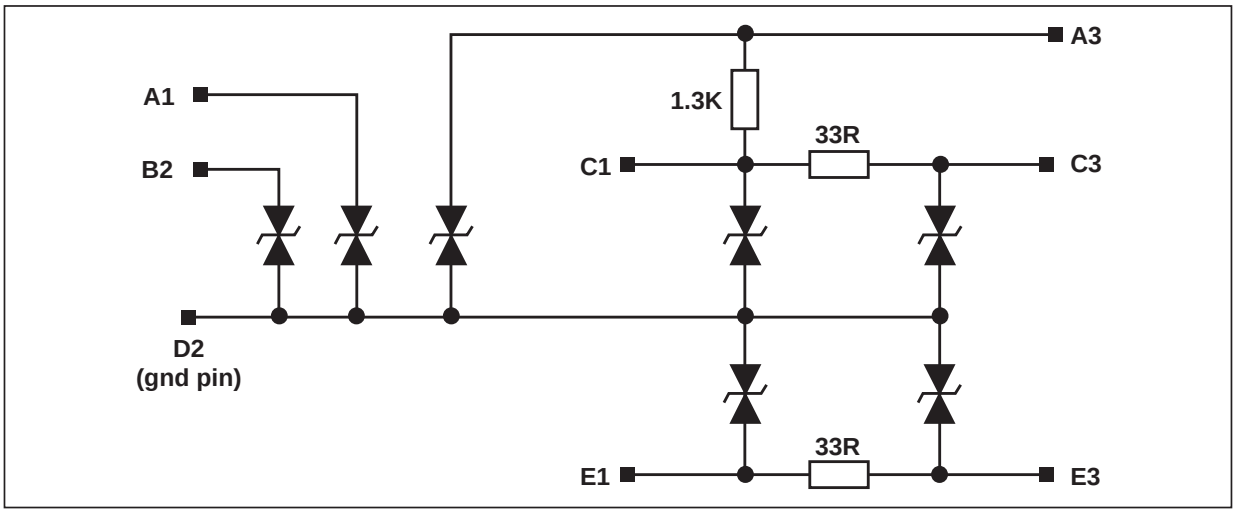


Fig. 1: Filtering behavior

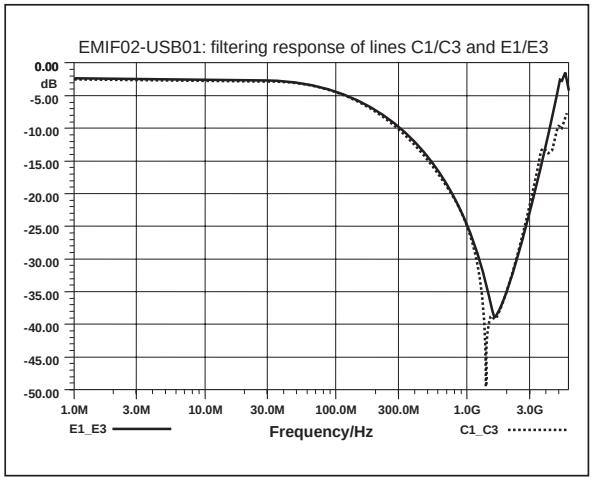


Fig. 2: ESD response to IEC61000-4-2 Level 4

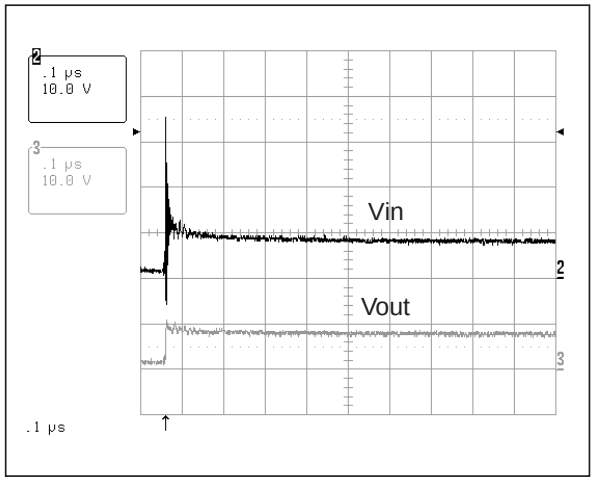


Fig. 3: Capacitance versus reverse applied voltage

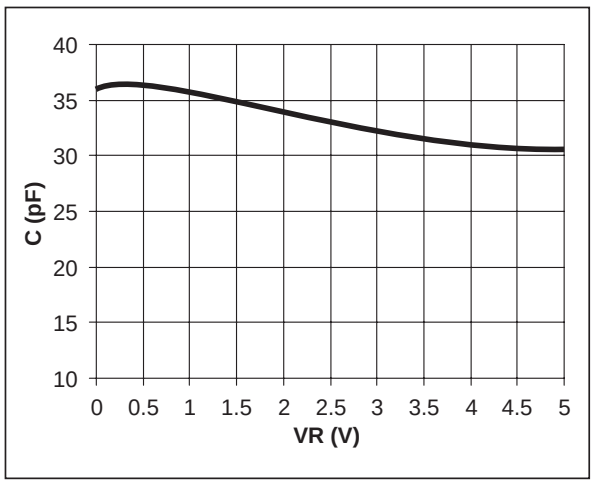
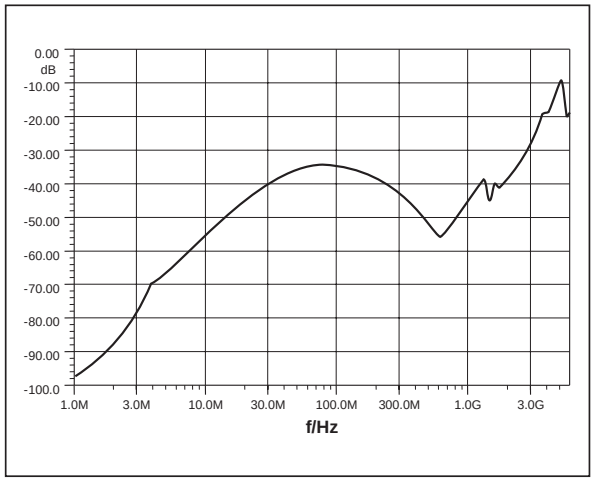


Fig. 4: Digital crosstalk

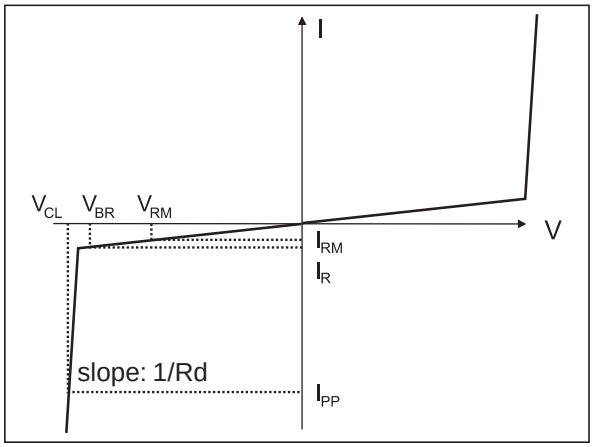


ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C)

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharge	15 8	kV
T_j	Junction temperature	125	°C
T_{op}	Operating temperature range	-40 to + 85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
Rd	Dynamic impedance
I_{PP}	Peak pulse current



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6			V
I_{RM}	V_{RM} = 3V		0.1	0.5	µA
C_{line}	@ 0V		40	45	pF
R_1,R_2	Tolerance ± 5%		33.0		Ω
R_3	Tolerance ± 5%		1.30		kΩ

APLAC MODELS

Fig. 5: Aplac model of resistors

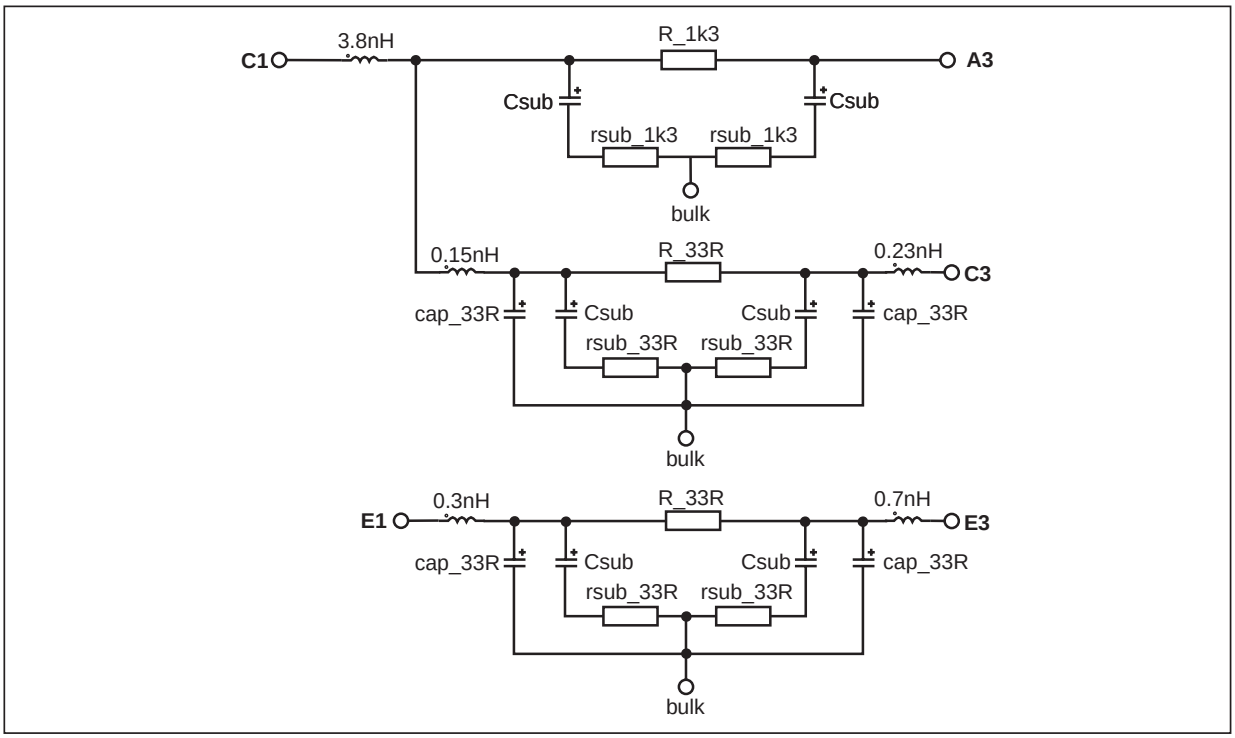


Fig. 6: Aplac model of the diodes

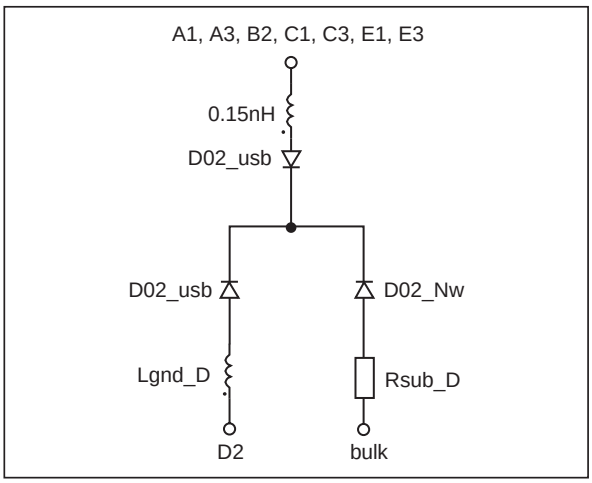


Fig. 7: Aplac model of bumps & ground connections

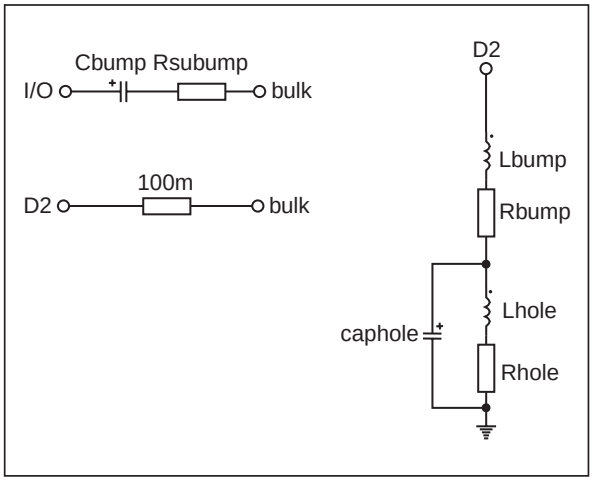
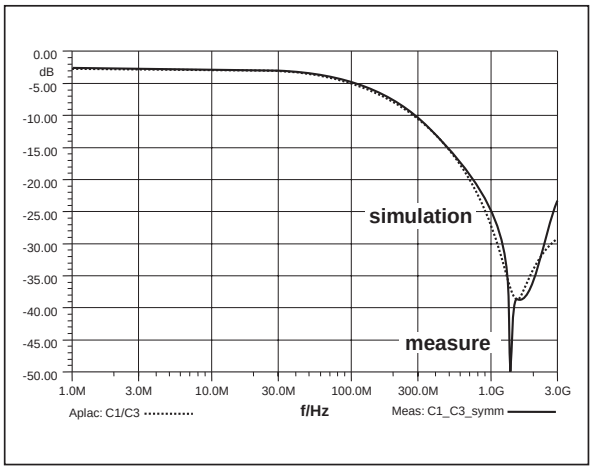


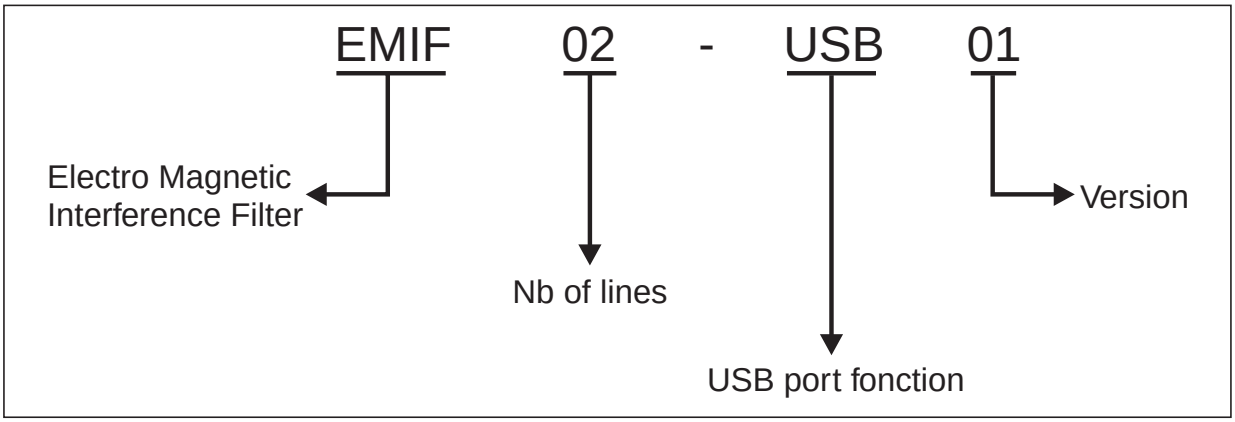
Fig. 8: Aplac model parameters

aplacvar R_33R 33.9	Model D02_Nw	Model D02_usb
aplacvar cap_33R 1.2pF	BV=100	BV=16
	IBV=1m	IBV=1m
aplacvar R_1k3 1.3k	CJO=6.8p	CJO=Cz
	M=0.3333	M=0.3333
	RS=2	RS=2
aplacvar Cz 29pF	VJ=0.6	VJ=0.6
aplacvar Rsub_D 100	TT=100n	TT=100n
aplacvar Csub 0.3pF		
aplacvar Rsub_33R 15		
aplacvar Rsub_1k3 50		
aplacvar lhole 10pH		
aplacvar Rhole 400m		
aplacvar Caphole 0.4pF		
aplacvar Lgnd_D 150pH		
aplacvar Lbump 50pH		
aplacvar Rbump 50m		
aplacvar Cbump 1.5pF		
aplacvar Rsubump 150		

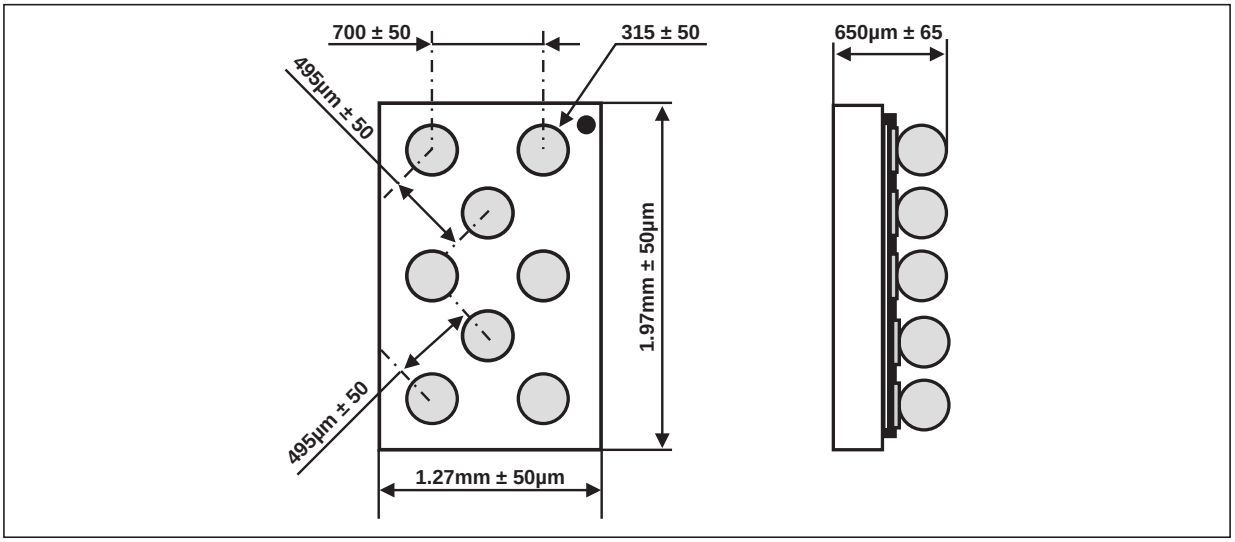
Fig. 9: Comparison between Aplac simulations and measured frequency response.



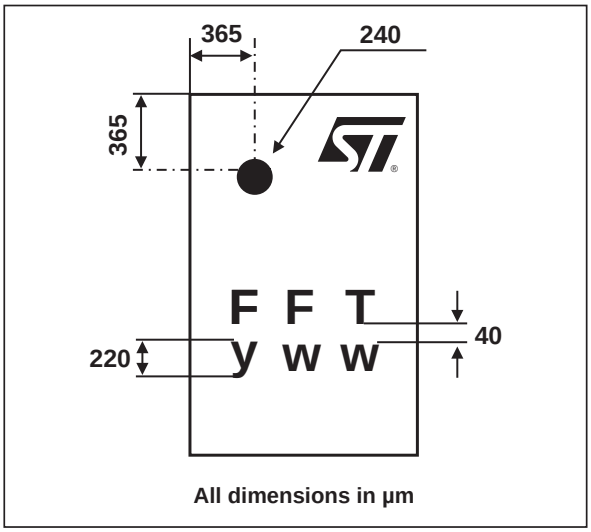
ORDER CODE



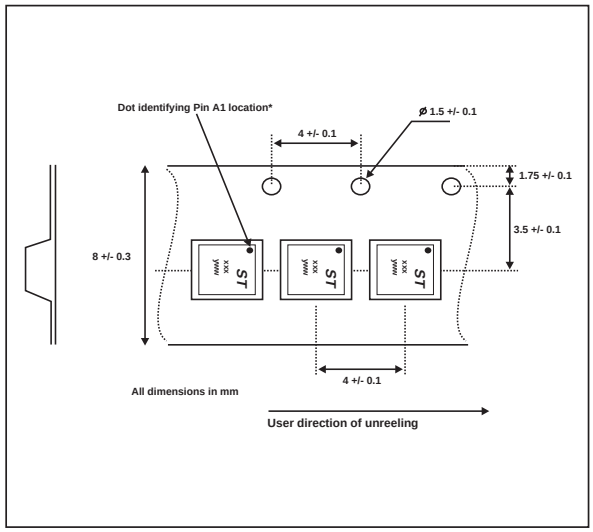
PACKAGE MECHANICAL DATA



MARKING



PACKING



OTHER INFORMATION

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-USB01	FFT	Flip Chip	3.35 mg	5000	Tape & reel (7”)

Note: More packing informations are available in the application note AN1235: "Flip-Chip CSP: Package description and recommandations for use"