

FDV302P Digital FET, P-Channel

General Description

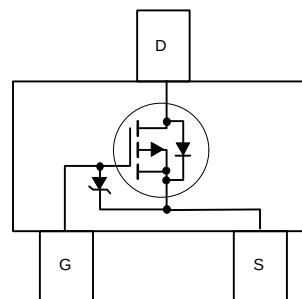
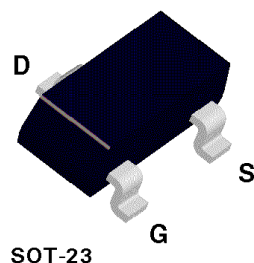
This P-Channel logic level enhancement mode field effect transistor is produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for digital transistors. Since bias resistors are not required, this one P-channel FET can replace several digital transistors with different bias resistors such as the DTCx and DCDx series.

Features

- -25 V, -0.12 A continuous, -0.5 A Peak.
 $R_{DS(ON)} = 13 \Omega @ V_{GS} = -2.7 V$
 $R_{DS(ON)} = 10 \Omega @ V_{GS} = -4.5 V.$
- Very low level gate drive requirements allowing direct operation in 3V circuits. $V_{GS(th)} < 1.5V.$
- Gate-Source Zener for ESD ruggedness. >6kV Human Body Model
- Compact industry standard SOT-23 surface mount package.
- Replace many PNP digital transistors (DTCx and DCDx) with one DMOS FET.



Mark:302



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDV302P	Units
V_{DSS}	Drain-Source Voltage	-25	V
V_{GSS}	Gate-Source Voltage	-8	V
I_D	Drain Current	- Continuous	A
		- Pulsed	
P_D	Maximum Power Dissipation	0.35	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)	6.0	kV

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	357	$^\circ\text{C/W}$
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Electrical Characteristics (T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = -250 μA	-25			V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	I _D = -250 μA, Referenced to 25 °C		-20		mV / °C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -20 V, V _{GS} = 0 V T _J = 55°C			-1	μA
I _{GSS}	Gate - Body Leakage Current	V _{GS} = -8 V, V _{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note)						
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Temp. Coefficient	I _D = -250 μA, Referenced to 25 °C		1.9		mV / °C
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250 μA	-0.65	-1	-1.5	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = -2.7 V, I _D = -0.05 A		10.6	13	Ω
		V _{GS} = -4.5 V, I _D = -0.2 A		7.9	10	
		T _J =125°C		12	18	
I _{D(on)}	On-State Drain Current	V _{GS} = -2.7 V, V _{DS} = -5 V	-0.05			A
g _{FS}	Forward Transconductance	V _{DS} = -5 V, I _D = -0.2 A		0.135		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input Capacitance	V _{DS} = -10 V, V _{GS} = 0 V, f = 1.0 MHz		11		pF
C _{oss}	Output Capacitance			7		pF
C _{rss}	Reverse Transfer Capacitance			1.4		pF
SWITCHING CHARACTERISTICS (Note)						
t _{D(on)}	Turn - On Delay Time	V _{DD} = -6 V, I _D = -0.2 A, V _{GS} = -4.5 V, R _{GEN} = 50 Ω		5	12	ns
t _r	Turn - On Rise Time			8	16	ns
t _{D(off)}	Turn - Off Delay Time			9	18	ns
t _f	Turn - Off Fall Time			5	10	ns
Q _g	Total Gate Charge	V _{DS} = -5 V, I _D = -0.2 A, V _{GS} = -4.5 V		0.22	0.31	nC
Q _{gs}	Gate-Source Charge			0.11		nC
Q _{gd}	Gate-Drain Charge			0.04		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I _S	Maximum Continuous Drain-Source Diode Forward Current				-0.2	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = -0.2 A (Note)		-1	-1.5	V

Note:

Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

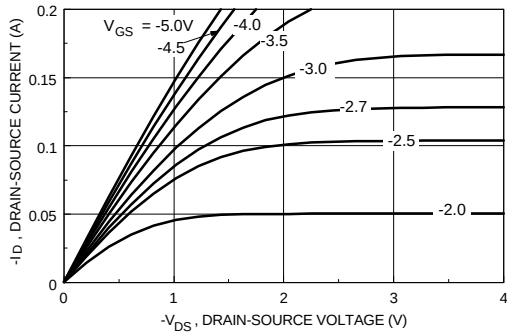


Figure 1. On-Region Characteristics.

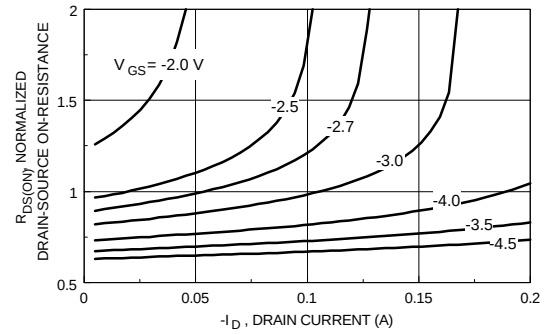


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

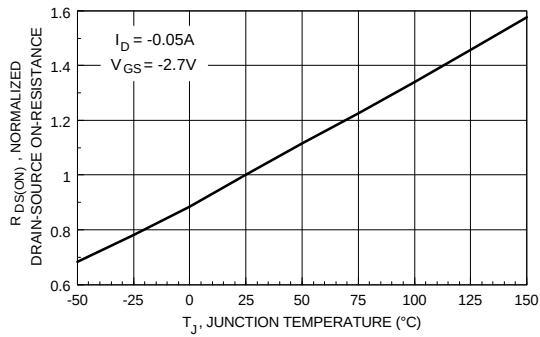


Figure 3. On-Resistance Variation with Temperature.

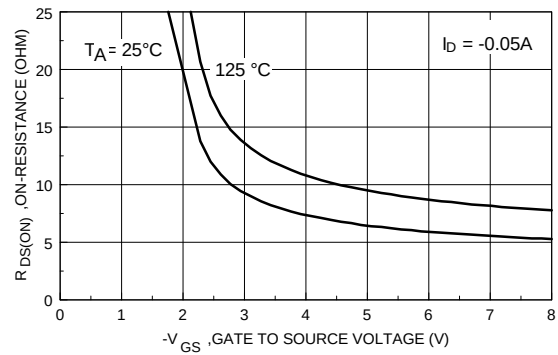


Figure 4. On Resistance Variation with Gate-To- Source Voltage.

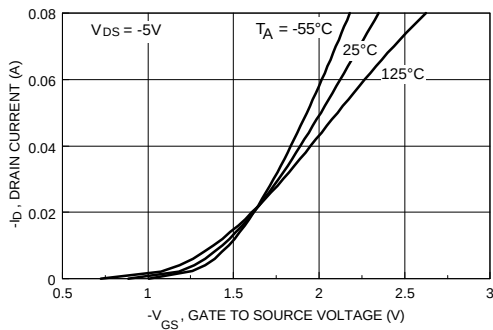


Figure 5. Transfer Characteristics.

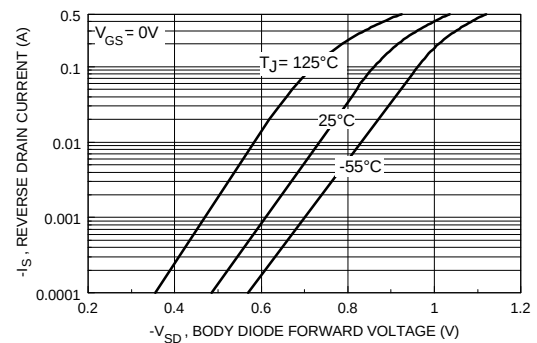


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical And Thermal Characteristics

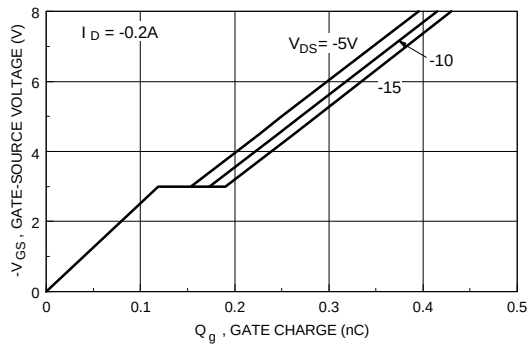


Figure 7. Gate Charge Characteristics.

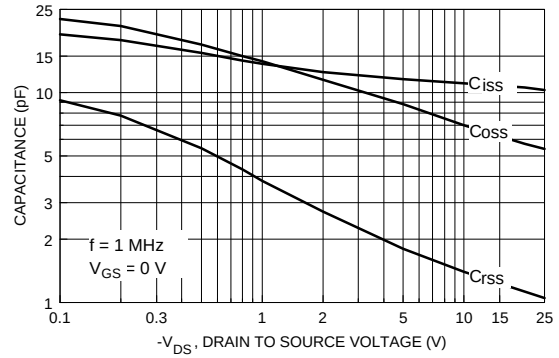


Figure 8. Capacitance Characteristics.

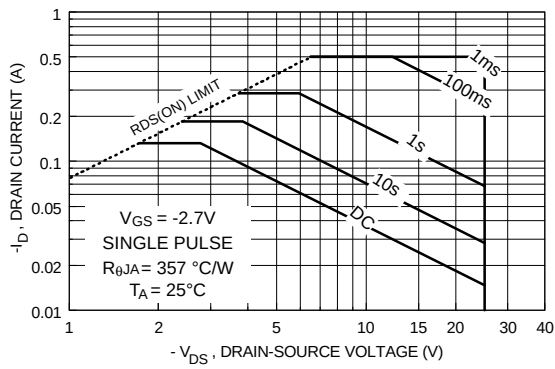


Figure 9. Maximum Safe Operating Area.

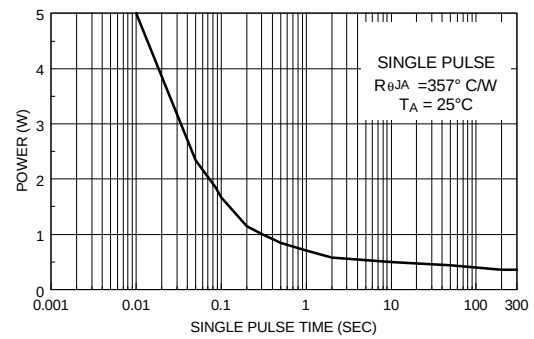


Figure 10. Single Pulse Maximum Power Dissipation.

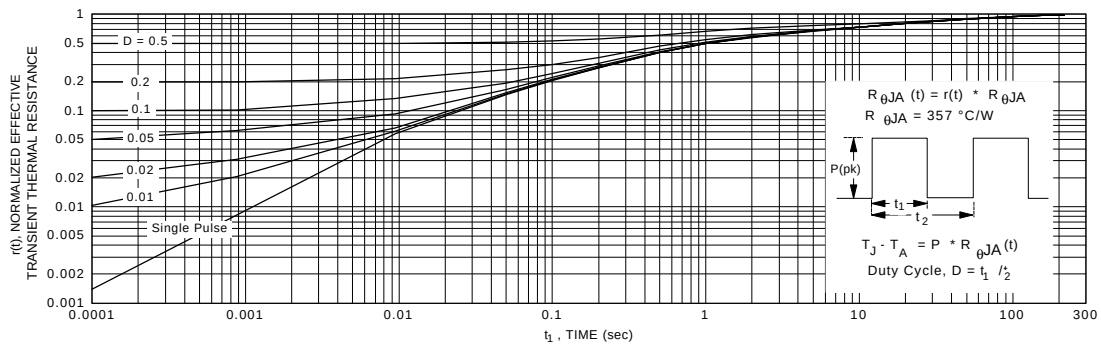


Figure 11. Transient Thermal Response Curve.