

XC61C

Series

Standard Voltage Detectors ($V_{DF}=1.6V\sim6.0V$)



◆CMOS

◆Highly Accurate : $\pm 2\%$

◆Low Power Consumption : $0.7\mu A$ ($V_{IN} = 1.5V$)

◆Ultra small SSOT-24 (SC-82) Package

■General Description

The XC61C series are highly precise, low power consumption voltage detectors, manufactured using CMOS and laser trimming technologies. Detect voltage is extremely accurate with minimal temperature drift.

Both CMOS and N-channel open drain output configurations are available.

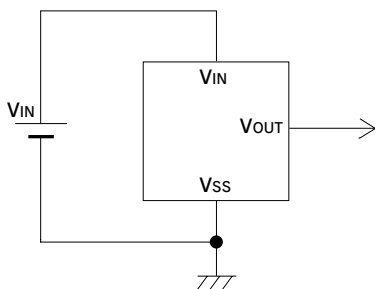
■Applications

- Microprocessor reset circuitry
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection
- System battery life and charge voltage monitors

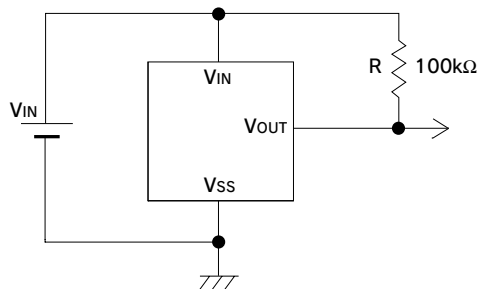
■Features

- Highly accurate** : $\pm 2\%$
- Low power consumption** : TYP $0.7\mu A$ [$V_{IN}=1.5V$]
- Detect voltage range** : $1.6V \sim 6.0V$ in $0.1V$ increments
- Operating voltage range** : $0.7V \sim 10.0V$
- Detect voltage temperature characteristics** : $TYP \pm 100ppm/^{\circ}C$
- Output configuration** : N-channel open drain or CMOS
- Ultra small package** : SSOT-24 (150mW) super mini-mold
: SOT-23 (150mW) mini-mold
: SOT-89 (500mW) mini-power mold
: TO-92 (300mW)

■Typical Application Circuits



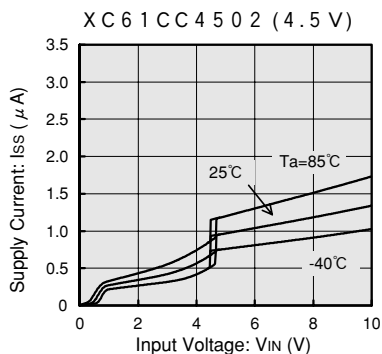
CMOS Output



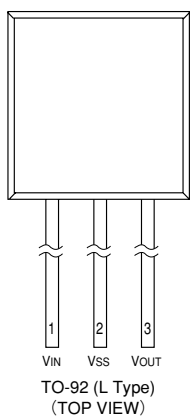
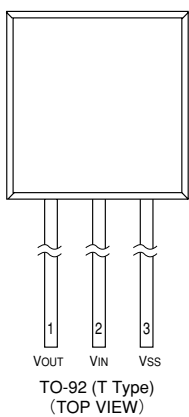
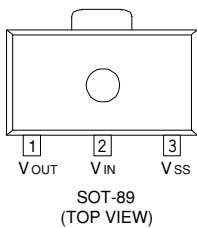
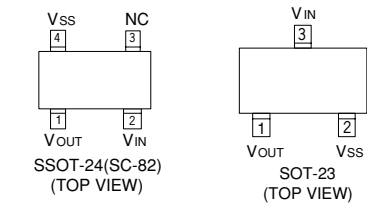
N-ch Open Drain Output

■Typical Performance Characteristic

SUPPLY CURRENT vs. INPUT VOLTAGE



Pin Configuration



Pin Assignment

PIN NUMBER					PIN NAME	FUNCTION
SSOT-24	SOT-23	SOT-89	TO-92 (T)	TO-92 (L)		
2	3	2	2	1	V _{IN}	Supply Voltage Input
4	2	3	3	2	V _{SS}	Ground
1	1	1	1	3	V _{OUT}	Output
3	-	-	-	-	NC	No Connection

2

Product Classification

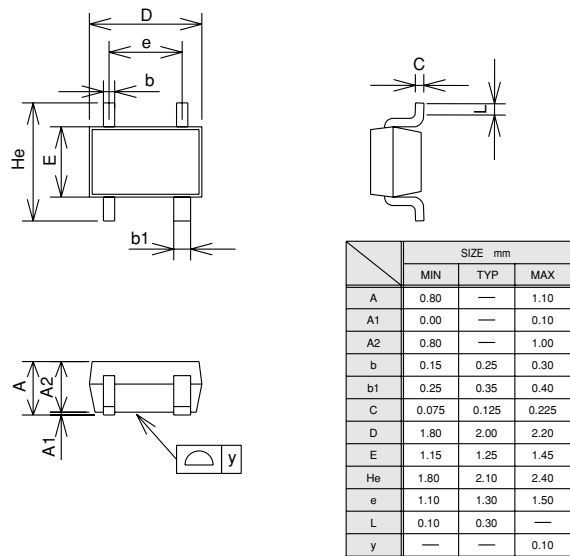
Ordering Information

XC61C xx xx xx xx
a b c d e f

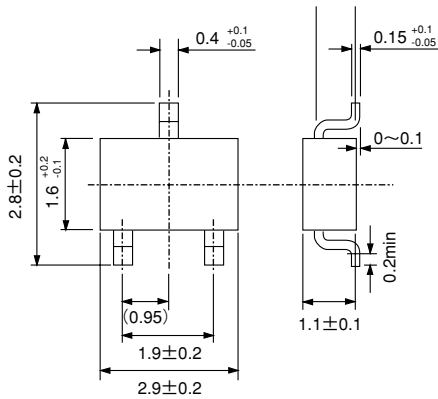
DESIGNATOR	DESCRIPTION	DESIGNATOR	DESCRIPTION
a	Output Configuration : C = CMOS N = N-ch open drain	e	Package Type: N = SSOT-24 (SC-82) M = SOT-23 P = SOT-89 T = TO-92 (Standard) L = TO-92 (Custom Pin Configuration)
b	Detect Voltage : 25 = 2.5V 38 = 3.8V		
c	Output Delay : 0 = No delay	f	Device Orientation : R = Embossed Tape (Right) L = Embossed Tape (Left) H = Paper Type (TO-92) B = Bag (TO-92)
d	Detect Accuracy : 2 = within $\pm 2.0\%$		

■Packaging Information

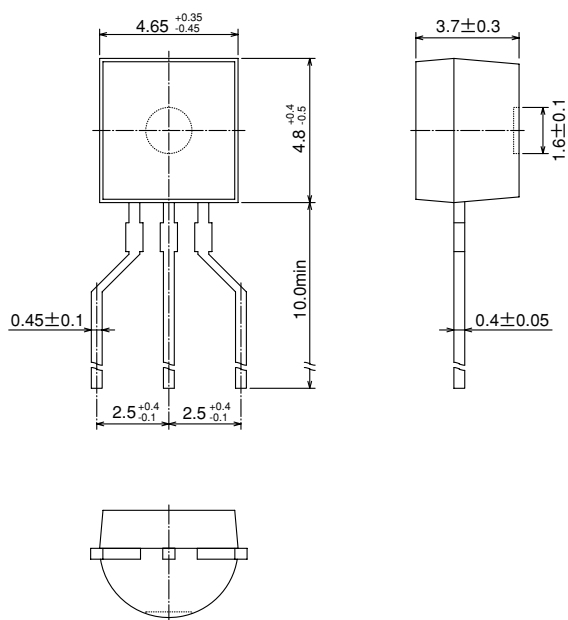
●SSOT-24 (SC-82)



●SOT-23

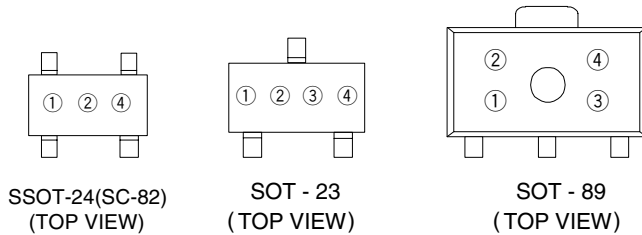


●TO-92



■ Marking

● SSOT-24, SOT-23, SOT-89



① Represents the integer of the Output Voltage and Detect Voltage

DESIGNATOR	CONFIGURATION	VOLTAGE (V)
A	CMOS	0.②
B	CMOS	1.②
C	CMOS	2.②
D	CMOS	3.②
E	CMOS	4.②
F	CMOS	5.②
H	CMOS	6.②

DESIGNATOR	CONFIGURATION	VOLTAGE (V)
K	N-ch	0.②
L	N-ch	1.②
M	N-ch	2.②
N	N-ch	3.②
P	N-ch	4.②
R	N-ch	5.②
S	N-ch	6.②

② Represents the decimal number of the Detect Voltage

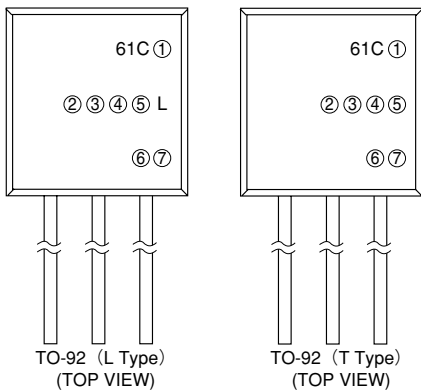
DESIGNATOR	VOLTAGE	DESIGNATOR	VOLTAGE
0	①.0	5	①.5
1	①.1	6	①.6
2	①.2	7	①.7
3	①.3	8	①.8
4	①.4	9	①.9

③ Based on Internal Standards
(SSOT-24 excepted)

DESIGNATOR
3

④ Represents the assembly lot no.
Based on internal standards

● TO-92



① Represents the output configuration

DESIGNATOR	OUTPUT CONFIGURATION
C	CMOS
N	N-ch

② Represents the Detect Voltage

DESIGNATOR		VOLTAGE (V)
②	③	
3	3	3.3
5	0	5.0

④ Indicates Delay Time

DESIGNATOR	DELAY TIME
0	No delay

⑤ Represents the Detect Voltage Accuracy

DESIGNATOR	DETECT VOLTAGE ACCURACY
1	within $\pm 1\%$ (semi-custom)
2	within $\pm 2\%$

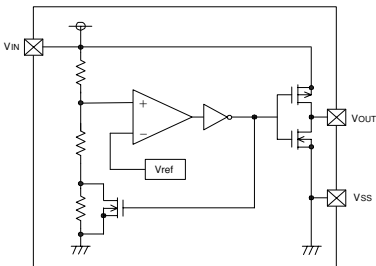
⑥ Represents a least significant digit of the produced year

DESIGNATOR	Produced year
0	2000
1	2001

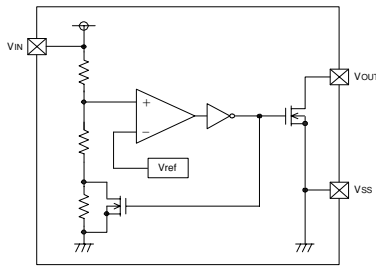
⑦ Denotes the production lot number
0 to 9, A to Z repeated (G.I.J.O.Q.W excepted)

■Block Diagram

(1) CMOS Output



(2) N-ch Open Drain Output



■Absolute Maximum Ratings

Ta = 25°C

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		VIN	12	V
Output Current		IOUT	50	mA
Output Voltage	CMOS	VOUT	VSS -0.3 ~ VIN +0.3	V
	N-ch open drain		VSS -0.3 ~ 12	
Power Dissipation	SSOT-24	Pd	150	mW
	SOT-23		150	
	SOT-89		500	
	TO-92		300	
Operating Ambient Temperature		Topr	-40 ~ +85	°C
Storage Temperature		Tstg	-40 ~ +125	°C

■Electrical Characteristics

VDF (T) = 1.6 to 6.0V ± 2%

Ta = 25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	CIRCUIT
Detect Voltage	VDF		VDF x 0.98	VDF	VDF x 1.02	V	1
Hysteresis Range	VHYS		VDF x 0.02	VDF x 0.05	VDF x 0.08	V	1
Supply Current	ISS	VIN =1.5V		0.7	2.3	μA	2
		=2.0V		0.8	2.7		
		=3.0V		0.9	3.0		
		=4.0V		1.0	3.2		
		=5.0V		1.1	3.6		
Operating Voltage	VIN	VDF(T) = 1.6V to 6.0V	0.7		10.0	V	1
Output Current	IOUT	N-ch	VDS=0.5V			mA	3
		VIN=1.0V	1.0	2.2			
		=2.0V	3.0	7.7			
		=3.0V	5.0	10.1			
		=4.0V	6.0	11.5			
		=5.0V	7.0	13.0			
		P-ch	VDS=2.1V		-10.0	-2.0	4
(with CMOS output)		VIN=8.0V					
Temperature Characteristics	$\frac{\Delta \text{ VDF}}{\Delta \text{ Topr} \cdot \text{ VDF}}$	-40°C ≤ Topr ≤ 85°C		± 100		ppm/°C	-
Delay Time (VDR→VOUT inversion)	tDLY				0.2	ms	5

Note :

VDF (T) : Established Detect Voltage Value

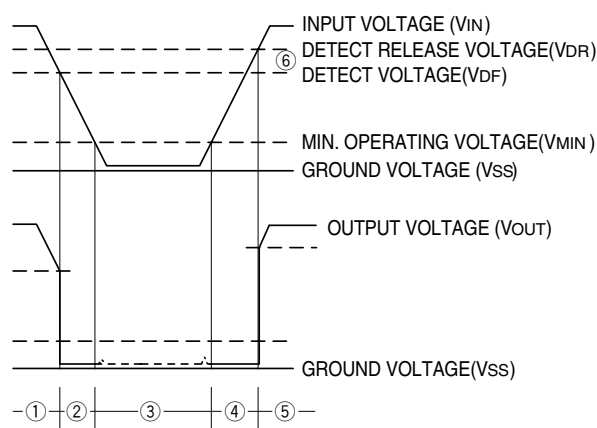
Release Voltage : VDR = VDF + VHYS

Functional Description

Functional Description (CMOS output)

- ① When input voltage (V_{IN}) rises above detect voltage (V_{DF}), output voltage (V_{OUT}) will be equal to V_{IN} .
(A condition of high impedance exists with N-ch open drain output configurations.)
- ② When input voltage (V_{IN}) falls below detect voltage (V_{DF}), output voltage (V_{OUT}) will be equal to the ground voltage (V_{SS}) level.
- ③ When input voltage (V_{IN}) falls to a level below that of the minimum operating voltage (V_{MIN}), output will become unstable. In this condition, V_{IN} will equal the pulled-up output (should output be pulled-up.)
- ④ When input voltage (V_{IN}) rises above the ground voltage (V_{SS}) level, output will be unstable at levels below the minimum operating voltage (V_{MIN}). Between the V_{MIN} and detect release voltage (V_{DR}) levels, the ground voltage (V_{SS}) level will be maintained.
- ⑤ When input voltage (V_{IN}) rises above detect release voltage (V_{DR}), output voltage (V_{OUT}) will be equal to V_{IN} .
(A condition of high impedance exists with N-ch open drain output configurations.)
- ⑥ The difference between V_{DR} and V_{DF} represents the hysteresis range.

Timing Chart



■Directions for use

●Notes on Use

1. Please use this IC within the stated maximum ratings. Operation beyond these limits may cause degrading or permanent damage to the device.
2. When a resistor is connected between the VIN pin and the input with CMOS output configurations, oscillation may occur as a result of voltage drops at RIN if load current (IOUT) exists. (refer to the Oscillation Description (1) below)
3. When a resistor is connected between the VIN pin and the input with CMOS output configurations, irrespective of N-ch output configurations, oscillation may occur as a result of through current at the time of voltage release even if load current (IOUT) does not exist. (refer to the Oscillation Description (2) below)
4. With a resistor connected between the VIN pin and the input, detect and release voltage will rise as a result of the IC's supply current flowing through the VIN pin.
5. In order to stabilise the IC's operations, please ensure that VIN pin's input frequency's rise and fall times are more than several μ sec / V.
6. Please use N-ch open drains configuration, when a resistor RIN is connected between the VIN pin and power source. In such cases, please ensure that RIN is less than 10k Ω and that C is more than 0.1 μ F.

2

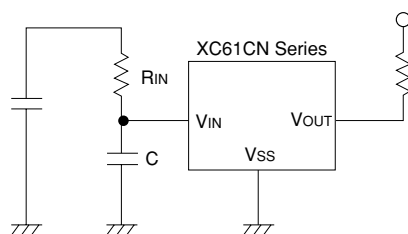


Diagram: Circuit using an input resistor

●Oscillation Description

(1) Output current oscillation with the CMOS output configuration

When the voltage applied at IN rises, release operations commence and the detector's output voltage increases. Load current (IOUT) will flow at RL. Because a voltage drop ($R_{IN} \times I_{OUT}$) is produced at the RIN resistor, located between the input (IN) and the VIN pin, the load current will flow via the IC's VIN pin. The voltage drop will also lead to a fall in the voltage level at the VIN pin. When the VIN pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, load current flow will cease and since voltage drop at RIN will disappear, the voltage level at the VIN pin will rise and release operations will begin over again. Oscillation may occur with this " release - detect - release " repetition.

Further, this condition will also appear via means of a similar mechanism during detect operations.

(2) Oscillation as a result of through current

Since the XC61C series are CMOS ICs, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur as a result of drops in voltage at the through current's resistor (RIN) during release voltage operations. (refer to diagram 2)

Since hysteresis exists during detect operations, oscillation is unlikely to occur.

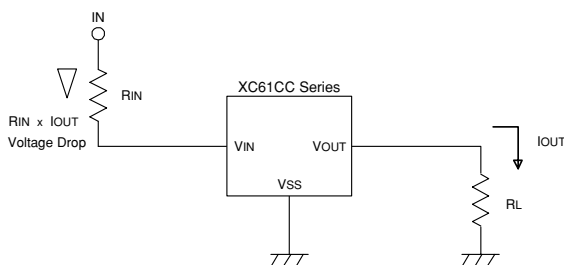


Diagram 1: Oscillation in relation to output current

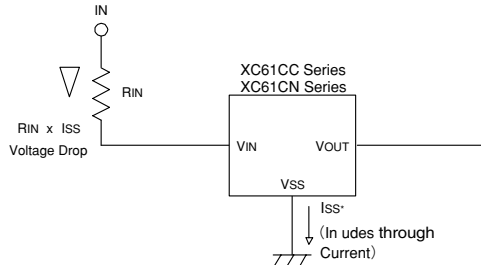
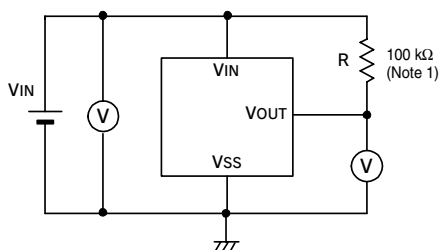


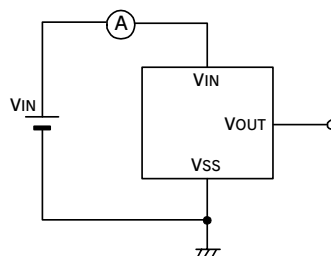
Diagram 2: Oscillation in relation to through current

Measuring Circuits

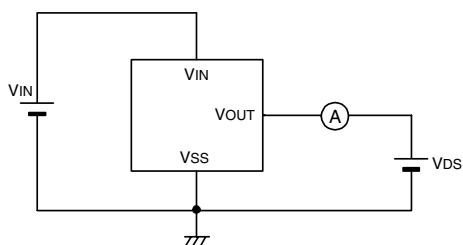
Circuit 1



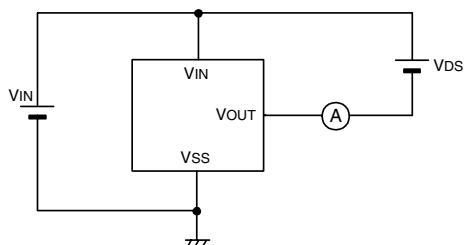
Circuit 2



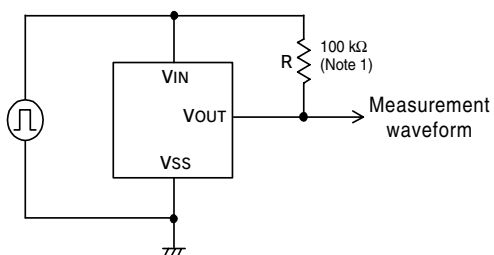
Circuit 3



Circuit 4



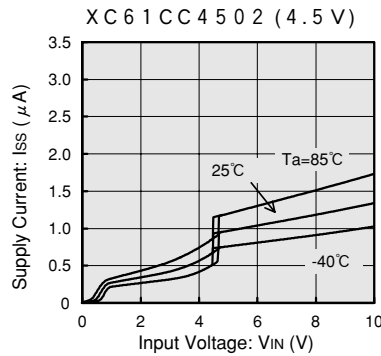
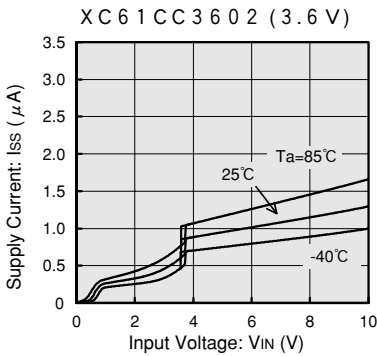
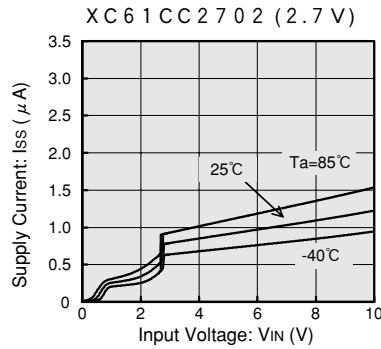
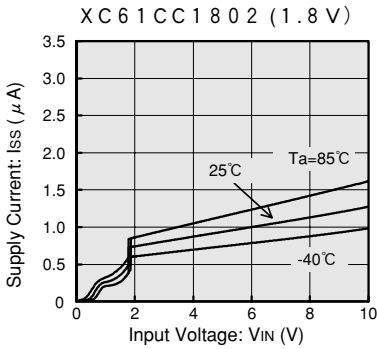
Circuit 5



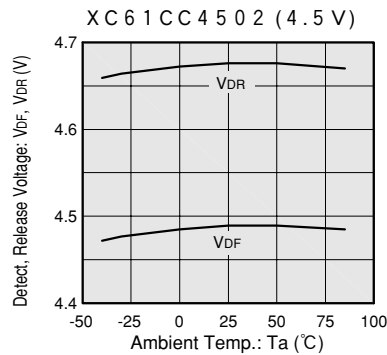
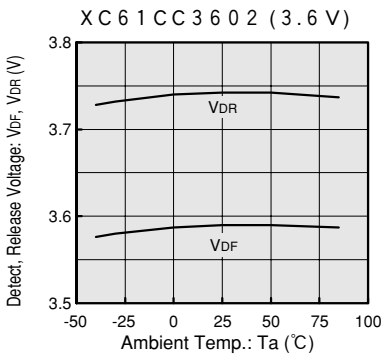
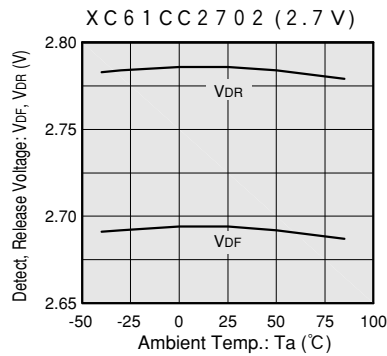
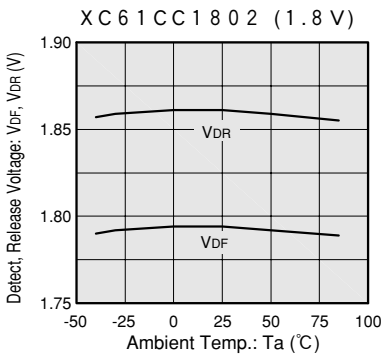
Note 1 : Not necessary with CMOS output products.

■ Typical Performance Characteristics

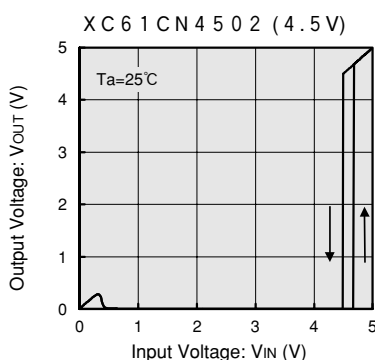
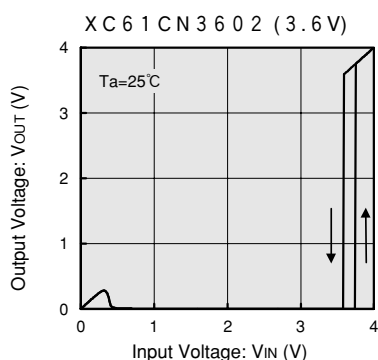
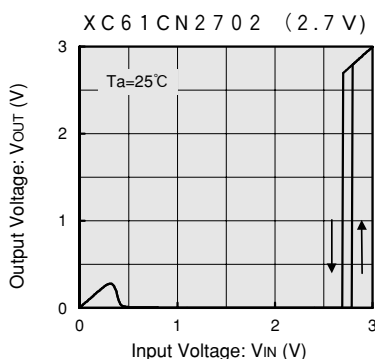
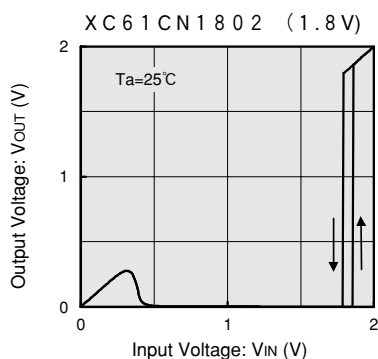
(1) SUPPLY CURRENT vs. INPUT VOLTAGE



(2) DETECT, RELEASE VOLTAGE vs. AMBIENT TEMPERATURE

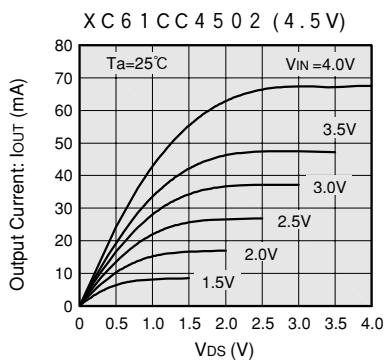
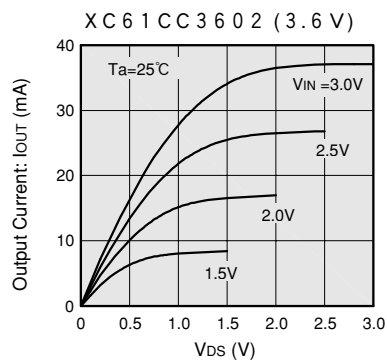
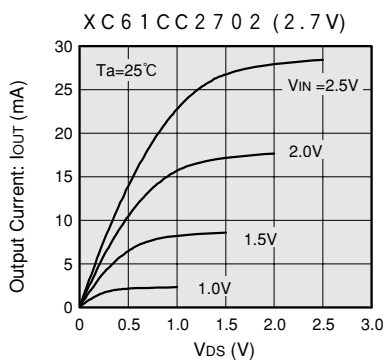
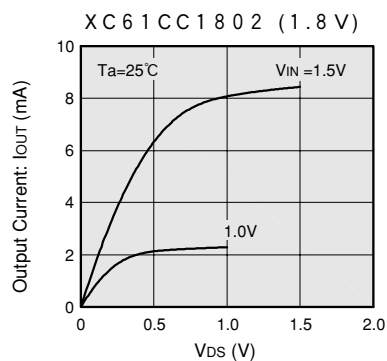


(3) OUTPUT VOLTAGE vs. INPUT VOLTAGE

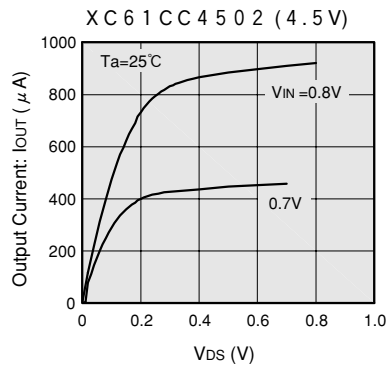
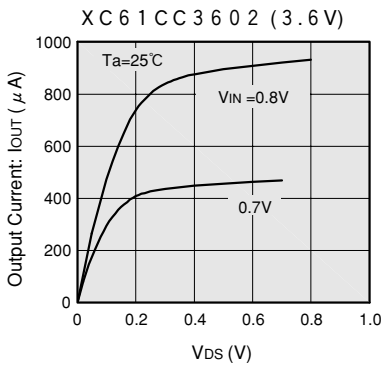
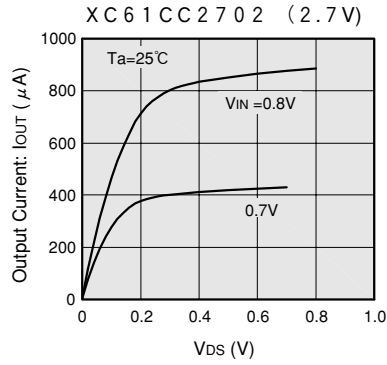
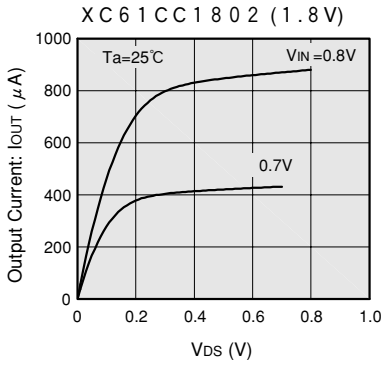


Note : The N-channel open drain pull up resistance value is 100k Ω .

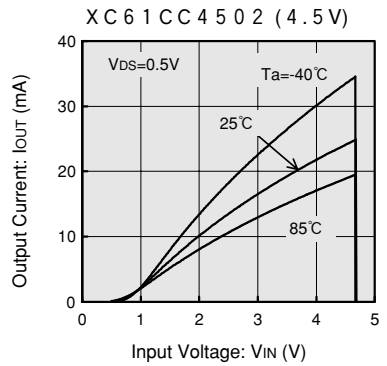
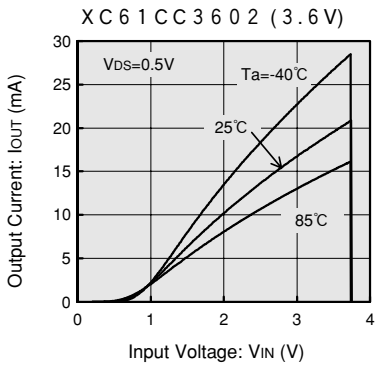
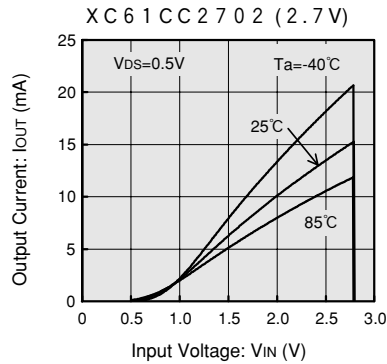
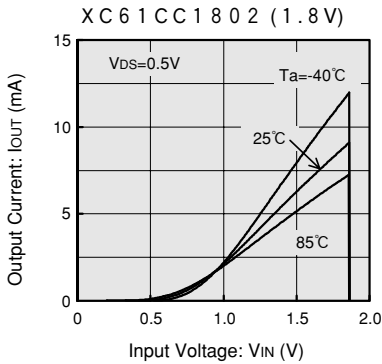
(4) N-ch DRIVER OUTPUT CURRENT vs. V_{DS}



(4) N-ch DRIVER OUTPUT CURRENT vs. V_{DS}



(5) N-ch DRIVER OUTPUT CURRENT vs. INPUT VOLTAGE



(6) P-ch DRIVER OUTPUT CURRENT vs. INPUT VOLTAGE

