

DOLBY PRO LOGIC SURROUND DECODER

■ GENERAL DESCRIPTION

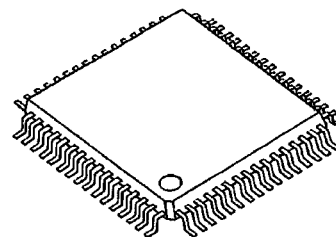
The NJW1102 is a Dolby Pro Logic Surround Decoder including modified Dolby B-Type noise reduction circuit, input auto-balance controller, noise sequencer, adaptive matrix, center and surround channel level trimmers, serial data interface and others. All of internal status and the balance of surround speakers are controlled by serial data. It performs the complete Dolby Pro Logic Surround function and surround function, such as Hall, Matrix, Simulated and others combine with the digital delay NJU9702.

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■ PACKAGE OUTLINE



NJW1102F61

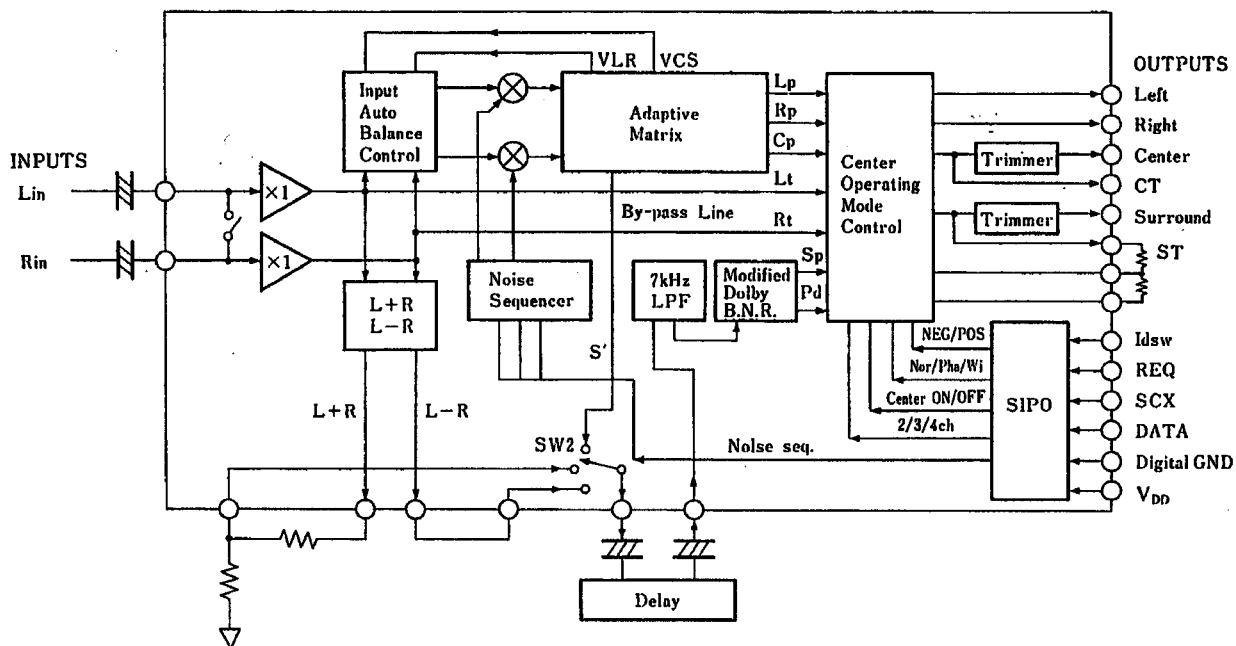
■ FEATURES

- Operating Voltage
 - Analog Block $V_{CC}=9-13$ or $\pm 5V$
 - Digital Block $V_{DD}=5V$
- Dolby Operating Level 300mVrms
- Center and Surround Channel Level Trimmers
 - 15 to +15dB/ 1dB step (-15dB to 3dB/ 1dB step in Pro Logic Mode)
- Internal Mode Control Switch
- Bi-CMOS Technology
- Package Outline TQFP64

■ FUNCTIONS

- Input Auto-Balance
- Noise Generator And Sequencer
- Adaptive Matrix
- Pro Logic Surround Mode Control : 4/3, Center ON/OFF, Normal/Phantom/Wideband
- 7kHz Low-pass Filter and Modified Dolby B Type Noise Reduction
- Center and Surround Channel Level Trimmer
- Other Surround Mode Control : S'Out Selector, Mixer And Mute Functions
- Serial Data Interface

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	13.0	V
	V _{DD}	6.5	V
Power Dissipation	P _D	700	mW
Operating Temperature Range	T _{opr}	-20 ~ +75	°C
Storage Temperature Range	T _{stg}	-40 ~ +125	°C

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{CC}=10V, V_{DD}=5V, 0dB reference is 300mVrms/1kHz at C-OUT with C ch trimmer being 0dB, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Overall						
Operating Voltage	V _{CC}		9	10	13	V
	V _{DD}		4.5	5.0	6.5	V
Operating Current	I _{CC}	No Signal		35	45	mA
	I _{DD}	No Signal		0.6	1.5	mA
Reference Voltage	V _{ref}	No Signal	3.6	4.0	4.4	V
Threshold Voltage	V _{thh}	Digital Input High Level	0.7V _{DD}		V _{DD}	V
	V _{thl}	Digital Input Low Level	0.0		0.3V _{DD}	V
Input short switch						
Resistance at input short	R _{on}			150	500	Ω
Switch Crosstalk	SC	V _{in} =0dB, f=1kHz, R _m =600 Ω		−100		dB
Input Auto Balance						
Capture Range	CPR			±5		dB
Error Correction	CER			±4		dB
Adaptive Matrix						
Output Level Accuracy Relative to C ch	△Vol	L, R, S' ch out	−0.5	0.0	0.5	dB
Matrix Rejection Relative	MR	L, R, C, S' ch out	25	40		dB
Headroom	HRAM	V _{CC} =9V at THD=1%	15	17		dB
Total Harmonic Distortion	THDAM	L, R, C, S' ch out at 4ch mode		0.050	0.200	%
		L, R ch out at 2ch mode		0.002	0.050	%
Signal to Noise Ratio	SNAM	R _g =0, weighted:CCIR/ARM at 4ch mode	75	80		dB
		L, R ch out at 2ch mode	93	100		dB
Noise Sequencer						
Output Noise Level	V _{no}		−15	−12.5	−10.0	dB
Output Noise Level Accuracy Relative to C ch	△V _{no}	L, R, S' ch out	−0.5	0.0	0.5	dB

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
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Modified Noise B Type Noise Reduction

(0dBd reference is input level at NR-IN when S out is adjusted to 0dB (300mVrms/100Hz) with S ch trimmer level being 0dB)

Voltage Gain	VGNR	Vin=0dBd, f=100Hz		9.5		dB
Decode Response 1	DEC1	Vin=0dBd, f=1.0kHz	-1.6	-0.1	1.4	dB
Decode Response 2	DEC2	Vin=-15dBd, f=1.4kHz	-3.0	-1.5	0.0	dB
Decode Response 3	DEC3	Vin=-20dBd, f=1.4kHz	-4.9	-3.4	-1.9	dB
Decode Response 4	DEC4	Vin=-40dBd, f=5.0kHz	-6.8	-5.3	3.8	dB
Total Harmonic Distortion	THDNR	Vin=0dBd, f=1kHz		0.070	0.300	%
Headroom	HRNR	Vin=9V at THD=1%	15	17		dB
Signal to Noise	SNNR	Rg=0, weighted : CCIR/ARM	73	78		dB

Other Surround

Total Harmonic Distortion	THDOS	Vin=0dB, f=1kHz L+R, L-R Output		0.050	0.200	%
Headroom	HROS	Vcc=9V at THD=1% L+R, L-R Output	15	17		dB
Signal to Noise Ratio	SNOS	Rg=0, weighted : CCIR/ARM L+R, L-R Output	75	80		dB
Adder Gain	AG			0		dB

C.S Channel Trimmer

Full Scale	FS	Digital Input=+15 or -15dB	+12	±15	±18	dB
Gain Accuracy at -6dB		Digital Input=-6dB	-7	-6	-5	dB
Non Linearity (Note 1)	NL	Digital Input=±1, 2, 4, 8dB	-0.5	0.0	0.5	dB

Control Timing

SCK Clock Width	t1	SCK	50			μS
REQ Set-up Time	t2	REQ-SCK	25			μS
REQ Hold Time	t3	REQ-SCK	25			μS
Data Set-up Time	t4	SCK-DATA	25			μS
Data Hold Time	t5	SCK-DATA	25			μS

(Note 1) $NL = A \cdot B / D - C$

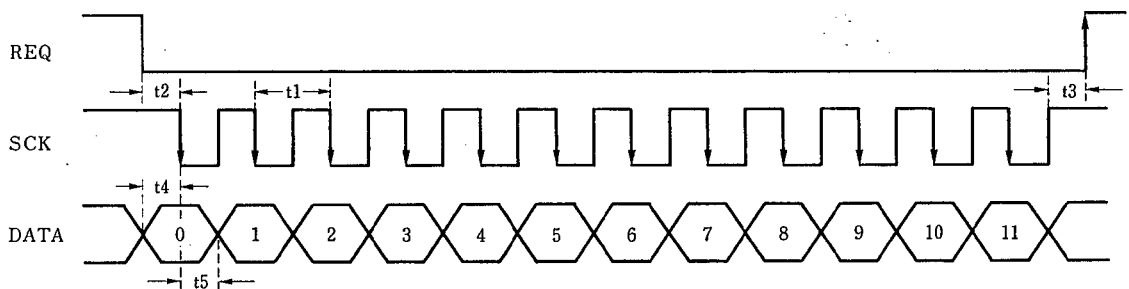
A : Measured gain value in full scale

B : Digital input value

C : Measured gain value of digital input

D : Full scale value

(Note 2) Control Timing



MEMO

[CAUTION]

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