

High-Voltage Switchmode Regulator

DESCRIPTION

The Si9104 high-voltage switchmode regulator is a monolithic BiC/DMOS integrated circuit which contains most of the components necessary to implement a high-efficiency DC-to-DC converter up to 3 W. It can either be operated from a low-voltage DC supply, or directly from a 10 to 120 V unregulated DC power source.

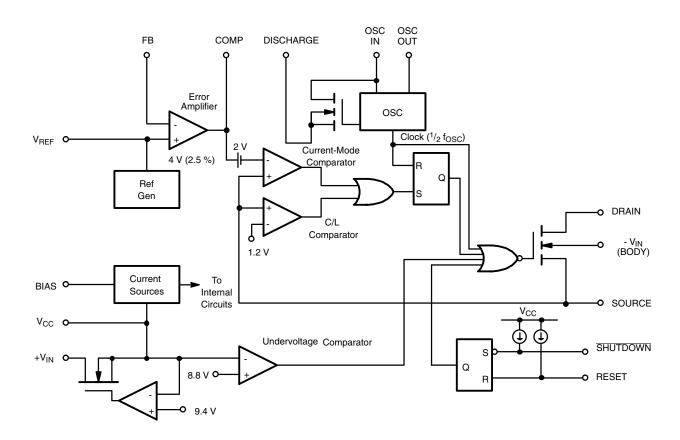
This device may be used with an appropriate transformer to implement most single-ended isolated power converter topologies (i.e., flyback and forward).

The Si9104 is available in a 16-pin wide-body SOIC and is specified over the D suffix (- 40 to 85 °C) temperature range.

FEATURES

- 10 to 120 V Input Range
- · Current-Mode Control
- On-Chip 200 V, 5 Ω MOSFET Switch
- SHUTDOWN and RESET
- High Efficiency Operation (> 80 %)
- · Internal Start-Up Circuit
- Internal Oscillator (1 MHz)

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS							
Parameter		Limit	Unit				
Voltages Referenced to - V _{IN} (V _{CC} < + V	_{IN} + 0.3 V)		·				
V _{CC}		15					
+V _{IN}	120 V						
V_{DS}	200						
I _D (Peak) (Note: 300 μs pulse, 2 % Duty C	2	Α					
I _D (rms)	250	mA					
Logic Inputs (RESET, SHUTDOWN, OSC	- 0.3 to V _{CC} + 0.3						
Linear Inputs (FEEDBACK, SOURCE)	- 0.3 to 7	v					
HV Pre-Regulator Input Current (continuous)		3	mA				
Storage Temperature		- 65 to 125					
Operating Temperature		- 40 to 85 °C					
Junction Temperature (T _J)		150					
Power Dissipation (Package) ^a	16-Pin Plastic Wide-Body SOIC ^b	900	mW				
Thermal Impedance (Θ_{JA})	16-Pin Plastic Wide-Body SOIC	140	°C/W				

Notes:

- a. Device Mounted with all leads soldered or welded to PC board.
- b. Derate 7.2 mW/°C above 25 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE					
Parameter	Limit	Unit			
Voltages Referenced to - V _{IN}					
V _{CC}	10 to 13.5	V			
+ V _{IN}	10 to 120	7 v			
f _{OSC}	40 kHz to 1 MHz				
R _{OSC}	25 kΩ to 1 MΩ				
Linear Inputs	0 to 7	V			
Digital Inputs	0 to V _{CC}	\ \ \			

SPECIFICATIONS ^a							
		Test Conditions Unless Otherwise Specified DISCHARGE = - V _{IN} = 0 V	[nits 40 to 85 °0	0	
Parameter	Symbol	$V_{CC} = 10 \text{ V}, + V_{IN} = 48 \text{ V}$ $R_{BIAS} = 390 \text{ k}\Omega, R_{OSC} = 330 \text{ k}\Omega$	Temp ^b	Min ^d	Тур ^с	Max ^d	Unit
Reference							
Output Voltage	V _R	OSC IN = - V_{IN} (OSC Disabled) $R_L = 10 \text{ M}\Omega$	Room Full	3.92 3.85	4.0	4.08 4.15	V
Output Impedance ^e	Z _{OUT}		Room	15	30	45	kΩ
Short Circuit Current	I _{SREF}	V _{REF} = - V _{IN}	Room	70	100	130	μΑ
Temperature Stability ^e	Т		Full		0.25	1.0	mV/°C
Long Term Stability ^e	T _{REF}	t = 1000 hrs., T _A = 125 °C	Room		5	25	mV
Oscillator							
Maximum Frequency ^e	f _{MAX}	$R_{OSC} = 0$	Room	1	3		MHz
lottical A company	f	$R_{OSC} = 330 \text{ k}\Omega^f$	Room	80	100	120	kHz
Initial Accuracy	[†] osc	$R_{OSC} = 150 \text{ k}\Omega^f$	Room	160	200	240	K⊓Z
Voltage Stability	Δf/f	$\Delta f/f = f(13.5 \text{ V}) - f(10 \text{ V})/f(10 \text{ V})$	Room	4	10	15	%
Temperature Coefficient ^e	T _{OSC}		Full		200	500	ppm/°C

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		Test Conditions Unless Otherwise Specified	Г		nits 40 to 85 °0	С	
Parameter	Symbol	DISCHARGE = $-V_{IN} = 0 V$ $V_{CC} = 10 V$, $+V_{IN} = 48 V$ $R_{BIAS} = 390 k\Omega$, $R_{OSC} = 330 k\Omega$	Tempb	Min ^d	Typ ^c	Max ^d	Unit
Error Amplifier	Cymbol	TIBIAS COUNTY TOSC COUNTY	Temp		ן יאָף	IWIGA	01111
	Τ., Ι	FB Tied to COMP	Ι_ Ι		l		
Feedback Input Voltage	V _{FB}	OSC IN = - V _{IN} (OSC Disabled)	Room	3.96	4.00	4.04	V
Input BIAS Current	I _{FB}	OSC IN = - V _{IN} , V _{FB} = 4 V	Room		25	500	nA
Input OFFSET Voltage	V _{OS}		Room		± 15	± 40	m۷
Open Loop Voltage Gain ^e	A _{VOL}	OSC IN = - V _{IN} (OSC Disabled)	Room	60	80		dB
Unity Gain Bandwidth ^e	BW	COO IIV = VIN (COO DISABICA)	Room	0.7	1		MH
Dynamic Output Impedance ^e	Z _{OUT}		Room		1000	2000	Ω
Output Current	la	Source (V _{FB} = 3.4 V)	Room		- 2.0	- 1.4	m/
Output Current	IOUT	Sink (V _{FB} = 4.5 V)	Room	0.12	0.15		m/
Power Supply Rejection	PSRR	10 V ≤ V _{CC} ≤ 13.5 V	Room	50	70		dE
Current Limit							
Threshold Voltage	V _{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC} V_{FB} = 0 V	Room	1.0	1.2	1.4	V
Delay to Output	t _d	R_L = 100 Ω from DRAIN to V_{CC} V_{SOURCE} = 1.5 V, See Figure 1	Room		100	200	ns
Pre-Regulator/Start-Up							
Input Voltage	+ V _{IN}	I _{IN} = 10 μA	Room	120			V
Input Leakage Current	+ I _{IN}	V _{CC} ≥ 10 V	Room			10	μΑ
Pre-Regulator Start-Up Current	I _{START}	Pulse Width ≤ 300 μs, V _{CC} = 7 V	Room	8	15		m/
V _{CC} Pre-Regulator Turn-Off Threshold Voltage	V _{REG}	I _{PRE-REGULATOR} = 10 μA	Room	7.8	9.4	9.8	
Undervoltage Lockout	V _{UVLO}	R_L = 100 Ω from DRAIN to V_{CC} See Detailed Description	Room	7.0	8.8	9.3	٧
V _{REG} - V _{UVLO}	V _{DELTA}	•	Room	0.3	0.6		1
Supply	, -==::- ,				L		
Supply Current	I _{CC}		Room	0.45	0.6	1.0	m
Bias Current	I _{BIAS}		Room	10	15	20	μ
Logic					L		
SHUTDOWN Delay ^e	t _{SD}	V _{SOURCE} = - V _{IN} , See Figure 2	Room		50	100	
SHUTDOWN Pulse Widthe	t _{SW}		Room	50			
RESET Pulse Width ^e	t _{RW}	See Figure 3.	Room	50			ns
Latching Pulse Width ^e SHUTDOWN and RESET Low	t _{LW}	See Figure 3.	Room	25			
Input Low Voltage	V _{IL}		Room			2.0	,,
Input High Voltage	V _{IH}		Room	8.0			V
Input Current Input Voltage High	I _{IH}	$V_{IN} = V_{CC}$	Room		1	5	
Input Current Input Voltage Low	I _{IL}	V _{IN} = 0 V	Room	- 35	- 25		μΑ
MOSFET Switch	, ,,,						
Breakdown Voltage	V _{BR(DSS)}	I _{DRAIN} = 100 μA	Full	200	220		V
Drain-Source On Resistance ^g	r _{DS(on)}	I _{DRAIN} = 100 mA	Room		3	5	Ω
Drain Off Leakage Current	I _{DSS}	V _{DRAIN} = 150 V	Room		5	10	μA
Drain Capacitance ^e	C _{DS}	DIDIN	Room		35		pF

Notes:

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. Room = 25 °C, Full = as determined by the operating temperature suffix.
 c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f. C_{STRAY} at OSC IN \leq 5 pF. g. Temperature coefficient of $r_{DS(on)}$ is 0.75 % per °C, typical.

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TIMING WAVEFORMS

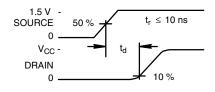


Figure 1.

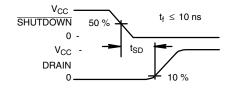


Figure 2.

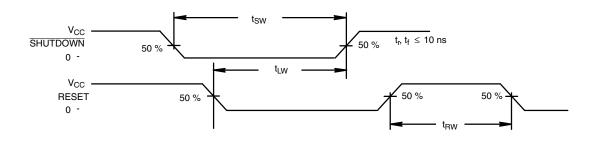


Figure 3.

TYPICAL CHARACTERISTICS

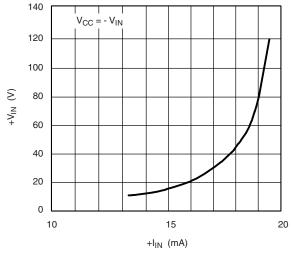


Figure 4. + V_{IN} vs. + I_{IN} at Start-Up

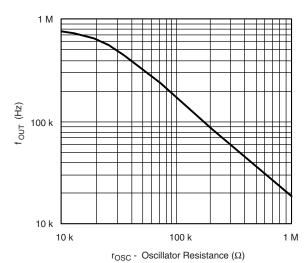
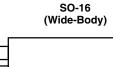
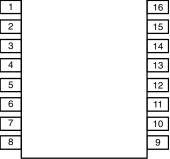


Figure 5. Output Switching Frequency vs. Oscillator Resistance







Top View

Order Number: Si9104DW

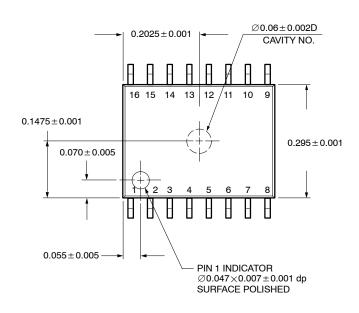
Function		Pin Number				
	14-Pin Plastic DIP	16-Pin SOIC	20-Pin PLCC			
SOURCE	4	1	7			
- V _{IN}	5	2	8			
V _{CC}	6	4	9			
OSC _{OUT}	7	5	10			
OSC _{IN}	8	6	11			
DISCHARGE	9	7	12			
V _{REF}	10	8	14			
SHUTDOWN	11	9	16			
RESET	12	10	17			
COMP	13	11	18			
FB	14	12	20			
BIAS	1	13	2			
+ V _{IN}	2	14	3			
DRAIN	3	16	5			
NC		3, 15	1, 4, 6,13, 15, 1			

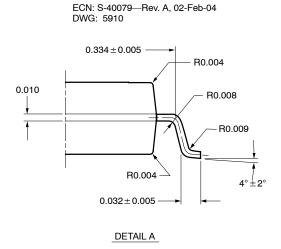
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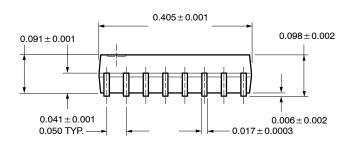
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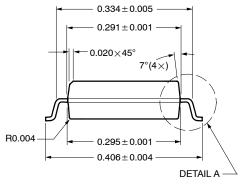


SOIC (WIDE-BODY): 16-LEAD (POWER IC ONLY)









All Dimensions In Inches



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