- Package Options Include Plastic Small Outline Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic DIPs
- Input and Output Latches with Active-High Enables
- Fast Compare to Zero
- Arithmetic and Logical Comparison
- Open-Collector P = Q Output

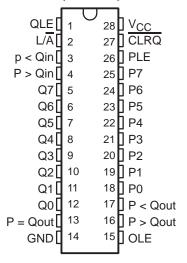
description

These Advanced Schottky devices are capable of performing high-speed arithmetic or logical comparisons on two 8-bit binary or two's complement words. Three fully decoded decisions about words P and Q are externally available at the outputs. These devices are fully expandable to any word length by connecting the totem pole P>Q and P<Q outputs of each stage to the P>Q and P<Q inputs of the next higher-order stage. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words. The opencollector P=Q output may be wire-ANDed together.

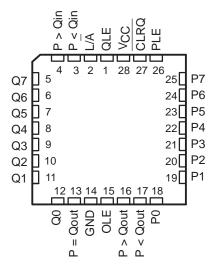
Both input words P and Q plus all three outputs (P>Q, P<Q, and P=Q) are equipped with latches to provide the designer with temporary data storage for avoiding race conditions. The enable circuitry is implemented with minimal delay times to enhance performance when the devices are cascaded for longer word lengths. Each latch is transparent when the appropriate latch enable, PLE, QLE, or OLE is high.

The enable inputs PLE and QLE and data inputs P and Q utilize pnp input transistors to reduce the low-level input current requirement to typically –0.25 mA, which minimizes loading effects.

SN54AS866 . . . JD PACKAGE SN74AS866A . . . N PACKAGE (TOP VIEW)



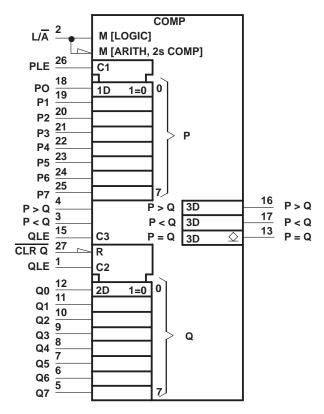
SN54AS866 . . . FK PACKAGE SN74AS866A . . . FN PACKAGE (TOP VIEW)



The Q register may be cleared to zero for a fast comparison of the P word to zero.

The SN54AS866 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AS866A is characterized for operation from 0°C to 70°C.

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic) OLE ⊃₇ <u>P7</u>=Q7 PLE 25 **P7** 1D **P7** P7 P6 ²⁴ P6 P5 P3 P5 P3=Q3 P4 P4 P4 21 Р3 P3 P3 C1 P2 = 20 P2 1D P<Q P2 16 P>Q 13 P=Q Р1 **P**1 P1 P0=Q0 P0 18 PO. $\frac{\overline{\mathsf{CLRQ}}}{\mathsf{QLE}} \frac{27}{1}$ _C1 Q7 Q7 Q7 Q6 Q6 Q6 Q5 Q5 Q5 Q4 Q4 Q3 4MSB= Q3 Q3 Q2 Q2 Q2 Q1 Q1 Q1 Q0 Q0 Q0 P>QIN 4/3 P<1/1 2/4 L/A Arith Logic



SN54AS866, SN74AS866A 8-BIT MAGNITUDE COMPARATORS

SDAS183A - DECEMBER 1982 - REVISED JUNE 1990

FUNCTION TABLE

COMPARISON	1/4	DATA INPUTS	INP	UTS	OUTPUTS				
COMPARISON	L/A	P0-P7, Q0-Q7	P>Q	P <q< th=""><th>P>Q</th><th>P<q< th=""><th>P=Q</th></q<></th></q<>	P>Q	P <q< th=""><th>P=Q</th></q<>	P=Q		
Logical	Н	P>Q	Х	Х	Н	L	L		
Logical	Н	P <q< td=""><td>Х</td><td>Х</td><td>L</td><td>Н</td><td>L</td></q<>	Х	Х	L	Н	L		
Logical	Н	P=Q	L	L	L	L	Н		
Logical	Н	P=Q	L	Н	L	Н	L		
Logical	Н	P=Q	Н	L	Н	L	L		
Logical	Н	P=Q	Н	Н	Н	Н	L		
Arithmetic	L	P AG Q	Х	Х	Н	L	L		
Arithmetic	L	Q AG P	Х	Х	L	Н	L		
Arithmetic	L	P=Q	L	L	L	L	Н		
Arithmetic	L	P=Q	L	Н	L	Н	L		
Arithmetic	L	P=Q	Н	L	Н	L	L		
Arithmetic	L	P=Q	Н	Н	Н	Н	L		

AG = arithmetically greater than

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}		7 V
Input voltage		7 V
Operating free-air temperature range:	SN54AS866	-55°C to 125°C
	SN74AS866A	0°C to 70°C
Storage temperature range		-65°C to 150°C

recommended operating conditions

		SN54AS866		SN74AS866A			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2	, G	1115	2			V
VIL	Low-level input voltage		V bby.	0.8			0.8	V
ІОН	High-level output current, all outputs except P=Q		,C,	-2			-2	mA
Vон	High-level output voltage, P=Q output	200		5.5			5.5	V
loL	Low-level output current	8,		20			20	mA
t _{su}	Setup time to PLE, OLE, OLE↓	2			2			ns
t _h	Hold time after PLE, QLE, OLE↓	4		·	4			
tA	Operating free-air temperature	-55		125	0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	ARAMETER	TEST CONDITIONS		SN	54AS866	5	SN	UNIT		
	AKAIVIETEK			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK		$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$			-1.2			-1.2	V
Vон	P>Q, P <q< td=""><td>$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$</td><td>$I_{OH} = -2 \text{ mA}$</td><td>V_{CC}-2</td><td></td><td></td><td>V_{CC}-2</td><td></td><td></td><td></td></q<>	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -2			V _{CC} -2			
IOH	P=Q only	$V_{CC} = 4.5 \text{ V},$	V _{OH} = 5.5 V			0.25			0.25	mA
VOL	-	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 20 \text{ mA}$		0.35	0.5		0.35	0.5	V
Ц		$V_{CC} = 5.5 \text{ V},$	V _I = 7 V		16	0.1			0.1	mA
1	L/A, OLE		\/. 0.7\/		-O.E.	40			40	
ΙН	Others	vCC = 5.5 v,	V _I = 2.7 V		< Y	20			20	μΑ
	L/A, OLE,			000	,					
	P>Qin,			PRODUC		-4			-4	
ηL	P <qin< td=""><td>$V_{CC} = 5.5 V$,</td><td>$V_{I} = 0.4 \ V$</td><td>8.</td><td></td><td></td><td></td><td></td><td></td><td>mA</td></qin<>	$V_{CC} = 5.5 V$,	$V_{I} = 0.4 \ V$	8.						mA
	CLRQ	1				-2			-2	
	P, Q, PLE, QLE	1			- 0.25	-1		- 0.25		
IO [‡]		$V_{CC} = 5.5 \text{ V},$	V _O = 2.25 V	-20		-112	-20		-112	mA
ICC		$V_{CC} = 5.5 \text{ V},$	See Note 1		160	240		160	240	mA

NOTE 1: I_{CC} is measured with all inputs high except L/\overline{A} , which is low.

switching characteristics (see Note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω , T_A = MIN to MAX§					
		·	SN54AS866			SN74AS866A			
			MIN	TYP	MAX	MIN	TYP	MAX	
^t PLH	L/Ā		1	8.5	14	1	8.5	19	ns
t _{PHL}			1	7.5	14	1	7	13	115
^t PLH	P <q, p="">Q</q,>		1	5	10	1	5	8	no
^t PHL	F <q, f="">Q</q,>	P <q, p="">Q</q,>	1	5.5	10	1	5.5	8	ns
^t PLH	Any P or Q]	1	13.5	21	1	13.5	17.5	
t _{PHL}	Data Input		0	10	17	1	10	15	ns
^t PLH	CLRQ]	1	16	21	1	16	20	ns
t _{PHL}	OLNQ		1	12	17	1	12	16	113

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 280 Ω , T_A = MIN to MAX§						UNIT
		, ,	SN54AS866			SN74AS866A			1
			MIN	TYP [†]	MAX	MIN	TYP†	MAX	
^t PLH	P <q,< td=""><td>Б. О</td><td>1</td><td>6.5</td><td>12</td><td>1</td><td>6.5</td><td>16</td><td></td></q,<>	Б. О	1	6.5	12	1	6.5	16	
tpHL	P>Q	P=Q	1	8	14	1	8	14	ns
^t PLH	Any P or Q	P=Q	1	10	15	1	10	17	
tPHL	Data Input	P=Q	10	9	14	1	9	14	ns
^t PLH	CLRQ	P=Q	29	12	17	1	12	24	ns
t _{PHL}	CLRQ	r=Q	1	13	18	1	13	21	115

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1 of the ALS/AS Logic Data Book, 1986.



[‡] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit, IOS.

[§] For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.

TYPICAL APPLICATION DATA

This sequence of comparisons illustrates how the \overline{CLRQ} function can be used to perform dual comparisons of the varying P terms (P0, P1, etc.). When \overline{CLRQ} is high, the P term is compared to the Q term. When \overline{CLRQ} is taken low, the P term is compared to zero. This or similar sequences can enhance performance and reduce package count to perform value range checks.

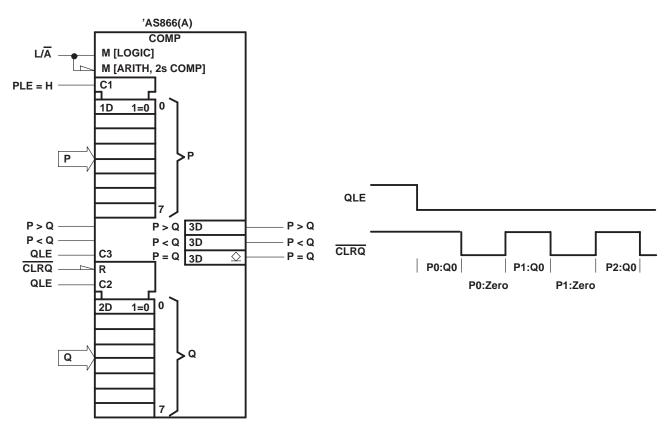


Figure 1. Magnitude Comparisons Combined With Quick Comparisons to Zero (Range Verifications)

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