

# INA121

## FET-Input, Low Power INSTRUMENTATION AMPLIFIER

### FEATURES

- **LOW BIAS CURRENT:**  $\pm 4\text{pA}$
- **LOW QUIESCENT CURRENT:**  $\pm 450\mu\text{A}$
- **LOW INPUT OFFSET VOLTAGE:**  $\pm 200\mu\text{V}$
- **LOW INPUT OFFSET DRIFT:**  $\pm 2\mu\text{V}/^\circ\text{C}$
- **LOW INPUT NOISE:**  
 $20\text{nV}/\sqrt{\text{Hz}}$  at  $f = 1\text{kHz}$  ( $G = 100$ )
- **HIGH CMR:** 106dB
- **WIDE SUPPLY RANGE:**  $\pm 2.25\text{V}$  to  $\pm 18\text{V}$
- **LOW NONLINEARITY ERROR:** 0.001% max
- **INPUT PROTECTION TO  $\pm 40\text{V}$**
- **8-PIN DIP AND SO-8 SURFACE MOUNT**

### APPLICATIONS

- **LOW-LEVEL TRANSDUCER AMPLIFIERS**  
Bridge, RTD, Thermocouple
- **PHYSIOLOGICAL AMPLIFIERS**  
ECG, EEG, EMG, Respiratory
- **HIGH IMPEDANCE TRANSDUCERS**
- **CAPACITIVE SENSORS**
- **MULTI-CHANNEL DATA ACQUISITION**
- **PORTABLE, BATTERY OPERATED SYSTEMS**
- **GENERAL PURPOSE INSTRUMENTATION**

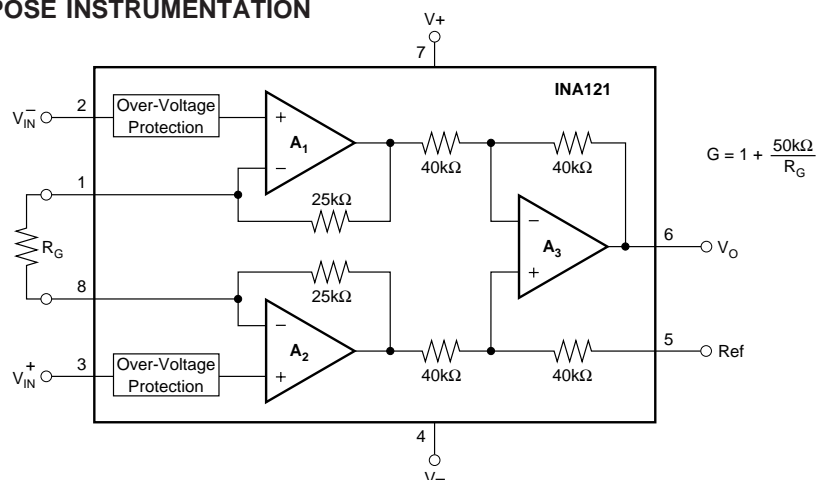
### DESCRIPTION

The INA121 is a FET-input, low power instrumentation amplifier offering excellent accuracy. Its versatile three-op amp design and very small size make it ideal for a variety of general purpose applications. Low bias current ( $\pm 4\text{pA}$ ) allows use with high impedance sources.

Gain can be set from 1V to 10,000V/V with a single external resistor. Internal input protection can withstand up to  $\pm 40\text{V}$  without damage.

The INA121 is laser-trimmed for very low offset voltage ( $\pm 200\mu\text{V}$ ), low offset drift ( $\pm 2\mu\text{V}/^\circ\text{C}$ ), and high common-mode rejection (106dB at  $G = 100$ ). It operates on power supplies as low as  $\pm 2.25\text{V}$  ( $+4.5\text{V}$ ), allowing use in battery operated and single 5V systems. Quiescent current is only  $450\mu\text{A}$ .

Package options include 8-pin plastic DIP and SO-8 surface mount. All are specified for the  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  industrial temperature range.



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# SPECIFICATIONS: $V_S = \pm 15V$

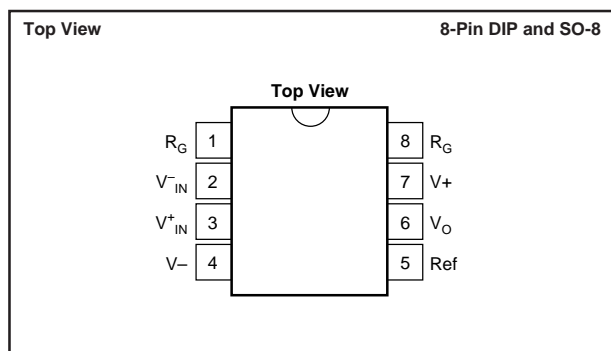
At  $T_A = +25^\circ C$ ,  $V_S = \pm 15V$ ,  $R_L = 10k\Omega$ , and  $I_A$  reference = 0V, unless otherwise noted.

| PARAMETER   | CONDITIONS   | INA121P, U                 |   |   | INA121PA, UA |   |  | UNITS   |
|---|--|----------------------------|---|---|--------------|---|--|---|
|   |  | MIN                        | TYP   | MAX   | MIN          | TYP   | MAX  |   |
| <b>INPUT</b><br>Offset Voltage, RTI<br>vs Temperature<br>vs Power Supply<br>Long-Term Stability<br>Impedance, Differential<br>Common-Mode<br>Input Voltage Range<br>Safe Input Voltage<br>Common-Mode Rejection | $V_S = \pm 2.25V$ to $\pm 18V$<br><br>$V_O = 0V$<br><br>$V_{CM} = -12.5V$ to $13.5V$<br>$G = 1$<br>$G = 10$<br>$G = 100$<br>$G = 1000$   |                            | $\pm 200 \pm 200/G$<br>$\pm 2 \pm 2/G$<br>$\pm 5 \pm 20/G$<br>$\pm 0.5$<br>$10^{12} \parallel 1$<br>$10^{12} \parallel 12$<br>See Text and Typical Curves | $\pm 500 \pm 500/G$<br>$\pm 5 \pm 20/G$<br>$\pm 50 \pm 150/G$<br><br><br>$\pm 40$ |              | $\pm 300 \pm 200/G$<br>*<br>*<br>*<br>*<br>*<br>* | $\pm 1000 \pm 1000/G$<br>$\pm 15 \pm 20/G$<br>*<br><br><br>* | $\mu V$<br>$\mu V/^\circ C$<br>$\mu V/V$<br>$\mu V/mo$<br>$\Omega \parallel pF$<br>$\Omega \parallel pF$<br><br>V<br>dB<br>dB<br>dB<br>dB |
| <b>BIAS CURRENT</b><br>vs Temperature<br>Offset Current<br>vs Temperature   | $V_{CM} = 0V$  |                            | $\pm 4$<br>See Typical Curve<br>$\pm 0.5$<br>See Typical Curve  | $\pm 50$  |              | *<br>*<br>*                                       | *<br><br><br>  | pA<br><br>pA  |
| <b>NOISE, RTI</b><br>Voltage Noise: $f = 10Hz$<br>$f = 100Hz$<br>$f = 1kHz$<br>$f = 0.1Hz$ to $10Hz$<br>Current Noise: $f = 1kHz$   | $R_S = 0\Omega$<br>$G = 100$<br>$G = 100$<br>$G = 100$<br>$G = 100$  |                            | 30<br>21<br>20<br>1<br>1  |   |              | *<br>*<br>*<br>*<br>*                             |  | $nV/\sqrt{Hz}$<br>$nV/\sqrt{Hz}$<br>$nV/\sqrt{Hz}$<br>$\mu Vp-p$<br>$fA/\sqrt{Hz}$  |
| <b>GAIN</b><br>Gain Equation<br>Range of Gain<br>Gain Error<br><br>Gain vs Temperature <sup>(1)</sup><br><br>Nonlinearity   | $V_O = -14V$ to $13.5V$<br>$G = 1$<br>$G = 10$<br>$G = 100$<br>$G = 1000$<br>$G = 1$<br>$G > 1$<br><br>$V_O = -14V$ to $13.5V$<br>$G = 1$<br>$G = 10$<br>$G = 100$<br>$G = 1000$ | 1                          | $1 + (50k\Omega/R_G)$<br><br>$\pm 0.01$<br>$\pm 0.03$<br>$\pm 0.05$<br>$\pm 0.5$<br>$\pm 1$<br>$\pm 25$   | 10,000<br><br>$\pm 0.05$<br>$\pm 0.4$<br>$\pm 0.5$<br>$\pm 10$<br>$\pm 100$       | *            | *<br><br>*<br>*<br>*<br>*<br>*                    | *<br><br>$\pm 0.1$<br>$\pm 0.5$<br>$\pm 0.7$<br>*<br>*       | V/V<br>V/V<br>%<br>%<br>%<br>%<br>ppm/ $^\circ C$<br>ppm/ $^\circ C$<br><br>% of FSR<br>% of FSR<br>% of FSR<br>% of FSR                  |
| <b>OUTPUT</b><br>Voltage: Positive<br>Negative<br>Positive<br>Negative<br>Capacitance Load Drive<br>Short-Circuit Current   | $R_L = 100k\Omega$<br>$R_L = 100k\Omega$<br>$R_L = 10k\Omega$<br>$R_L = 10k\Omega$   | $(V+) - 1.5$<br>$(V-) + 1$ | $(V+) - 0.9$<br>$(V-) + 0.15$<br>$(V+) - 0.9$<br>$(V-) + 0.25$<br>1000<br>$\pm 14$  |   | *            | *<br>*<br>*<br>*<br>*<br>*                        |  | V<br>V<br>V<br>V<br>pF<br>mA  |
| <b>FREQUENCY RESPONSE</b><br>Bandwidth, -3dB<br><br>Slew Rate<br>Settling Time, 0.01%<br><br>Overload Recovery  | $G = 1$<br>$G = 10$<br>$G = 100$<br>$G = 1000$<br>$V_O = \pm 10V$ , $G \leq 10$<br>$G = 1$ to $10$<br>$G = 100$<br>$G = 1000$<br>50% Input Overload                              |                            | 600<br>300<br>50<br>5<br>0.7<br>20<br>35<br>260<br>5  |   |              | *<br>*<br>*<br>*<br>*<br>*<br>*<br>*<br>*         |  | kHz<br>kHz<br>kHz<br>kHz<br>V/ $\mu s$<br>$\mu s$<br>$\mu s$<br>$\mu s$<br>$\mu s$  |
| <b>POWER SUPPLY</b><br>Voltage Range<br>Quiescent Current   | $I_O = 0V$   | $\pm 2.25$                 | $\pm 15$<br>$\pm 450$   | $\pm 18$<br>$\pm 525$   | *            | *<br>*  | *<br>*   | V<br>$\mu A$  |
| <b>TEMPERATURE RANGE</b><br>Specification<br>Operating<br>Storage<br>Thermal Resistance, $\theta_{JA}$<br>8-Lead DIP<br>SO-8 Surface Mount  |  | -40<br>-55<br>-55          |   | 85<br>125<br>125  | *<br>*<br>*  |   | *<br>*<br>*  | $^\circ C$<br>$^\circ C$<br>$^\circ C$<br><br>$^\circ C/W$<br>$^\circ C/W$  |

\* Specification same as INA121P, U.

NOTE: (1) Temperature coefficient of the "Internal Resistor" in the gain equation. Does not include TCR of gain-setting resistor,  $R_G$ .

## PIN CONFIGURATION



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

|   |                                   |
|---|-----------------------------------|
| Supply Voltage .....                    | $\pm 18V$                         |
| Analog Input Voltage Range .....        | $\pm 40V$                         |
| Output Short-Circuit (to ground) .....  | Continuous                        |
| Operating Temperature .....             | $-55^{\circ}C$ to $+125^{\circ}C$ |
| Storage Temperature .....               | $-55^{\circ}C$ to $+125^{\circ}C$ |
| Junction Temperature .....              | $+150^{\circ}C$                   |
| Lead Temperature (soldering, 10s) ..... | $+300^{\circ}C$                   |

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

## PACKAGE/ORDERING INFORMATION

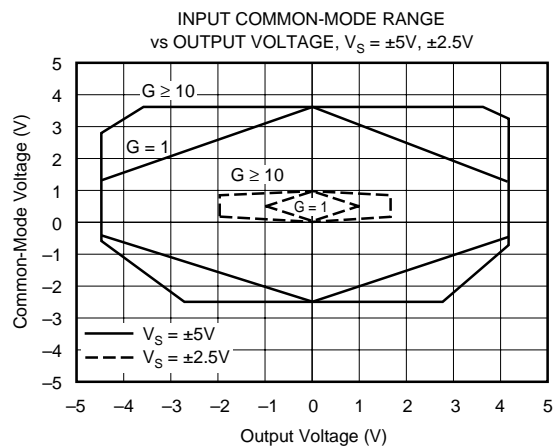
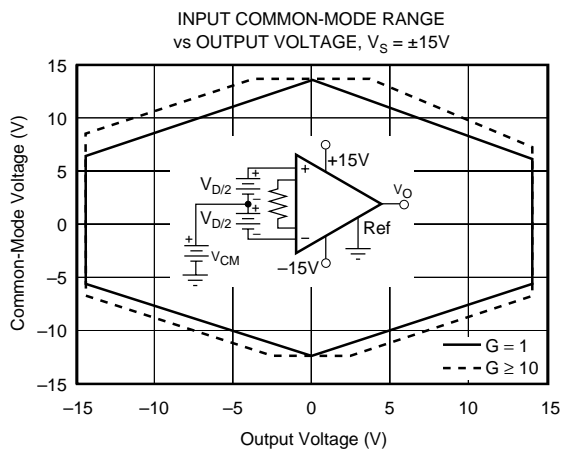
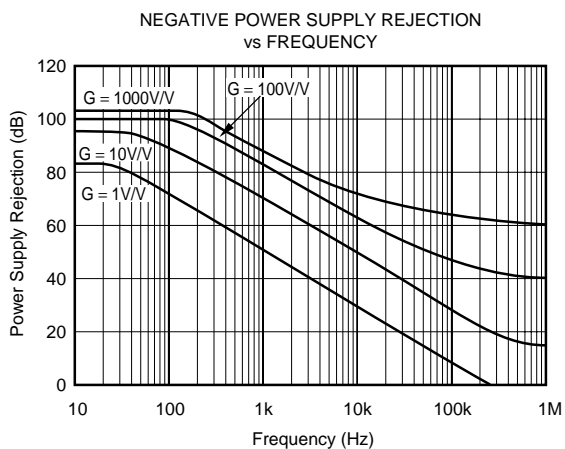
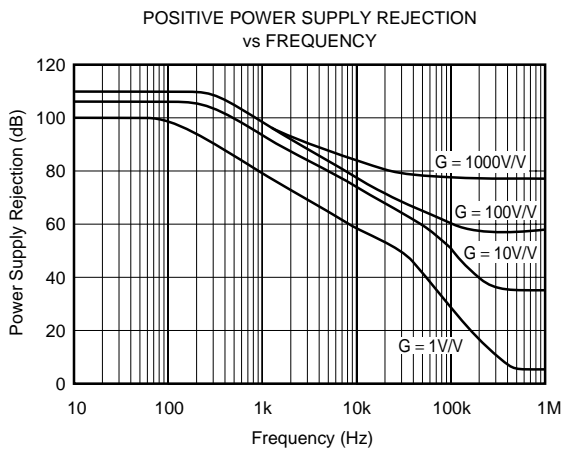
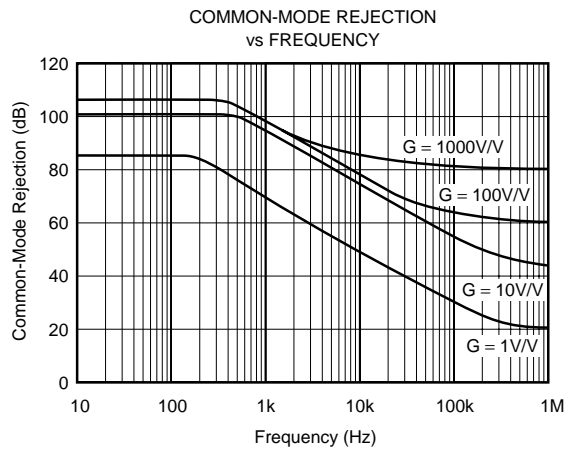
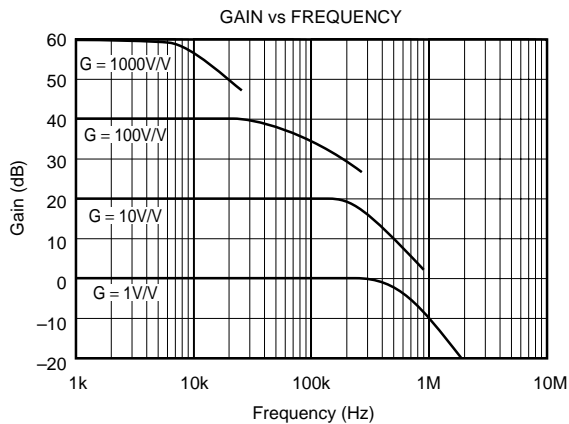
| PRODUCT  | PACKAGE            | PACKAGE DRAWING NUMBER(1) | SPECIFIED TEMPERATURE RANGE      | PACKAGE MARKING | ORDERING NUMBER(2) | TRANSPORT MEDIA |
|----------|--------------------|---------------------------|----------------------------------|-----------------|--------------------|-----------------|
| Single   |                    |                           |                                  |                 |                    |                 |
| INA121P  | 8-Pin DIP          | 006                       | $-40^{\circ}C$ to $+85^{\circ}C$ | INA121P         | INA121P            | Rails           |
| INA121PA | 8-Pin DIP          | 006                       | $-40^{\circ}C$ to $+85^{\circ}C$ | INA121PA        | INA121PA           | Rails           |
| INA121U  | SO-8 Surface-Mount | 182                       | $-40^{\circ}C$ to $+85^{\circ}C$ | INA121U         | INA121U            | Rails           |
| "        | "                  | "                         | "                                | "               | INA121U/2K5        | Tape and Reel   |
| INA121UA | SO-8 Surface-Mount | 182                       | $-40^{\circ}C$ to $+85^{\circ}C$ | INA121UA        | INA121UA           | Rails           |
| "        | "                  | "                         | "                                | "               | INA121UA/2K5       | Tape and Reel   |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "INA121U/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

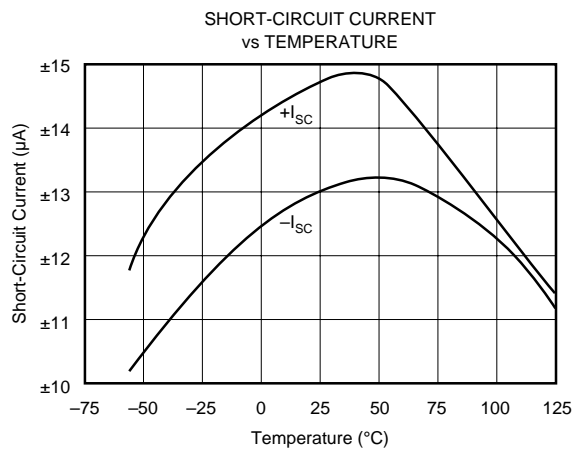
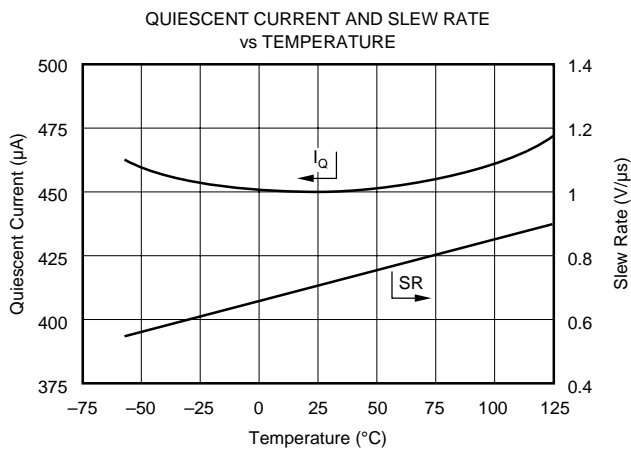
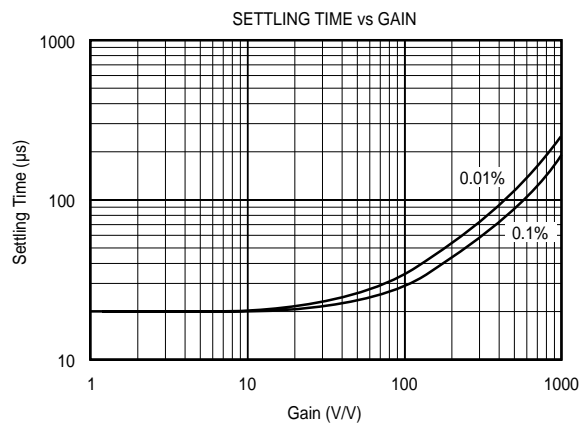
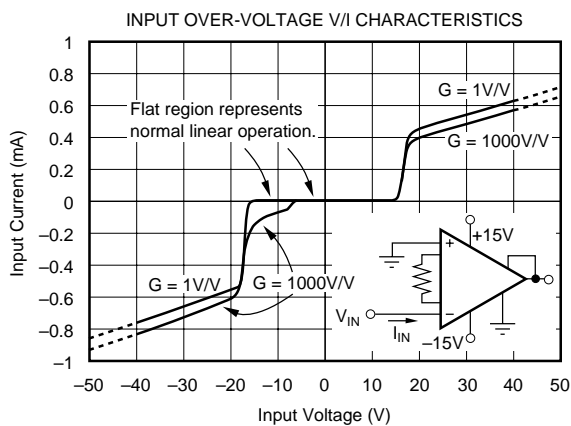
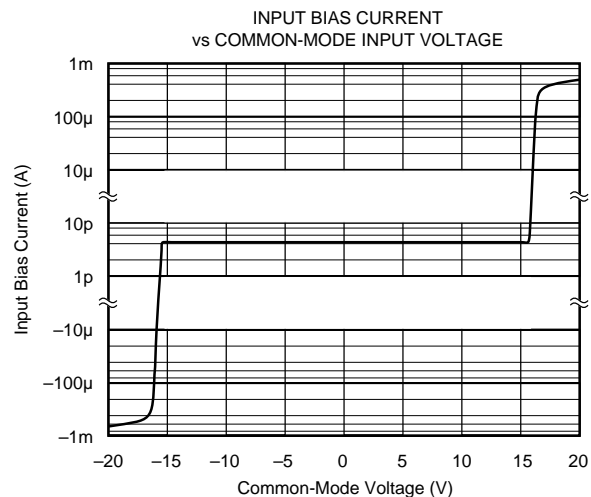
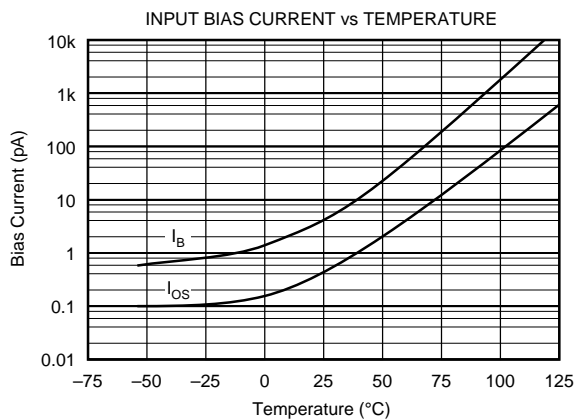
# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.



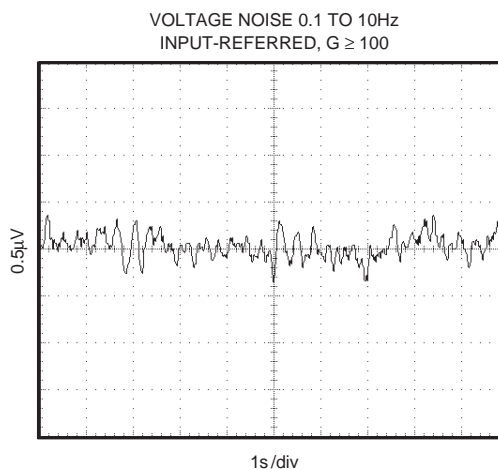
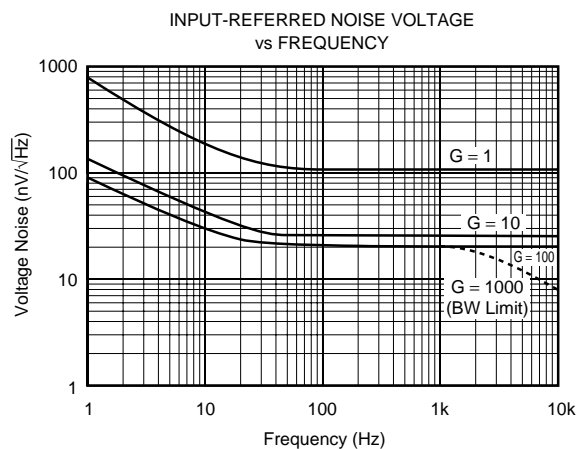
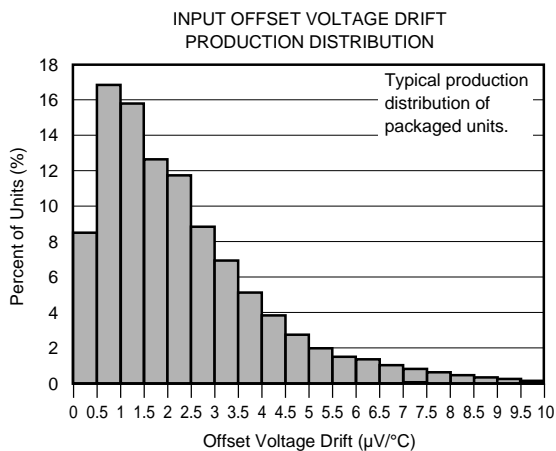
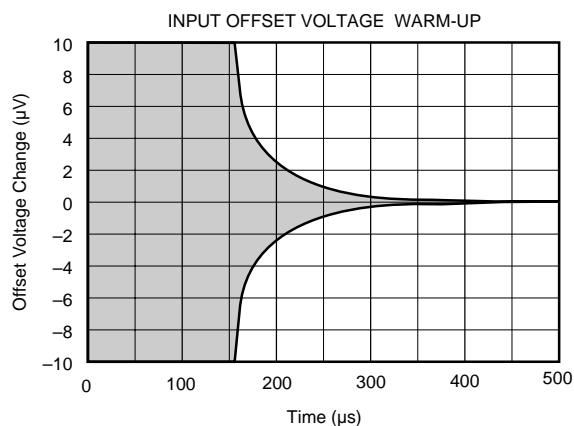
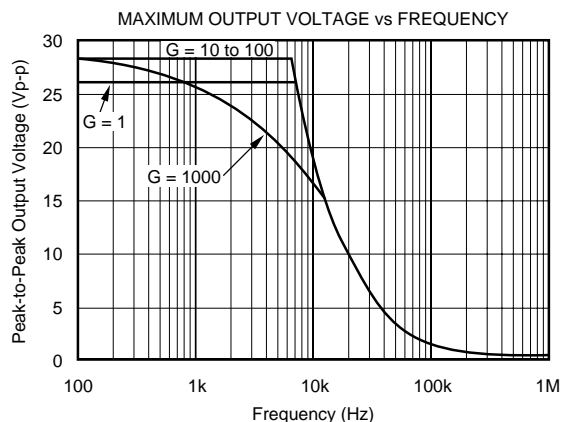
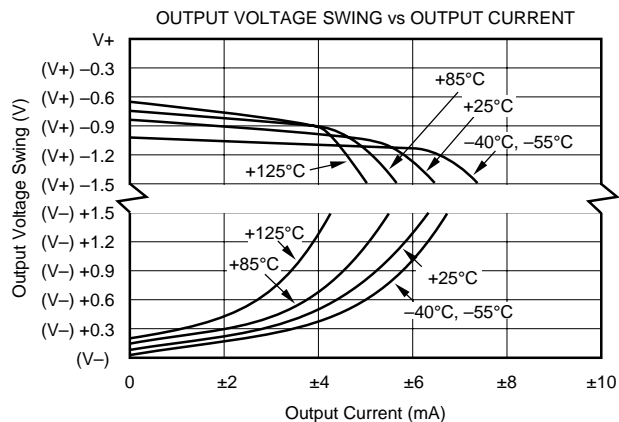
# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.



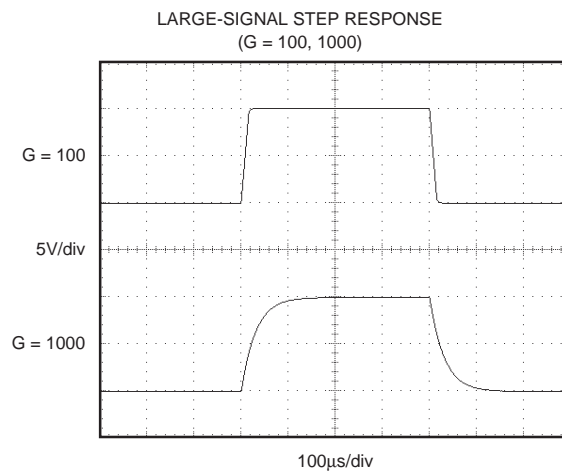
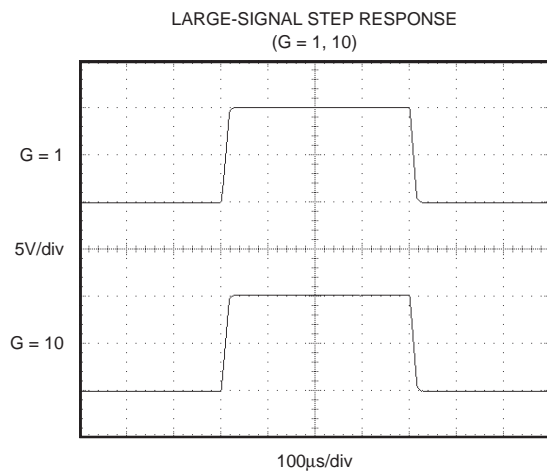
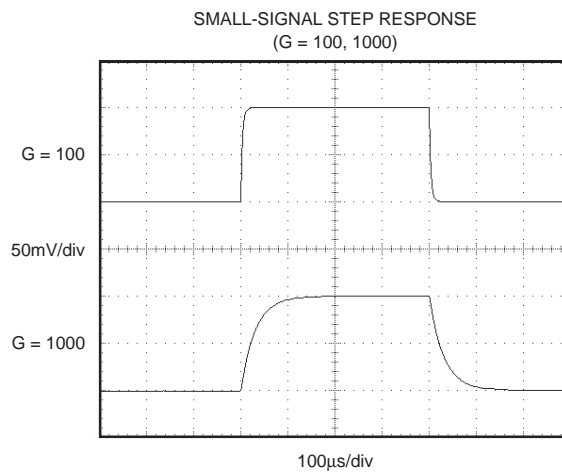
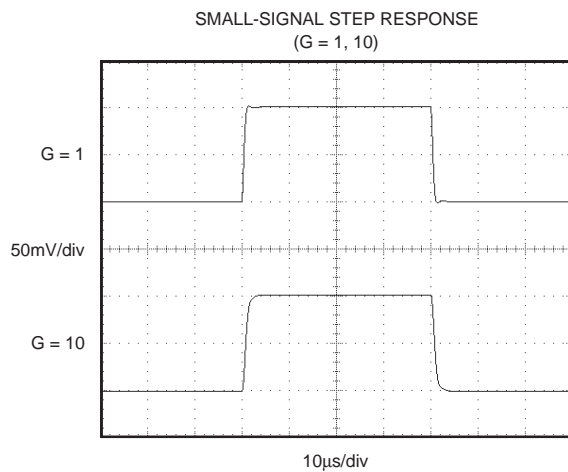
# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.



## APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA121. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 8Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR ( $G = 1$ ).

### SETTING THE GAIN

Gain of the INA121 is set by connecting a single external resistor,  $R_G$ , connected between pins 1 and 8:

$$G = 1 + \frac{50k\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in Equation 1 comes from the sum of the two internal feedback resistors of  $A_1$  and  $A_2$ . These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA121.

The stability and temperature drift of the external gain setting resistor,  $R_G$ , also affects gain.  $R_G$ 's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

### DYNAMIC PERFORMANCE

The typical performance curve "Gain vs Frequency" shows that, despite its low quiescent current, the INA121 achieves wide bandwidth, even at high gain. This is due to the current-feedback topology of the INA121. Settling time also remains excellent at high gain.

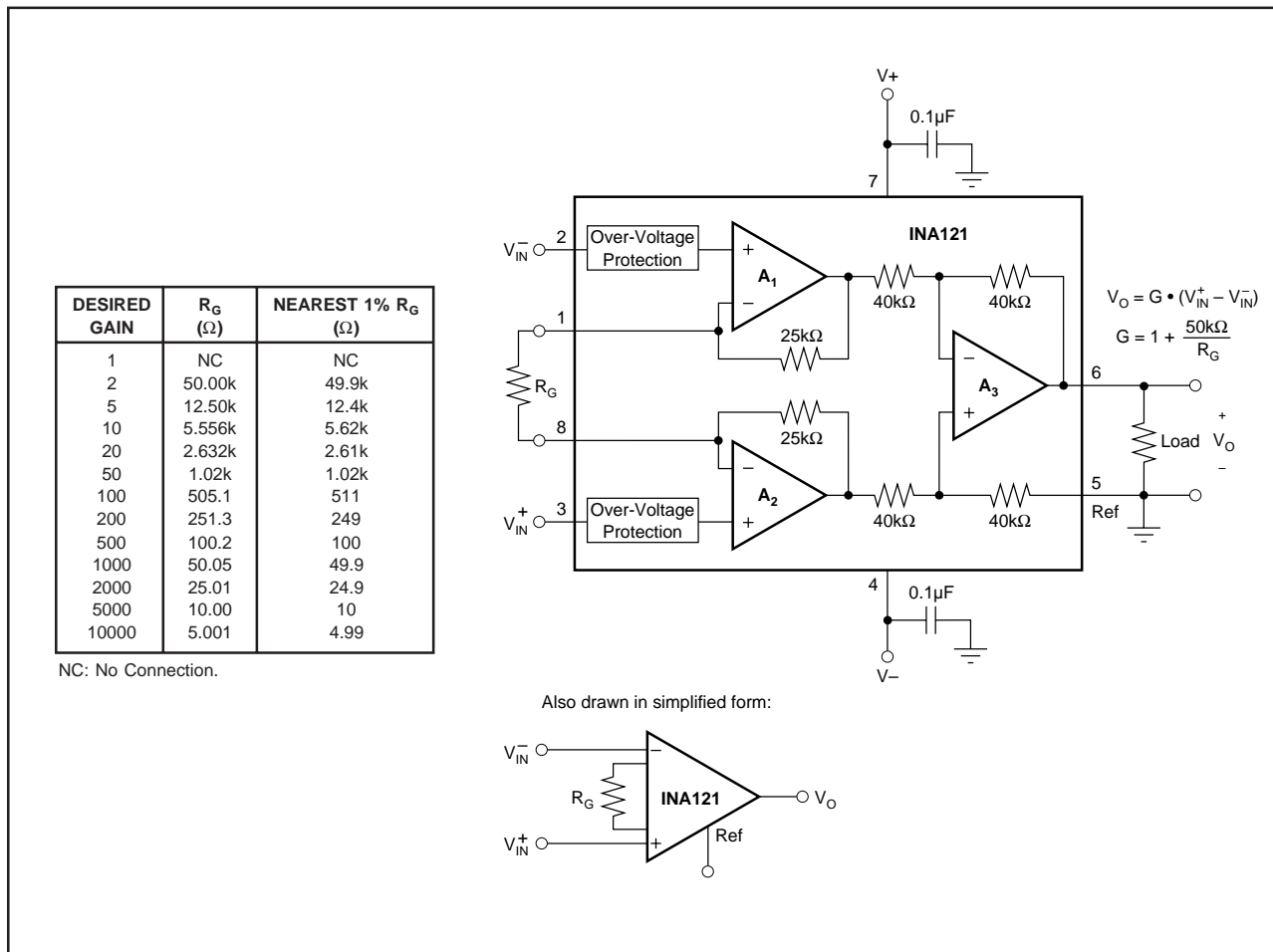


FIGURE 1. Basic Connections.



The INA121 provides excellent rejection of high frequency common-mode signals. The typical performance curve, “Common-Mode Rejection vs Frequency” shows this behavior. If the inputs are not properly balanced, however, common-mode signals can be converted to differential signals. Run the  $V_{IN}^+$  and  $V_{IN}^-$  connections directly adjacent each other, from the source signal all the way to the input pins. If possible use a ground plane under both input traces. Avoid running other potentially noisy lines near the inputs.

## NOISE AND ACCURACY PERFORMANCE

The INA121’s FET input circuitry provides low input bias current and high speed. It achieves lower noise and higher accuracy with high impedance sources. With source impedances of 2k $\Omega$  to 50k $\Omega$  the INA114, INA128, or INA129 may provide lower offset voltage and drift. For very low source impedance ( $\leq 1k\Omega$ ), the INA103 may provide improved accuracy and lower noise. At very high source impedances ( $> 1M\Omega$ ) the INA116 is recommended.

## OFFSET TRIMMING

The INA121 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection. Trim circuits with higher source impedance should be buffered with an op amp follower circuit to assure low impedance on the Ref pin.

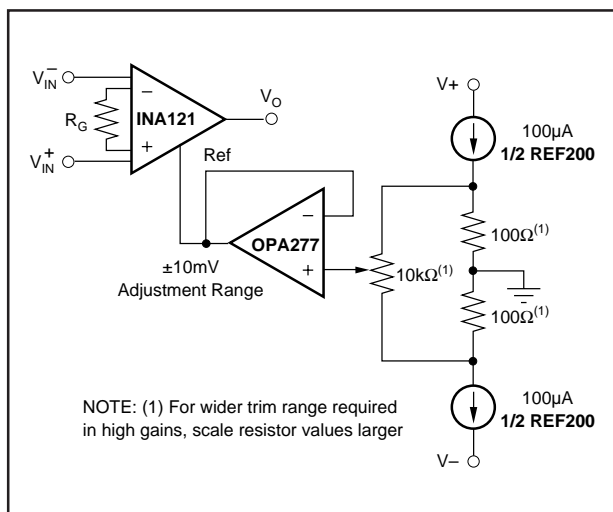


FIGURE 2. Optional Trimming of Output Offset Voltage.

## INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA121 is extremely high—approximately  $10^{12}\Omega$ . However, a path must be provided for the input bias current of both inputs. This input bias current is typically 4pA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA121 is to operate properly. Figure 3 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA121 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

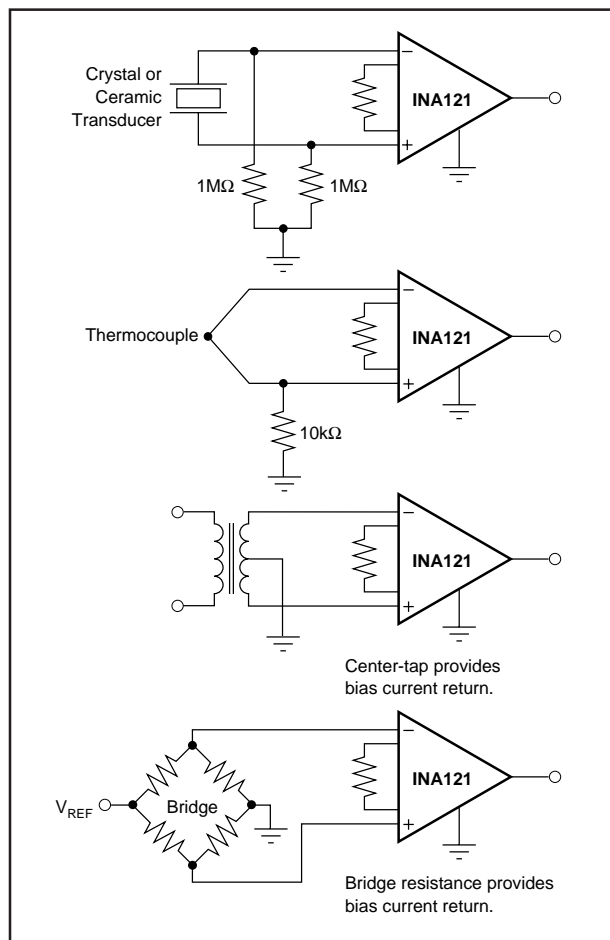


FIGURE 3. Providing an Input Common-Mode Current Path.

## INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA121 is from approximately 1.2V below the positive supply voltage to 2.1V above the negative supply. A differential input voltage causes the output voltage to increase. The linear input range, however, will be limited by the output voltage swing of amplifiers  $A_1$  and  $A_2$ . So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see typical performance curve “Input Common-Mode Range vs Output Voltage”.

A combination of common-mode and differential input voltage can cause the output of  $A_1$  or  $A_2$  to saturate. Figure 4 shows the output voltage swing of  $A_1$  and  $A_2$  expressed in terms of a common-mode and differential input voltages. For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA121 in a lower gain (see performance curve “Input Common-Mode Voltage Range vs Output Voltage”). If necessary, add gain after the INA121 to increase the voltage swing.

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of  $A_3$  will be near 0V even though both inputs are overloaded.

### LOW VOLTAGE OPERATION

The INA121 can be operated on power supplies as low as  $\pm 2.25V$ . Performance remains excellent with power supplies ranging from  $\pm 2.25V$  to  $\pm 18V$ . Most parameters vary only slightly throughout this supply voltage range—see typical

performance curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Typical performance curves, “Input Common-Mode Range vs Output Voltage” show the range of linear operation for  $\pm 15V$ ,  $\pm 5V$ , and  $\pm 2.5V$  supplies.

### INPUT FILTERING

The INA121’s FET input allows use of an R/C input filter without creating large offsets due to input bias current. Figure 5 shows proper implementation of this input filter to preserve the INA121’s excellent high frequency common-mode rejection. Mismatch of the common-mode input time constant ( $R_1C_1$  and  $R_2C_2$ ), either from stray capacitance or mismatched values, causes a high frequency common-mode signal to be converted to a differential signal. This degrades common-mode rejection. The differential input capacitor,  $C_3$ , reduces the bandwidth and mitigates the effects of mismatch in  $C_1$  and  $C_2$ . Make  $C_3$  much larger than  $C_1$  and  $C_2$ . If properly matched,  $C_1$  and  $C_2$  also improve ac CMR.

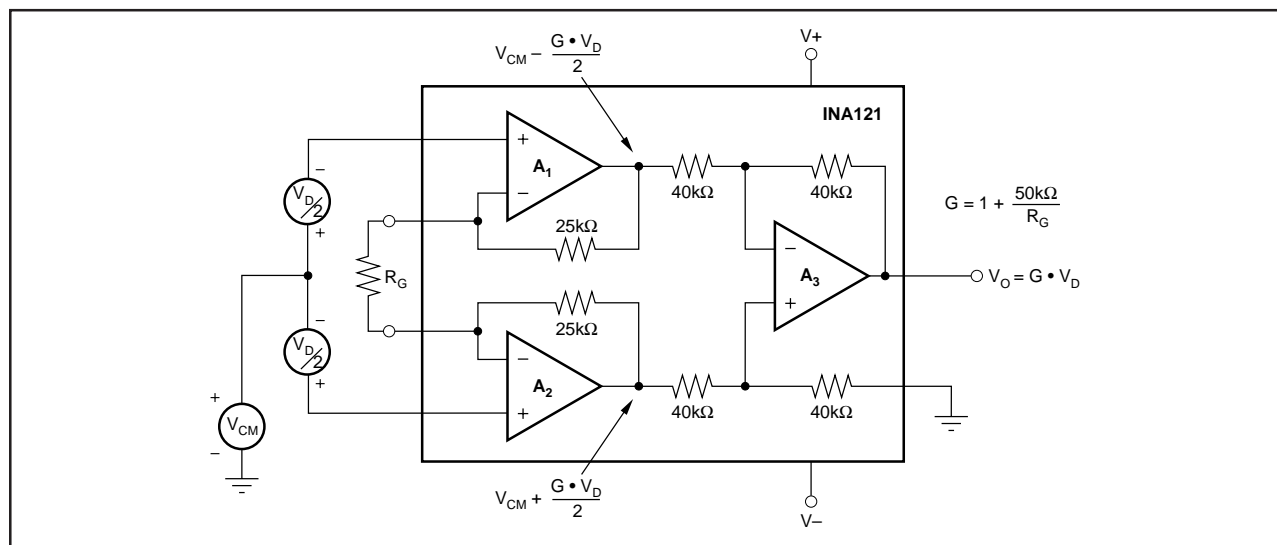


FIGURE 4. Voltage Swing of  $A_1$  and  $A_2$ .

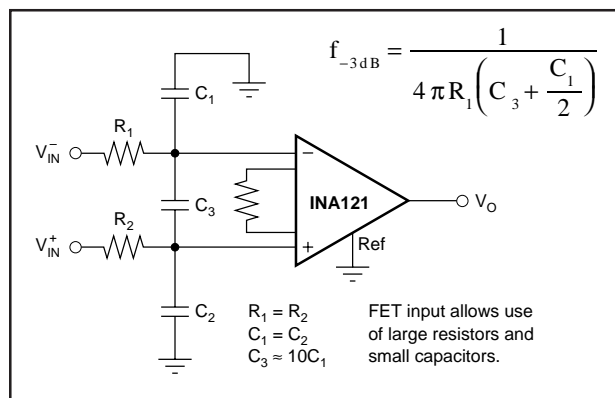


FIGURE 5. Input Low-Pass Filter.

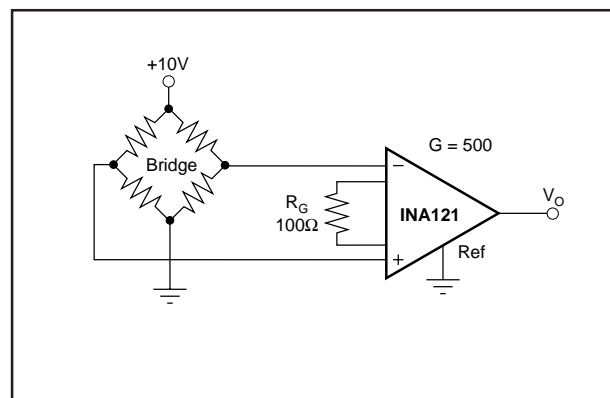


FIGURE 6. Bridge Transducer Amplifier.

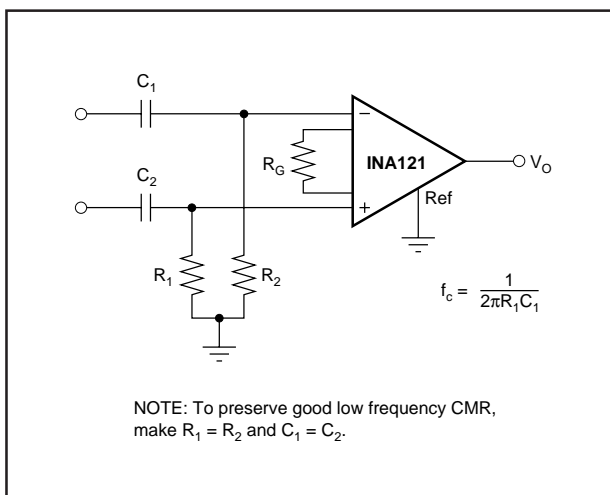


FIGURE 7. High-Pass Input Filter.

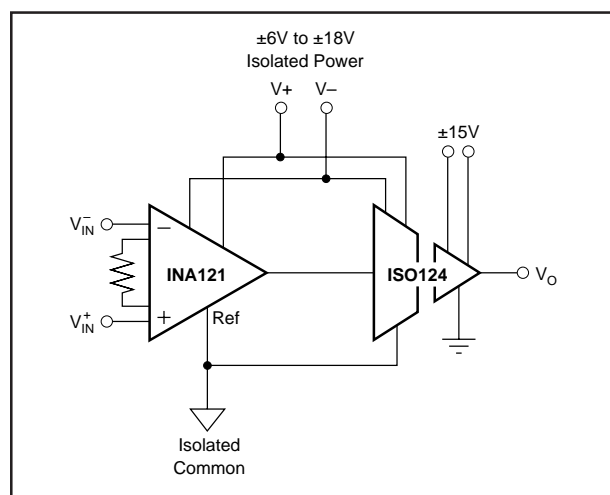


FIGURE 8. Galvanically Isolated Instrumentation Amplifier.

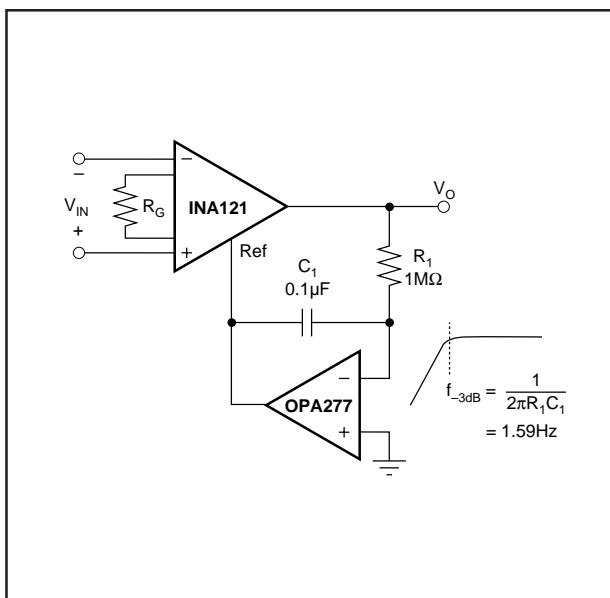


FIGURE 9. AC-Coupled Instrumentation Amplifier.

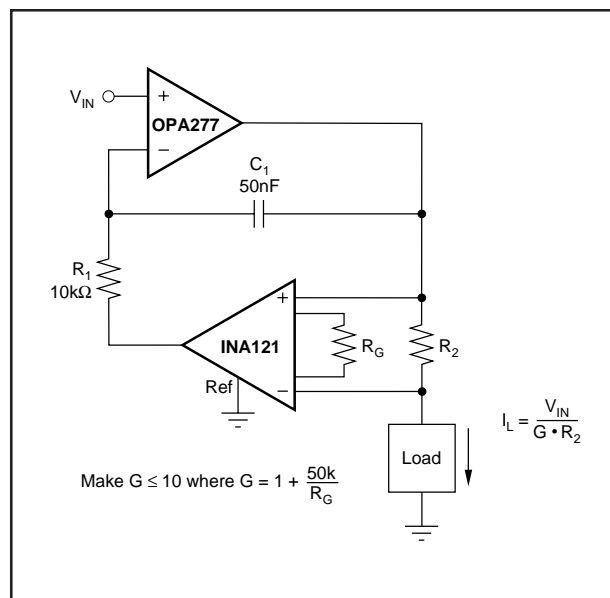


FIGURE 10. Voltage Controlled Current Source.

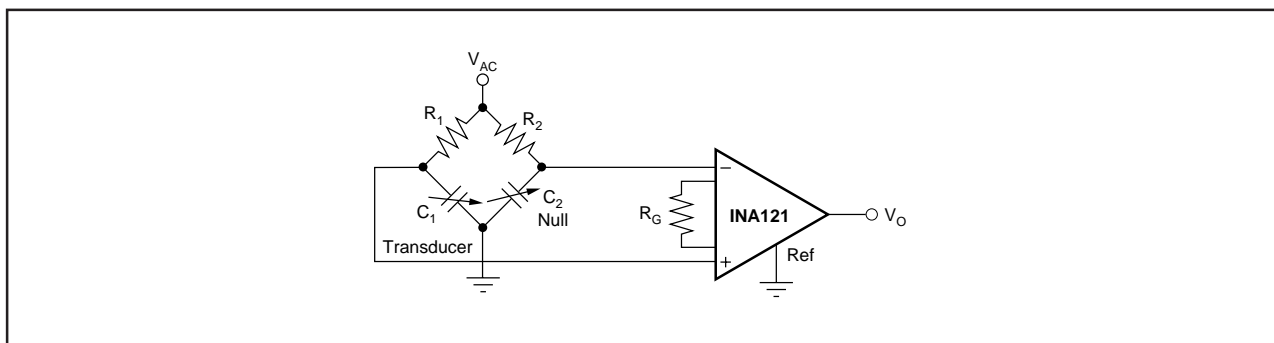


FIGURE 11. Capacitive Bridge Transducer Circuit.

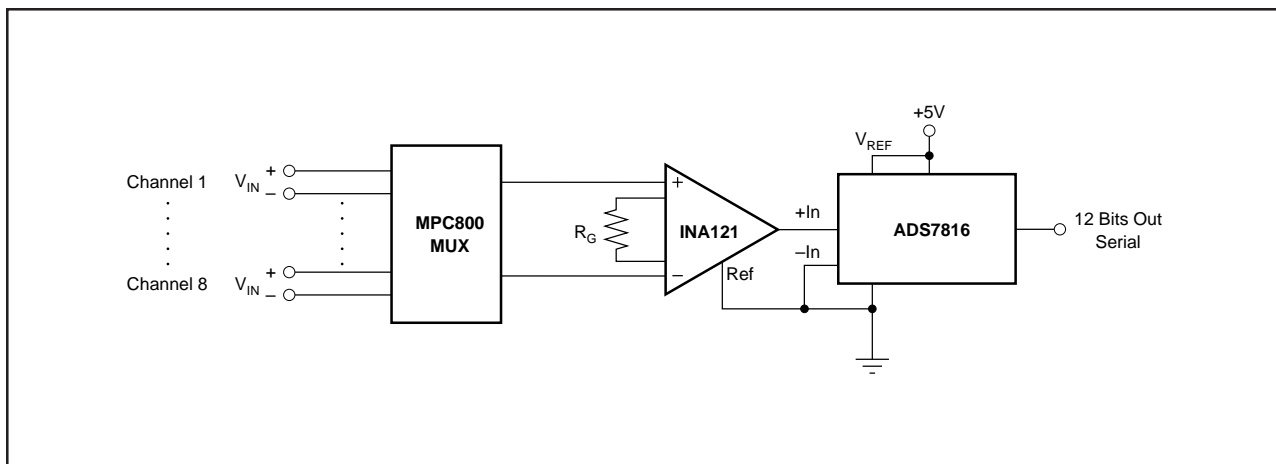


FIGURE 12. Multiplexed-Input Data Acquisition System.

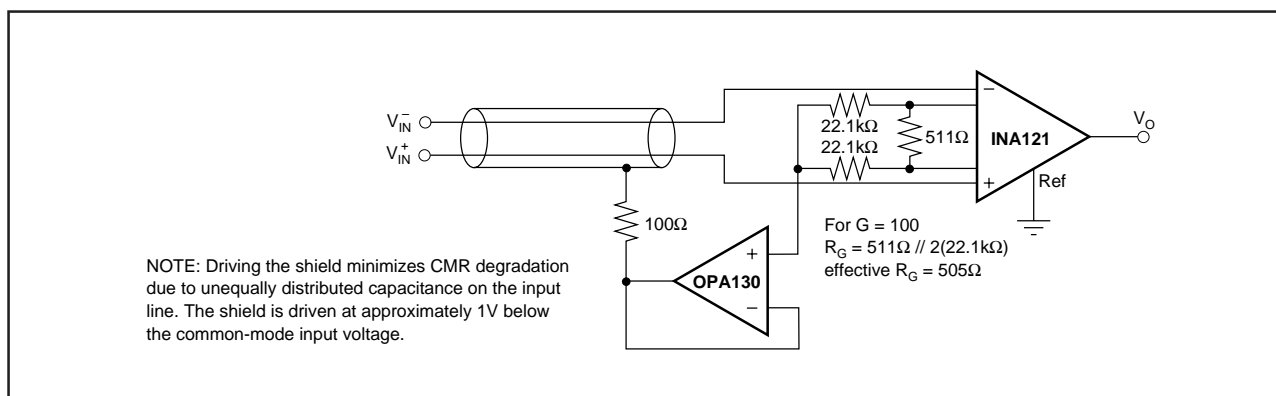


FIGURE 13. Shield Driver Circuit.

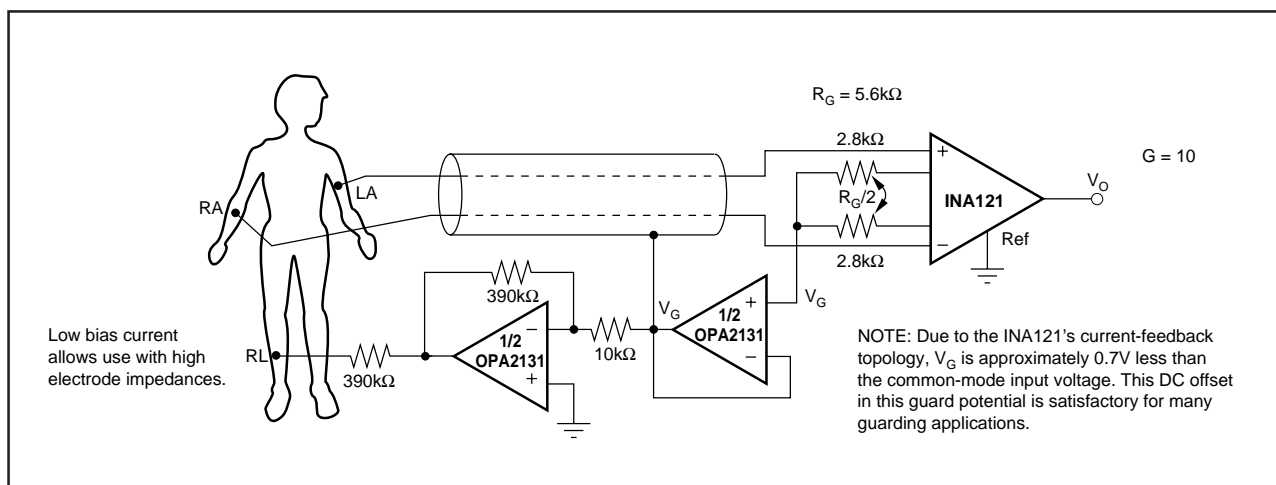


FIGURE 14. ECG Amplifier With Right-Leg Drive.