**Green-Mode PFC / Forward PWM Controller** **SG6932**

## FEATURES OVERVIEW

- Interleaved PFC / PWM switching
- Green-mode PFC and PWM operation
- Low operating current
- Innovative switching-charge multiplier-divider
- Multi-vector control for improved PFC output transient response
- Average-current-mode for input-current shaping
- PFC over-voltage and under-voltage protections
- PFC and PWM feedback open-loop protection
- Cycle-by-cycle current limiting for PFC/PWM
- Slope compensation for PWM
- Selectable PWM maximum duty cycle 50% and 65%
- Brownout protection
- Power-on sequence control and soft-start

## APPLICATIONS

- Switch-mode power supplies with active PFC
- Servo system power supplies
- PC-ATX power supplies

## DESCRIPTION

The highly integrated SG6932 is designed for power supplies with boost PFC and forward PWM. It requires very few external components to achieve green-mode operation and versatile protections / compensation. It is available in 16-pin DIP and SOP packages.

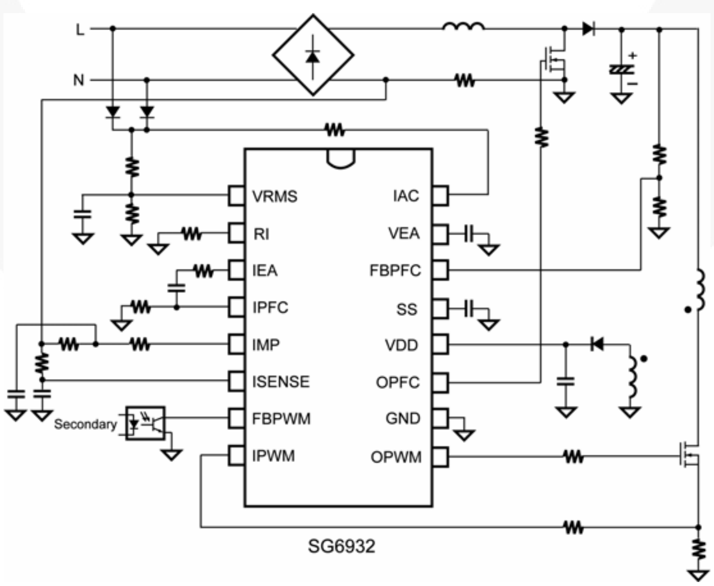
The patented interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise. At light load, the switching frequency is continuously decreased to reduce power consumption.

For PFC stage, the proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, SG6932 shuts off to prevent extra-high voltage on output.

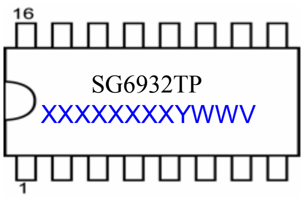
For the Forward PWM stage, the synchronized slope compensation ensures the stability of the current loop under continuous-conduction-mode operation. Hiccup operation during output overloading is guaranteed. The soft-start and programmable maximum duty cycle ensure safe operation.

SG6932 provides complete protection functions, such as brownout protection and RI open/short latch off.

## TYPICAL APPLICATION

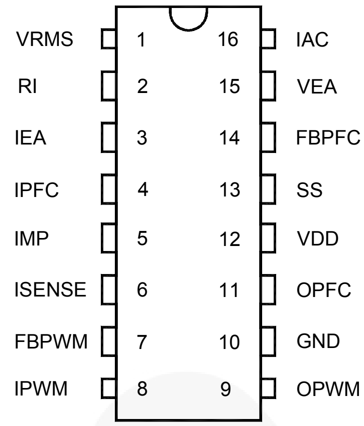


## MARKING DIAGRAMS




T: D=DIP, S=SOP
P : Z =Lead Free + ROHS Compatible
XXXXXXXX: Wafer Lot
Y: Year; WW: Week
V: Assembly Location

## PIN CONFIGURATION



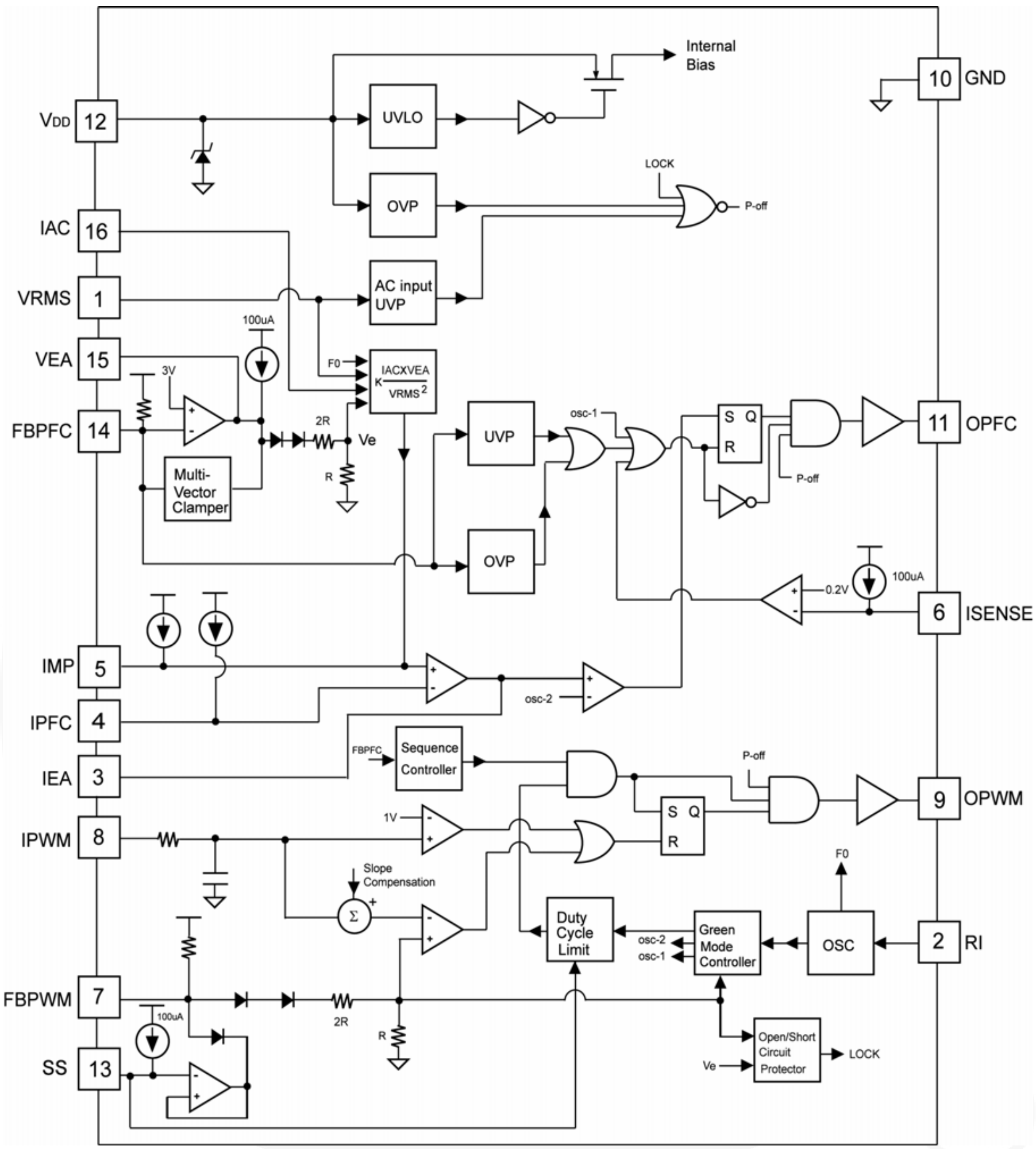

## ORDERING INFORMATION

| Part Number | Pb-Free | Package |
|---|---|---|
| SG6932DZ | | 16-pin DIP |
| SG6932SZ (Preliminary) | | 16-pin SOP |

## PIN DESCRIPTIONS

| Name | Pin No. | Type | Function |
|---|---|---|---|
| VRMS | 1 | Line-Voltage Detection | Line voltage detection. The pin is used for PFC multiplier and brownout protection. |
| RI | 2 | Oscillator Setting | Reference setting. One resistor connected between RI and ground determines the switching frequency. A resistor with resistance between 12k ~ 47kΩ is recommended. The switching frequency is equal to [1560 / $R_I$] kHz, where $R_I$ is in kΩ. For example, if $R_I$ is 24kΩ, the switching frequency is 65kHz. |
| IEA | 3 | Output of PFC Current Amplifier | This is the output of the PFC current amplifier. The signal from this pin is compared with an internal sawtooth and determines the pulse width for PFC gate drive. |
| IPFC | 4 | Inverting Input of PFC Current Amplifier | The inverting input of the PFC current amplifier. Proper external compensation circuits result in excellent input power factor via average-current-mode control. |
| IMP | 5 | Non-inverting Input of PFC Current Amplifier and Output of Multiplier | The non-inverting input of the PFC current amplifier and the output of the multiplier. Proper external compensation circuits result in excellent input power factor via average current mode control. |
| ISENSE | 6 | Peak Current Limit Setting for PFC | The peak current limit setting for PFC. |
| FBPWM | 7 | PWM Feedback Input | The control input for voltage-loop feedback of PWM stage. It is internally pulled high through a 6.5kΩ resistance. Usually an external opto-coupler from secondary feedback circuit is connected to this pin. |
| IPWM | 8 | PWM Current Sense | The current sense input for the PWM stage. Via a current sense resistor, this pin provides the control input for peak-current-mode control and cycle-by-cycle current limiting. |
| OPWM | 9 | PWM Gate Drive | The totem pole output drive for PWM MOSFET. This pin is internally clamped under 18V to protect the MOSFET. |
| GND | 10 | Ground | The power ground. |
| OPFC | 11 | PFC Gate Drive | The totem pole output drive for the PFC MOSFET. This pin is internally clamped under 18V to protect the MOSFET. |
| VDD | 12 | Supply | The power supply pin. The threshold voltages for start-up and turn-off are 14V and 10V, respectively. The operating current is lower than 10mA. |
| SS | 13 | PWM Soft-Start | During start-up, the SS pin charges an external capacitor with a 50µA constant current source. The voltage on FBPWM is clamped by SS during start-up. In the event of a protection condition occurring and/or PWM being disabled, the SS pin is quickly discharged. The voltage of SS pin can be used to select 50% or 65% maximum duty cycle. |
| FBPFC | 14 | Voltage Feedback Input for PFC | The feedback input for PFC voltage loop. The inverting input of PFC error amplifier. This pin is connected to the PFC output through a divider network. |
| VEA | 15 | Error Amplifier Output for PFC Voltage Feedback Loop | The error amplifier output for PFC voltage feedback loop. A compensation network (usually a capacitor) is connected between this pin and ground. A large capacitor value results in a narrow bandwidth and improves the power factor. |
| IAC | 16 | Input AC Current | For normal operation, this input is used to provide current reference for the multiplier. The suggested maximum $I_{AC}$ is 360µA. |

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Test Conditions | Value | | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage* | | 25 | | V |
| $I_{AC}$ | Input AC Current | | 2 | | mA |
| $V_{High}$ | OPWM, OPFC, IAC | | -0.5 to 25V | | V |
| $V_{Low}$ | Others | At $T_A$<50℃ | -0.5 to 7V | | V |
| $P_D$ | Power Dissipation | | 0.8 | | W |
| $T_J$ | Operating Junction Temperature | | -40 to 125 | | ℃ |
| $T_{stg}$ | Storage Temperature Range | | -55 to +150 | | ℃ |
| $R_{\theta jC}$ | Thermal resistance (Junction-to-Case) | | DIP | 33.64 | ℃/W |
| | | | SOP | 41.95 | |
| $T_L$ | Lead Temperature (Wave soldering, 10 seconds) | | 260 | | ℃ |
| ESD | Electrostatic Discharge Capability, Human Body Model | | 4.5 | | KV |
| | Electrostatic Discharge Capability, Machine Model | | 250 | | V |

*All voltage values, except differential voltages, are given with respect to the network ground terminal.

## RECOMMENDED OPERATING JUNCTION TEMPERATURE: -30°C~ 85°C*

* For proper operation.

## ELECTRICAL CHARACTERISTICS

$V_{DD}$=15V, $T_A$=25°C unless otherwise noted.

### $V_{DD}$ Section

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD-OP}$ | Continuously Operating Voltage | | | | 20 | V |
| $I_{DD\ ST}$ | Start-Up Current | $V_{DD}$ -0.16V | | 10 | 20 | μA |
| $I_{DD-OP}$ | Operating Current | $V_{DD}$=15V; OPFC OPWM open | | 6 | 10 | mA |
| $V_{TH-ON}$ | Start Threshold Voltage | | 13 | 14 | 15 | V |
| $V_{DD-min}$ | Min. Operating Voltage | | 9 | 10 | 11 | V |
| $V_{DD-OVP}$ | VDD OVP1 (turn off PWM with delay) | | 23.5 | 24.5 | 25.5 | V |
| $TV_{DD-OVP}$ | Delay time of VDD OVP1 | $R_I$=24kΩ | 8 | | 25 | μs |

### Oscillator & Green-Mode Operation

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{RI}$ | RI Voltage | | 1.176 | 1.200 | 1.224 | V |
| $F_{OSC}$ | PWM Frequency | $R_I$=24kΩ | 62 | 65 | 68 | KHz |
| $F_{OSC-MINFREQ}$ | Minimum Frequency in Green Mode | $R_I$=24kΩ | 18 | 20 | 22 | KHz |
| RI | RI Range | | 12 | | 47 | kΩ |
| $RI_{OPEN}$ | RI Pin Open Protection<br>If RI > $RI_{open}$ , PWM Turned Off | | | 200 | | kΩ |
| $RI_{SHORT}$ | RI Pin Short Protection<br>If RI< $RI_{short}$ , PWM Turned Off | | | 2 | | kΩ |

## $V_{RMS}$ for UVP and ON/OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{RMS-UVP-1}$ | RMS AC Voltage Under-Voltage Threshold to Turn Off PFC (with $T_{UVP}$ Delay) for UVP Mode1 | | 0.75 | 0.8 | 0.85 | V |
| $V_{RMS-UVP-2}$ | Recovery Level on $V_{RMS}$ for UVP | | $V_{RMS-UVP-1}$+ 0.17V | $V_{RMS-UVP-1}$+ 0.19V | $V_{RMS-UVP-1}$+ 0.21V | V |
| $T_{UVP}$ | Under-Voltage Protection Propagation to Turn Off PFC Delay Time (No Delay for Start-up) | $R_I$=24kΩ | 150 | 195 | 240 | ms |

## PFC Stage

### Voltage Error Amplifier

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{REF}$ | Reference Voltage | | 2.95 | 3.00 | 3.05 | V |
| Av | Open-Loop Gain | | | 60 | | dB |
| $Z_o$ | Output Impedance | | | 110 | | kΩ |
| $OVP_{FBPFC}$ | PFC Over-voltage Protection | | 3.20 | 3.25 | 3.30 | V |
| $\triangle OVP_{FBPFC}$ | PFC Feedback Voltage Protection Hysteresis | | 60 | 90 | 120 | mV |
| $V_{FBPFC-H}$ | Clamp-High Feedback Voltage | | 3.10 | 3.15 | 3.20 | V |
| $G_{FBPFC-H}$ | Clamp-High Gain | | | 0.5 | | mA/V |
| $V_{FBPFC-L}$ | Clamp-Low Feedback Voltage | | 2.75 | 2.85 | 2.90 | V |
| $G_{FBPFC-L}$ | Clamp-Low Gain | | | 6.5 | | mA/mV |
| $I_{FBPFC-L-}$ | Maximum Source Current | | 1.5 | 2.0 | | mA |
| $I_{FBPFC-H-}$ | Maximum Sink Current | | 70 | 110 | | μA |
| $UVP_{VFB}$ | PFC Feedback Under-Voltage Protection | | 0.35 | 0.40 | 0.45 | V |
| $V_{FBHIGH}$ | Output High Voltage on $V_{EA}$ | | 6 | 7 | 8 | V |
| $V_{RD-FBPFC}$ | Voltage level on FBPFC to Enable OPWM During Start-up | | 2.6 | 2.7 | 2.8 | V |
| $T_{UVP-PFC}$ | Debounce Time of PFC UVP | | 40 | 70 | 120 | μs |

### Current Error Amplifier

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OFFSET}$ | Input Offset Voltage ((-) > (+)) | | | 8 | | mV |
| $A_I$ | Open-loop Gain | | | 60 | | dB |
| BW | Unit Gain Bandwidth | | | 1.5 | | MHz |
| CMRR | Common-mode Rejection Ratio | $V_{CM}$=0 ~ 1.5V | | 70 | | dB |
| $V_{OUT-HIGH}$ | Output High Voltage | | 3.2 | | | V |
| $V_{OUT-LOW}$ | Output Low Voltage | | | | 0.2 | V |
| $I_{MR1}$, $I_{MR2}$ | Reference Current Source | $R_I$=24kΩ ($I_{MR}$=20+$I_{RI}$•0.8) | 50 | | 70 | μA |
| $I_L$ | Maximum Source Current | | | 3 | | mA |
| $I_H$ | Maximum Sink Current | | | 0.25 | | mA |

## Peak Current Limit

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_P$ | Constant Current Output | $R_I$=24kΩ | 90 | 100 | 110 | μA |
| $V_{pk}$ | Peak Current Limit Threshold Voltage Cycle-by-Cycle Limit ($V_{sense}$ < $V_{pk}$) | $V_{RMS}$=1.05V | 0.15 | 0.20 | 0.25 | V |
| | | $V_{RMS}$=3V | 0.35 | 0.40 | 0.45 | V |
| $T_{pkD}$ | Propagation Delay | | | | 200 | ns |
| Bnkt | Leading-Edge Blanking Time | | 270 | 350 | 450 | ns |

## Multiplier

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{AC}$ | Input AC Current | Multiplier Linear Range | 0 | | 360 | μA |
| $I_{MO-max}$ | Maximum Multiplier Current Output; | $R_I$=24kΩ | | 230 | | μA |
| $I_{MO-1}$ | Multiplier Current Output (Low-Line, High-Power) | $V_{RMS}$=1.05V; $I_{AC}$=90μA; $V_{EA}$=7.5V; $R_I$=24kΩ | 200 | 230 | 280 | μA |
| $I_{MO-2}$ | Multiplier Current Output (High-Line, High-Power) | $V_{RMS}$=3V; $I_{AC}$=264μA; $V_{EA}$=7.5V; $R_I$=24kΩ | 65 | 85 | | μA |
| $V_{IMP}$ | Voltage of IMP Open | | 3.4 | 3.9 | 4.4 | V |

## PFC Output Driver

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{Z-PFC}$ | Output Voltage Maximum (Clamp) | $V_{DD}$=20V | | 16 | 18 | V |
| $V_{OL-PFC}$ | Output Voltage Low | $V_{DD}$=15V; $I_O$=100mA | | | 1.5 | V |
| $V_{OH-PFC}$ | Output Voltage High | $V_{DD}$=13V; $I_O$=100mA | 8 | | | V |
| $T_{R-PFC}$ | Rising Time | $V_{DD}$=15V; $C_L$=5nF; O/P=2V to 9V | 40 | 70 | 120 | ns |
| $T_{f-PFC}$ | Falling Time | $V_{DD}$=15V; $C_L$=5nF; O/P=9V to 2V | 40 | 60 | 110 | ns |
| $DC_{(MAX)}$ | Maximum Duty Cycle | | 93 | | 97 | % |

## PWM Stage

### FBPWM

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $A_V$ | FB to Current Comparator Attenuation | | 2.2 | 2.7 | 3.2 | V/V |
| $Z_{FB}$ | Input Impedance | | 4 | 5 | 7 | kΩ |
| $FB_{OPEN-LOOP}$ | PWM Open-Loop Protection Voltage | | 4.2 | 4.5 | 4.8 | V |
| $T_{OPEN-PWM-Hiccup}$ | Interval of PWM Open-Loop Protection Reset | $R_I$=24kΩ | 500 | 600 | 700 | ms |
| $T_{OPEN-PWM}$ | PWM Open-Loop Protection Delay Time | $R_I$=24kΩ | 80 | 95 | 120 | ms |
| $V_N$ | Frequency Reduction Threshold on FBPWM | | 1.9 | 2.1 | 2.3 | V |
| $S_G$ | Green-Mode Modulation Slope | | 60 | 75 | 90 | Hz/mV |
| $V_G$ | Voltage on FBPWM for Minimum Green-Mode Frequency | | 1.35 | 1.60 | 1.75 | V |

## PWM-Current Sense

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{PD-PWM}$ | Propagation Delay to Output – $V_{LIMIT}$ Loop | $V_{DD}$=15V, OPWM drops to 9V | 60 | | 120 | ns |
| $V_{LIMIT}$ | Peak Current Limit Threshold Voltage | | 0.65 | 0.70 | 0.75 | V |
| $T_{BNK-PWM}$ | Leading-Edge Blanking Time | | 270 | 350 | 450 | ns |
| $\triangle V_{SLOPE}$ | Slope Compensation<br>$\triangle V_s = \triangle V_{SLOPE}$ x $(T_{on}/T)$<br>$\triangle V_s$: Compensation Voltage Added to Current Sense | | 0.40 | 0.45 | 0.55 | V |

## Output Driver

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{Z-PWM}$ | Output Voltage Maximum (Clamp) | $V_{DD}$=20V | | 16 | 18 | V |
| $T_{PWM}$ | Interval of OPWM Lags Behind OPFC at Start-up | $R_I$=24kΩ | 2 | 4 | 6 | ms |
| $V_{OL-PWM}$ | Output Voltage Low | $V_{DD}$=15V; $I_O$=100mA | | | 1.5 | V |
| $V_{OH-PWM}$ | Output Voltage High | $V_{DD}$=13V; $I_O$=100mA | 8 | | | V |
| $T_{R-PWM}$ | Rising Time | $V_{DD}$=15V; $C_L$=5nF; O/P=2V to 9V | 30 | 60 | 120 | ns |
| $T_{F-PWM}$ | Falling Time | $V_{DD}$=15V; $C_L$=5nF; O/P=9V to 2V | 30 | 50 | 110 | ns |

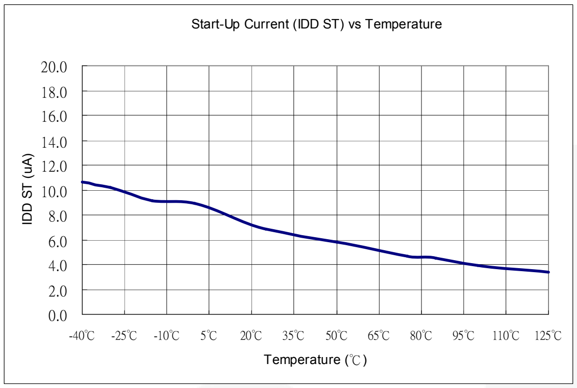
## Maximum Duty Cycle

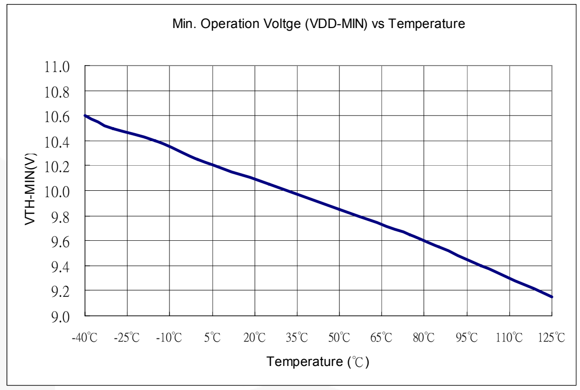
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $DC_{SS=6V}$ | Maximum Duty Cycle for SS=6V | $R_I$=24kΩ | 62 | | 66 | % |
| $DC_{SS=5V}$ | Maximum Duty Cycle for SS=5V | $R_I$=24kΩ | 46 | | 50 | % |

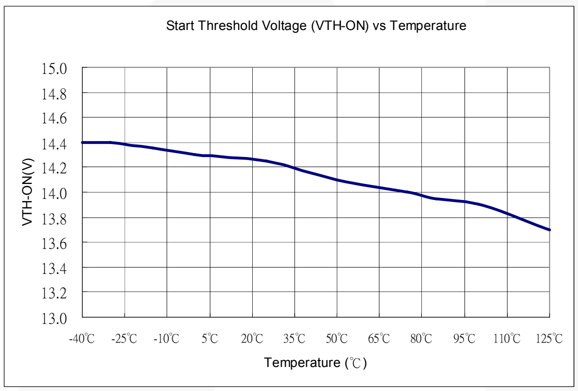
## Soft-Start

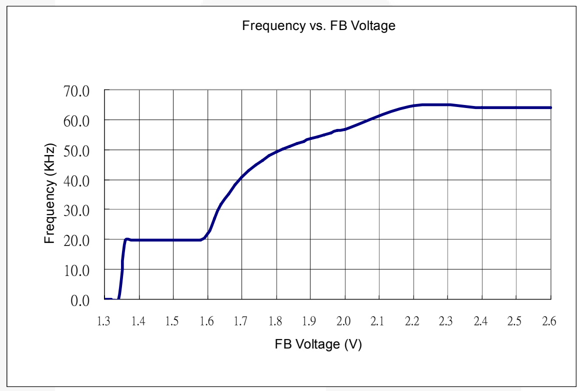
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SS}$ | Constant Current Output for Soft-Start | $R_T$=24kΩ | 44 | 50 | 56 | μA |
| $V_{DC-MAX-50\%}$ | Voltage of SS for 50% Maximum Duty Cycle | | | | 5 | V |
| $V_{DC-MAX--65\%}$ | Voltage of SS for 65% Maximum Duty Cycle | | 6 | | | V |
| $R_D$ | Discharge Resistance | | | 470 | | Ω |

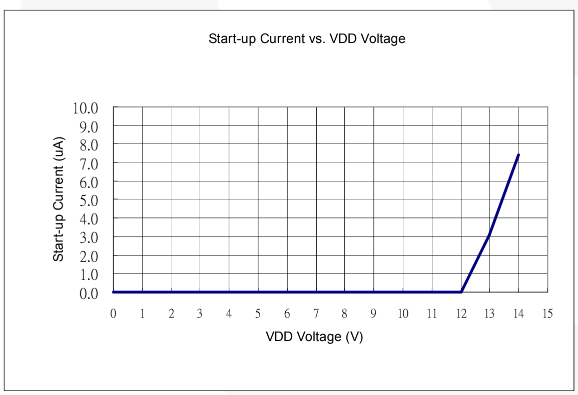
# TYPICAL CHARACTERISTICS

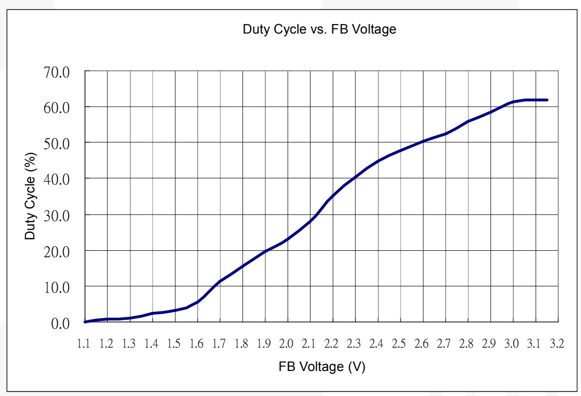


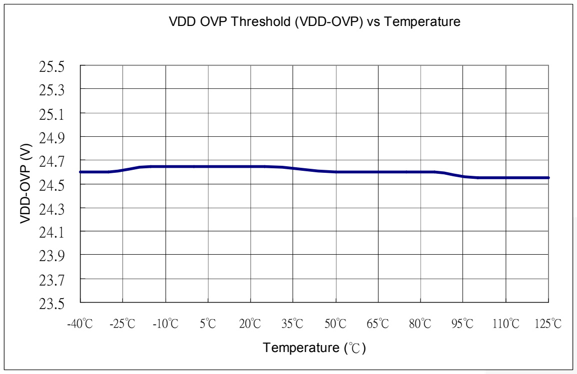



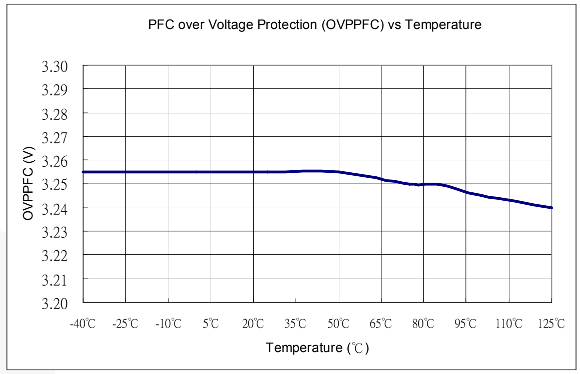



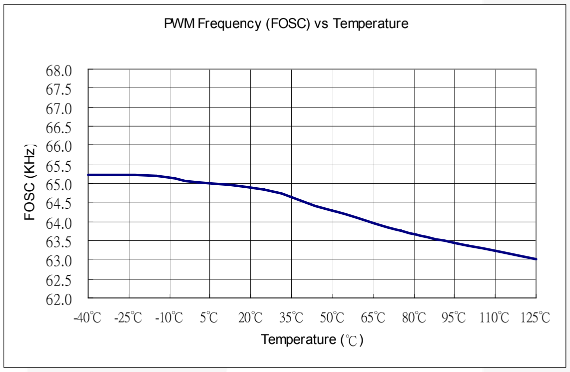



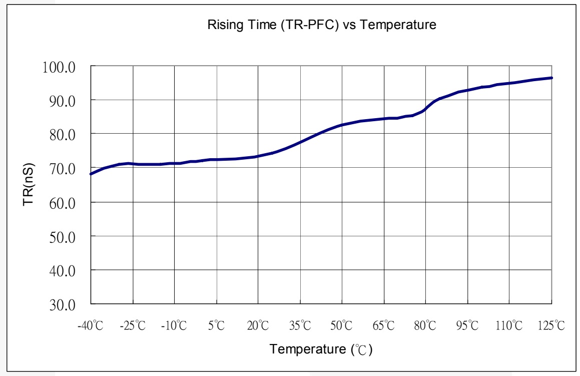



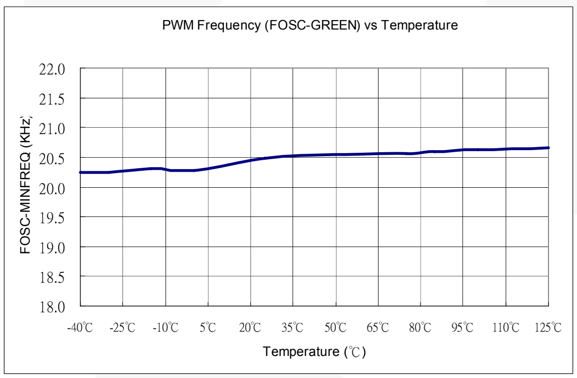



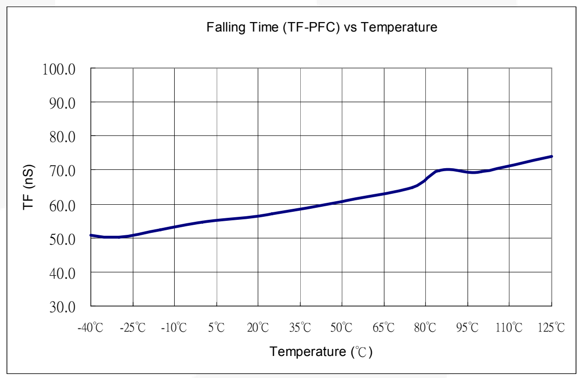

VDD OVP Threshold (VDD-OVP) vs Temperature
VDD-OVP (V)
Temperature (℃)

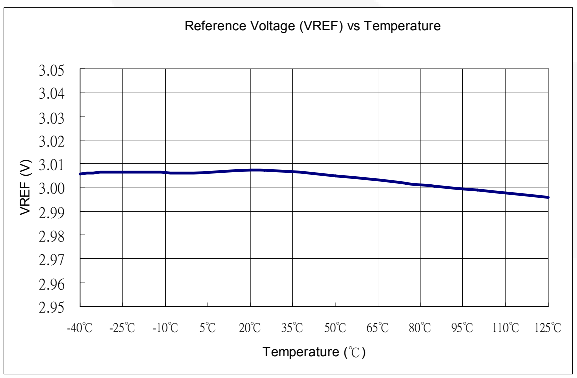

PFC over Voltage Protection (OVPPFC) vs Temperature
OVPPFC (V)
Temperature (℃)

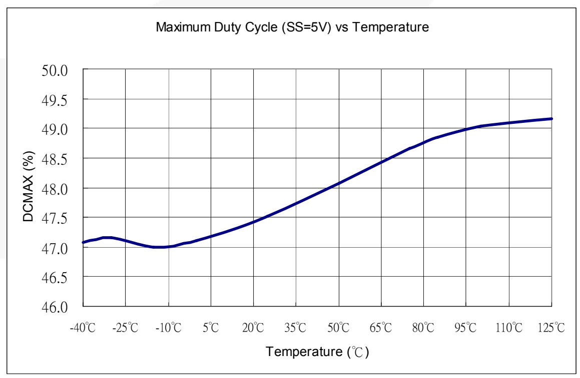

PWM Frequency (FOSC) vs Temperature
FOSC (KHz)
Temperature (℃)

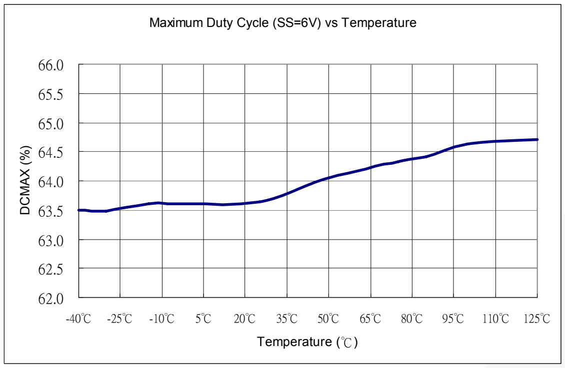

Rising Time (TR-PFC) vs Temperature
TR(nS)
Temperature (℃)

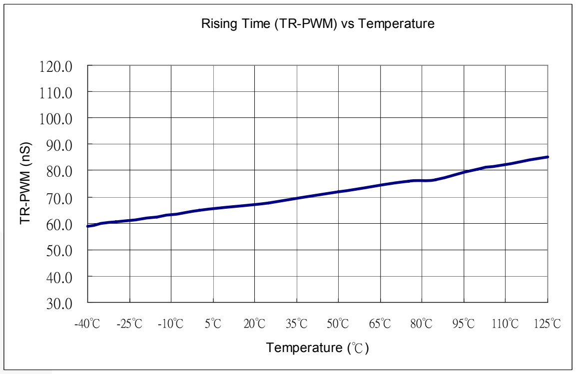

PWM Frequency (FOSC-GREEN) vs Temperature
FOSC-MINFREQ (KHz)
Temperature (℃)

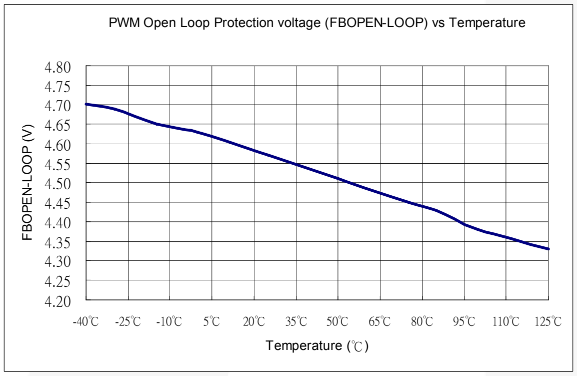

Falling Time (TF-PFC) vs Temperature
TF (nS)
Temperature (℃)

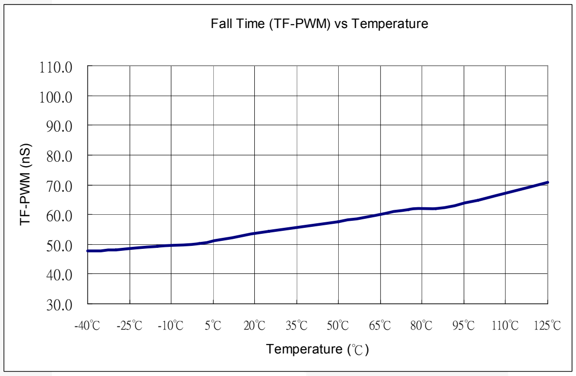

Reference Voltage (VREF) vs Temperature
VREF (V)
Temperature (℃)

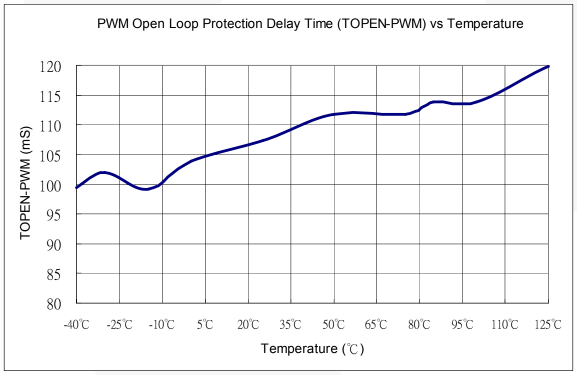

Maximum Duty Cycle (SS=5V) vs Temperature
DCMAX (%)
Temperature (℃)

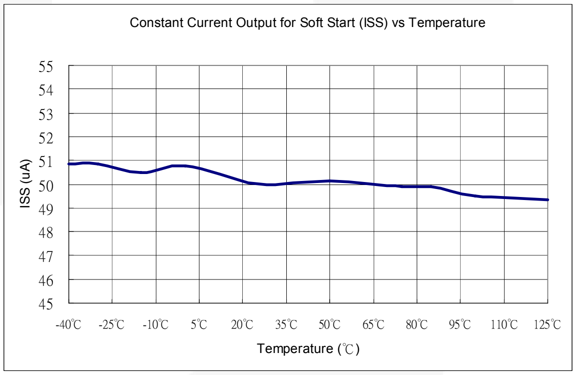

Maximum Duty Cycle (SS=6V) vs Temperature
DCMAX (%)
66.0
65.5
65.0
64.5
64.0
63.5
63.0
62.5
62.0
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)

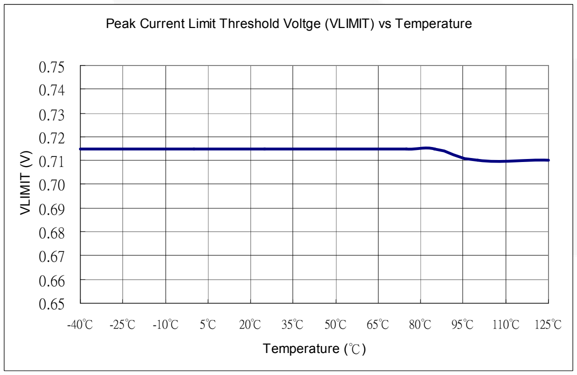

Rising Time (TR-PWM) vs Temperature
TR-PWM (nS)
120.0
110.0
100.0
90.0
80.0
70.0
60.0
50.0
40.0
30.0
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)


PWM Open Loop Protection voltage (FBOPEN-LOOP) vs Temperature
FBOPEN-LOOP (V)
4.80
4.75
4.70
4.65
4.60
4.55
4.50
4.45
4.40
4.35
4.30
4.25
4.20
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)


Fall Time (TF-PWM) vs Temperature
TF-PWM (nS)
110.0
100.0
90.0
80.0
70.0
60.0
50.0
40.0
30.0
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)


PWM Open Loop Protection Delay Time (TOPEN-PWM) vs Temperature
TOPEN-PWM (mS)
120
115
110
105
100
95
90
85
80
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)


Constant Current Output for Soft Start (ISS) vs Temperature
ISS (uA)
55
54
53
52
51
50
49
48
47
46
45
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)


Peak Current Limit Threshold Voltge (VLIMIT) vs Temperature
VLIMIT (V)
0.75
0.74
0.73
0.72
0.71
0.70
0.69
0.68
0.67
0.66
0.65
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)

## OPERATION DESCRIPTION

The highly integrated SG6932 is designed for power supplies with boost PFC and forward PWM. It requires very few external components to achieve green-mode operation and versatile protections / compensation.

The patented interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise. At light load, the switching frequency is linearly decreased to reduce power consumption.

The PFC function is implemented by average-current-mode control. The patented switching charge multiplier-divider provides high-degree noise immunity for the PFC circuit. This also enables the PFC circuit to operate over a much wider region. The proprietary multi-vector output voltage control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6932 shuts off PFC to prevent extra-high voltage on output.

For the forward PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-mode operation. Hiccup operation during output overloading is also guaranteed. To prevent the power supply from drawing large current during start-up, the start-up for PWM stage is delayed 4ms after the PFC output voltage reaches its setting value.

In addition, SG6932 provides complete protection functions such as brownout protection and built-in latch for over-voltage and RI open/short.

## $I_{AC}$ signal

Figure 1 shows the IAC pin connected to input voltage by a resistance and the current, $I_{AC}$, is the input for PFC multiplier. For the linear range of $I_{AC}$ 0~360µA, the range input voltage should be connected a resistance over 1.2M.

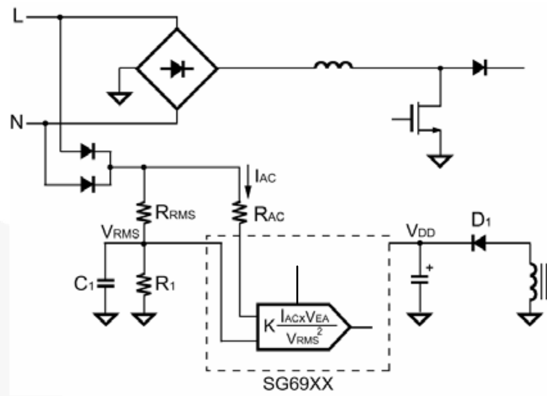



Figure 1. Input Voltage Detection

## Switching Frequency / Current Sources

The switching frequency of SG6932 can be programmed by the resistor RI connected between RI pin and GND. The relationship is:

$$f_{PWM} = \frac{1560}{R_I\ (k\Omega)} (kHz) \quad \text{-------------} \quad (1)$$

For example, a 24kΩ resistor $R_I$ results in a 65kHz switching frequency. Accordingly, constant current $I_T$ flows through $R_I$.

$$I_T = \frac{1.2V}{R_I\ (k\Omega)} (mA) \quad \text{----------------} \quad (2)$$

$I_T$ is used to generate internal current reference.

## Line Voltage Detection ($V_{RMS}$)

Figure 2 shows a resistive divider with low-pass filtering for line-voltage detection on VRMS pin. The $V_{RMS}$ voltage is used for the PFC multiplier and brownout protection. For brownout protection, when the $V_{RMS}$ voltage drops below 0.8V, OPFC turns off.

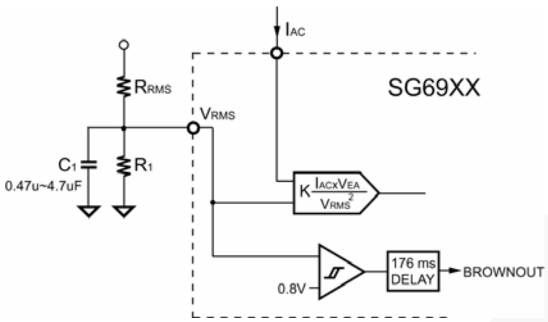



Figure 2. Line-Voltage Detection on VRMS Pin

## Interleave Switching / Green-Mode

The SG6932 uses interleaved switching to synchronize the PFC and PWM stages. This reduces switching noise and spreads the EMI emissions. Figure 3 shows off-time ($T_{OFF}$) inserted between the turn-off of the PFC gate drives and the turn-on of the PWM.

The off-time ($T_{OFF}$) is increased in response to the decreasing of the voltage level of FBPWM; therefore, the PWM switching frequency is linearly decreased to reduce switching losses.

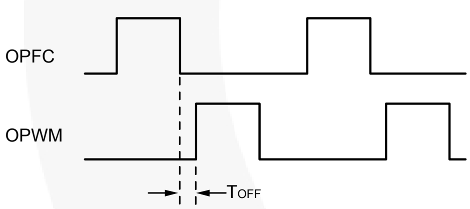



Figure 3. Interleaved Switching

## PFC Operation

The purpose of a boost active power factor corrector (PFC) is to shape the input current of a power supply. The input current waveform and phase follow that of the input voltage. Using SG6932, average-current-mode control is utilized for continuous-current-mode operation for the PFC booster. With the innovative multi-vector control for voltage loop and switching-charge multiplier-divider for current reference, excellent input power factor is achieved with good noise immunity and transient response. Figure 4 shows the total control loop for the average-current-mode control circuit of SG6932.

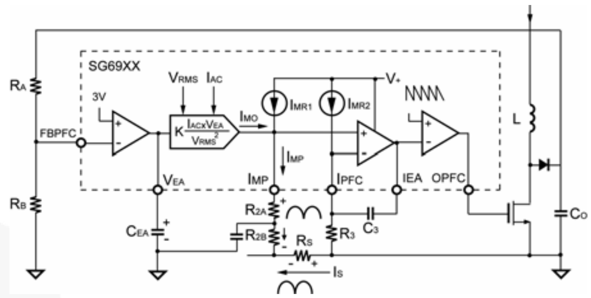



Figure 4. Control Loop of PFC Stage

The current source output from the switching charge multiplier-divider can be expressed as:

$$I_{MO} = K \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} (\mu A) \quad (3)$$

$I_{MP}$, the current output from IMP pin, is the summation of $I_{MO}$ and $I_{MR1}$. $I_{MR1}$ and $I_{MR2}$ are identical fixed-current sources. $R_2$ and $R_3$ are also identical. They are used to pull high the operating point of the IMP and IPFC pins when the voltage across $R_S$ goes negative with respect to ground.

Through the differential amplification of the signal across $R_S$, better noise immunity is achieved. The output of IEA is compared with an internal sawtooth and the pulse width for PFC is determined. Through the average current-mode control loop, the input current $I_S$ is proportional to $I_{MO}$:

$$I_{MO} \times R_2 = I_S \times R_S \quad (4)$$

According to Equation 4, the minimum value of $R_2$ and maximum of $R_S$ can be determined since $I_{MO}$ should not exceed the specified maximum value.

There are different concerns in determining the value of the sense resistor, $R_S$. The value of $R_S$ should be small enough to reduce power consumption, but large enough to maintain the resolution. A current transformer (CT) may be used to improve the efficiency of high power converters.

To achieve good power factor, the voltage for $V_{RMS}$ and $V_{EA}$ should be kept as DC as possible, according to Equation 3. Good RC filtering for $V_{RMS}$ and narrow bandwidth (lower than the line frequency) for voltage loop are suggested for better input current shaping. The transconductance error amplifier has output impedance $R_O$ (>90kΩ) and a capacitor $C_{EA}$ (1µF ~ 10µF) connected to ground (as shown in Figure 5). This establishes a dominant pole *f1* for the voltage loop:

$$f_1 = \frac{1}{2\pi \times R_0 \times C_{EA}} \quad (5)$$

The average total input power can be expressed as:

$$\begin{aligned} Pin &= Vin(rms) \times Iin(rms) \\ &\propto V_{RMS} \times I_{MO} \\ &\propto V_{RMS} \times \frac{I_{AC} \times V_{EA}}{V_{RMS}{}^2} \\ &\propto V_{RMS} \times \frac{\frac{Vin}{R_{AC}} \times V_{EA}}{V_{RMS}{}^2} \propto V_{EA} \end{aligned} \quad (6)$$

From Equation 6, $V_{EA}$, the output of the voltage error amplifier, actually controls the total input power and the power delivered to the load.

## Multi-Vector Error Amplifier

The voltage-loop error amplifier is transconductance, which has high output impedance (> 90kΩ). A capacitor $C_{EA}$ (1µF ~ 10µF) connected from VEA to ground provides a dominant pole for the voltage loop. Although the PFC stage has a low bandwidth voltage loop for better input power factor, the innovative multi-vector error amplifier provides a fast transient response to clamp the overshoot and undershoot of the PFC output voltage.

Figure 5 shows the block diagram of the multi-vector error amplifier. When the variation of the feedback voltage exceeds ± 5% of the reference voltage, the transconductance error amplifier adjusts its output impedance to increase the loop response. If $R_A$ is opened, SG6932 shuts off immediately to prevent extra-high voltage on the output capacitor.

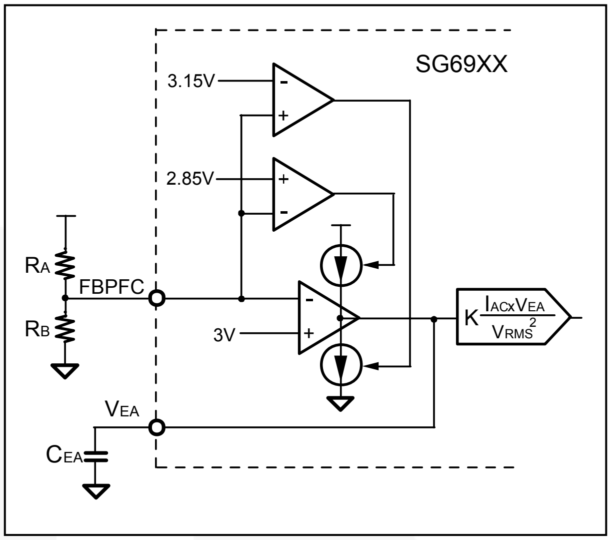



Figure 5. Multi-Vector Error Amplifier

## Cycle-by-Cycle Current Limiting

SG6932 provides cycle-by-cycle current limiting for both PFC and PWM stages. Figure 6 shows the peak current limit for the PFC stage. The PFC gate drive is terminated once the voltage on the ISENSE pin goes below $V_{PK}$.

The voltage of $V_{RMS}$ determines the voltage of $V_{PK}$. The relationship between $V_{PK}$ and $V_{RMS}$ is shown in Figure 6.

The amplitude of the constant current, $I_P$, is determined by the internal current reference, $I_T$, according to the equation:

$$Ip = 2 \times I_T = 2 \times \frac{1.2V}{R_I} \quad (7)$$

Therefore, the peak current of the $I_S$ is given by ($V_{RMS}$<1.05V):

$$Is\_peak = \frac{(Ip \times R_P) - 0.2V}{R_S} \quad (8)$$

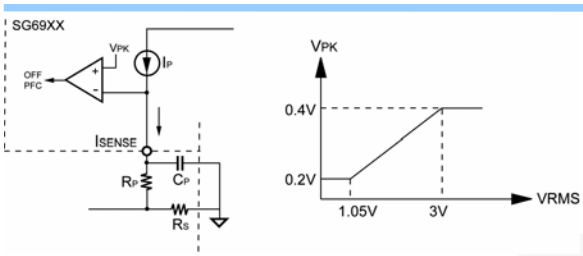



Figure 6. Current Limit

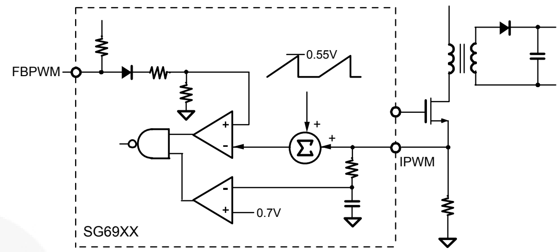



Figure 8. Slope Compensation

## Power-On Sequence / Soft-Start

The SG6932 is enabled whenever the line voltage is higher than the brownout threshold. Once the SG6932 is active, the PFC stage is enabled first. The PWM stage is enabled following a 4ms delay after FBPFC voltage exceeds 2.7V. During start-up of PWM stage, the SS pin charges an external capacitor with a constant-current source. The voltage on FBPWM is clamped by SS during start-up. In the event of a protection condition occurring and/or PWM being disabled, the SS pin is quickly discharged.

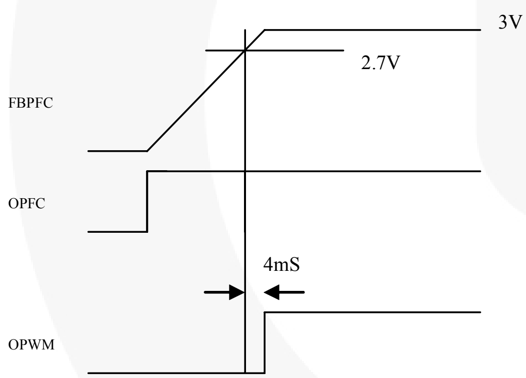



Figure 7. Power-On Sequence

## Forward PWM and Slope Compensation

The PWM stage is designed for forward power converters. Peak current mode control is used to optimize system performance. Slope compensation is added to stabilize the current loop. The SG6932 inserts a synchronized positively sloped ramp at each switching cycle. The positively sloped ramp is represented by the voltage signal $V_{s\text{-}comp}$. In the example in Figure 8, the ramp signal voltage is 0.55V.

## Limited Power Control

Every time the output of power supply is shorted or over loaded, the FBPWM voltage increases. If the FB voltage is higher than a designed threshold, 4.2V, for longer than 95ms, the PWM output is turned off.

## Gate Drivers

SG6932 output stages are fast totem-pole gate drivers. The output driver is clamped by an internal 18V Zener diode to protect the power MOSFET.

## Protections

The SG6932 provides full protection functions to prevent the power supply and the load from being damaged. The protection features include:

*PFC Feedback Over-Voltage Protection.* When the PFC feedback voltage exceeds the over-voltage threshold, the SG6932 inhibits the PFC switching signal. This protection also prevents the PFC power converter from operating abnormally while the FBPFC pin is open.

*Second PFC Over-Voltage Protection (OVP_PFC).* The PFC stage over-voltage input. The comparator disables the PFC output driver if this input exceeds 3.25V. This pin can be connected to the FBPFC pin or the PFC boost output through a divider network. This pin provides an extra input for PFC over-voltage protection.

*PFC Feedback Under-Voltage Protection.* The SG6932 stops the PFC switching signal whenever the PFC feedback voltage drops below the under-voltage threshold. This protection feature is designed to prevent the PFC power converter from experiencing abnormal conditions while the FBPFC pin is shorted to ground.

*$V_{DD}$ Over-Voltage Protection.* The PFC and PWM stages are disabled whenever the $V_{DD}$ voltage exceeds the over-voltage threshold.

*RI Pin Open / Short Protection.* The RI pin is used to set the switching frequency and internal current reference. The PFC and PWM stages of SG6932 are disabled whenever the RI pin is short or open.

## PCB Layout

SG6932 has a single ground pin, which prevents high sink currents in the output being returned separately. Good high-frequency or RF layout practices should be followed. Avoid long PCB traces and component leads. Locate decoupling capacitors near the SG6932. A resistor of 5 ~ 20Ω is recommended, connected in series from the output to the gate of the MOSFET.

Isolating the interference between the PFC and PWM stages is also important. Figure 9 shows an example of the PCB layout. The *ground trace 1* is connected from the ground pin of SG6932 to the decoupling capacitor, which should be low impedance and as short as possible. The *ground trace 2* provides a signal ground. It should be connected directly to the decoupling capacitor $C_{DD}$ and/or to the ground pin of the SG6932. The *ground trace 3* is independently tied from the decoupling capacitor to the PFC output capacitor $C_O$. The ground in the output capacitor $C_O$ is the major ground reference for power switching. To provide a good ground reference and reduce the switching noise of both the PFC and PWM stages, the *ground traces 6 and 7* should be located very near and be low impedance.

The IPFC pin is connected directly to $R_S$ through $R_3$ to improve noise immunity. Do not incorrectly connect to the ground trace 2. The IMP and ISENSE pins should be connected directly via the resistors $R_2$ and $R_P$ to another terminal of $R_S$.

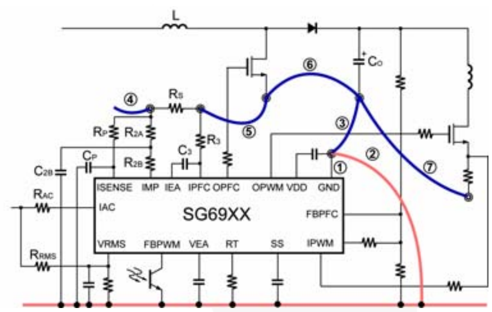
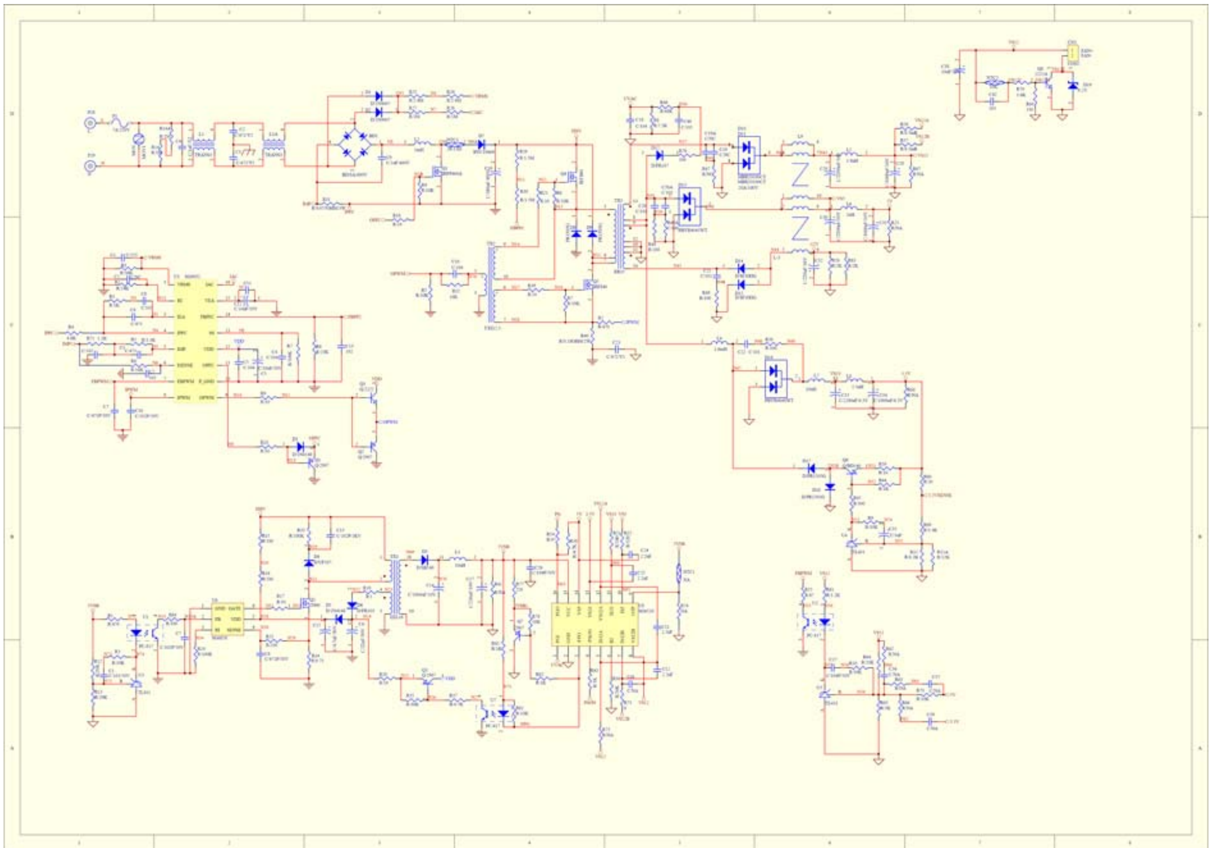


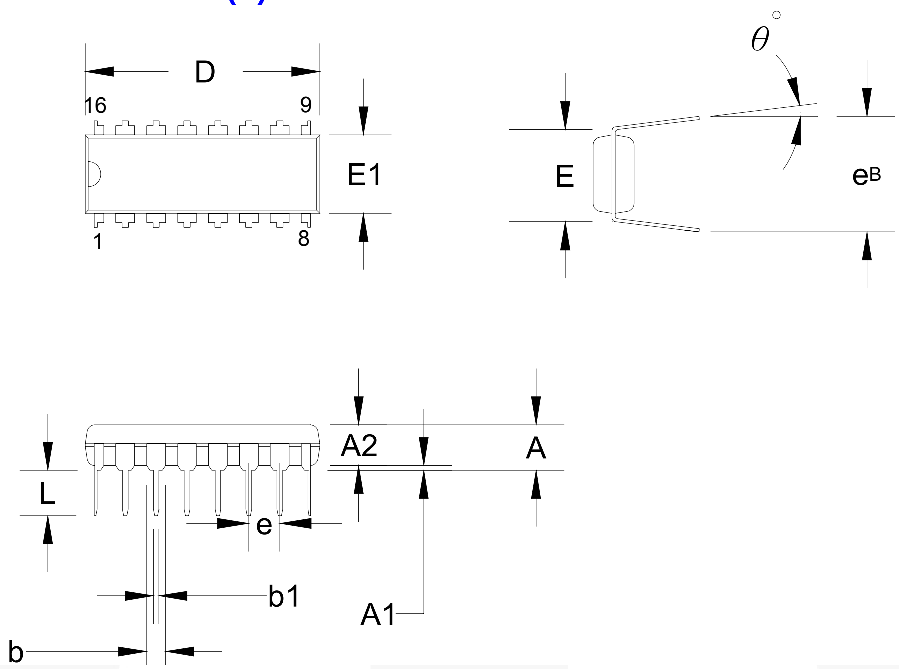

Figure 9. PCB Layout

## REFERENCE CIRCUIT



## PACKAGE INFORMATION

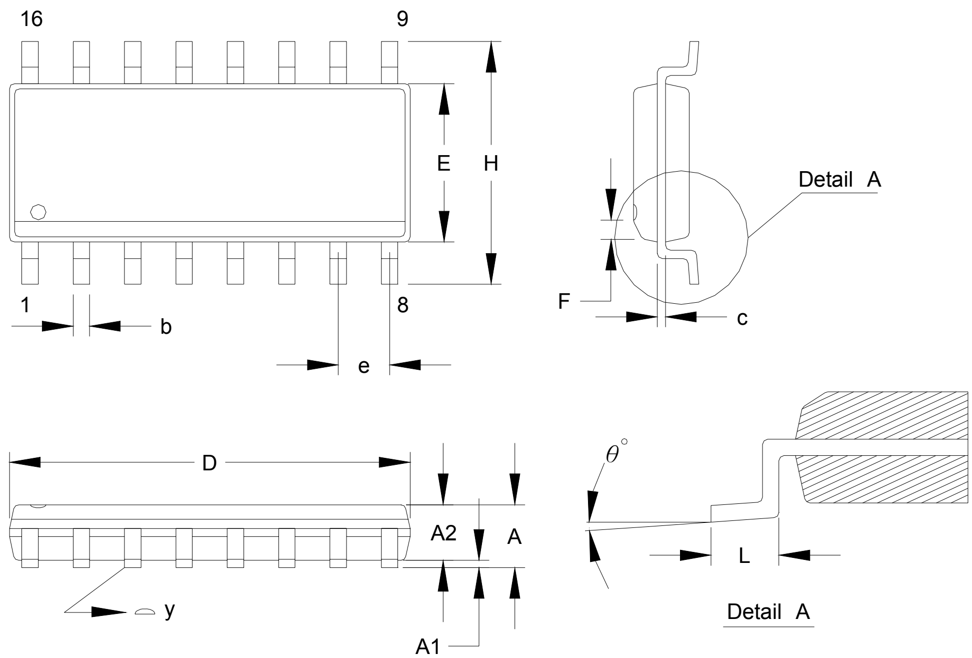
## 16 PINS – PLASTIC DIP (D)




## DIMENSION

| Symbol | Millimeter | | | Inch | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 5.334 | | | 0.210 |
| A1 | 0.381 | | | 0.015 | | |
| A2 | 3.175 | 3.302 | 3.429 | 0.125 | 0.130 | 0.135 |
| b | | 1.524 | | | 0.060 | |
| b1 | | 0.457 | | | 0.018 | |
| D | 18.669 | 19.177 | 19.685 | 0.735 | 0.755 | 0.775 |
| E | | 7.620 | | | 0.300 | |
| E1 | 6.121 | 6.299 | 6.477 | 0.241 | 0.248 | 0.255 |
| e | | 2.540 | | | 0.100 | |
| L | 2.921 | 3.302 | 3.810 | 0.115 | 0.130 | 0.150 |
| $e_B$ | 8.509 | 9.017 | 9.525 | 0.335 | 0.355 | 0.375 |
| $\theta^\circ$ | 0° | 7° | 15° | 0° | 7° | 15° |

## 16 PINS – PLASTIC SOP (S)




## DIMENSION

| Symbol | Millimeter | | | Inch | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 1.346 | | 1.753 | 0.053 | | 0.069 |
| A1 | 0.101 | | 0.254 | 0.004 | | 0.010 |
| A2 | 1.244 | | 1.499 | 0.049 | | 0.059 |
| b | | 0.406 | | | 0.016 | |
| c | | 0.203 | | | 0.008 | |
| D | 9.804 | | 10.008 | 0.386 | | 0.394 |
| E | 3.810 | | 3.988 | 0.150 | | 0.157 |
| e | | 1.270 | | | 0.050 | |
| H | 5.791 | | 6.198 | 0.228 | | 0.244 |
| L | 0.406 | | 1.270 | 0.016 | | 0.050 |
| F | | 0.381X45˚ | | | 0.015X45˚ | |
| y | | | 0.101 | | | 0.004 |
| $\theta$˚ | 0˚ | | 8˚ | 0˚ | | 8˚ |

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Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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|---|---|---|
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