STFI260N6F6

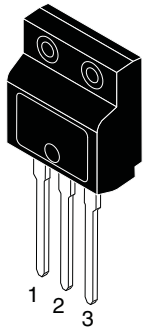
N-channel 60 V, 0.0024 Ω, 80 A STripFET™ VI DeepGATE™ Power MOSFET in I²PAKFP package

Datasheet — preliminary data

Features

Order codes	V_{DSS}	$R_{DS(on)}$ max	I_D
STFI260N6F6	60 V	< 0.003 Ω	80 A

- Fully insulated and low profile package with increased creepage path from pin to heatsink plate
- Low gate charge
- Very low on-resistance
- High avalanche ruggedness

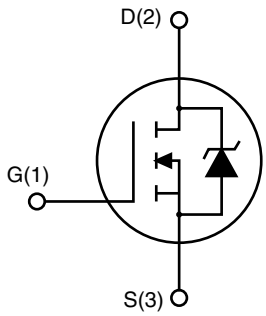


I²PAKFP (TO-281)

Application

- Switching applications

Figure 1. Internal schematic diagram



Description

This device is an N-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STFI260N6F6	260N6F6	I²PAK (TO-281)	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25 °C	80(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	80(1)	A
I_{DM} (1)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25 °C	41.7	W
	Derating factor	0.28	W/°C
T_{stg}	Storage temperature	- 55 to 175	°C
T_j	Operating junction temperature		

1. Current limited by package.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	3.6	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 250 µA	60			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = 60 V V_{DS} = 60 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 60 A		2.4	3	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	11400	-	pF
C_{oss}	Output capacitance			1100		pF
C_{rss}	Reverse transfer capacitance			400		pF
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 120 A, V_{GS} = 10 V *(see Figure 14)*	-	183	-	nC
Q_{gs}	Gate-source charge			53		nC
Q_{gd}	Gate-drain charge			41		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 60 A R_G = 4.7 Ω V_{GS} = 10 V *(see Figure 13)*	-	31.4	-	ns
t_r	Rise time			165		ns
$t_{d(off)}$	Turn-off-delay time		-	144.4	-	ns
t_f	Fall time			62.6		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		120	A
I_{SDM} (1)	Source-drain current (pulsed)		-		480	A
V_{SD} (2)	Forward on voltage	I_{SD} = 120 A, V_{GS} = 0	-		1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 120 A, V_{DD} = 48 V di/dt = 100 A/µs, T_j = 150 °C *(see Figure 15)*	-	55.6 116 3.8		ns nC A

1. Current limited by package.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

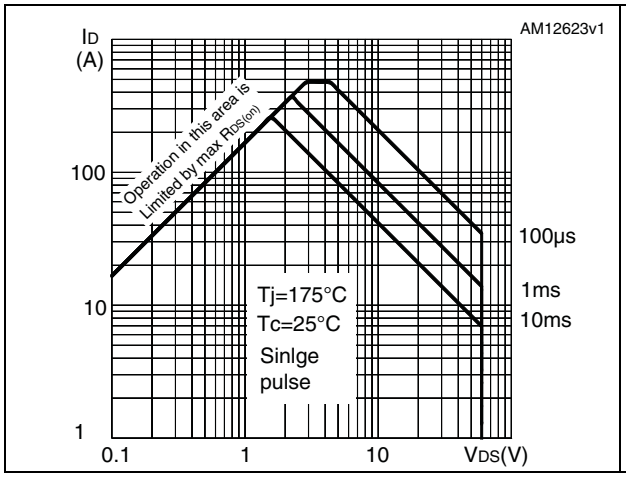


Figure 3. Thermal impedance

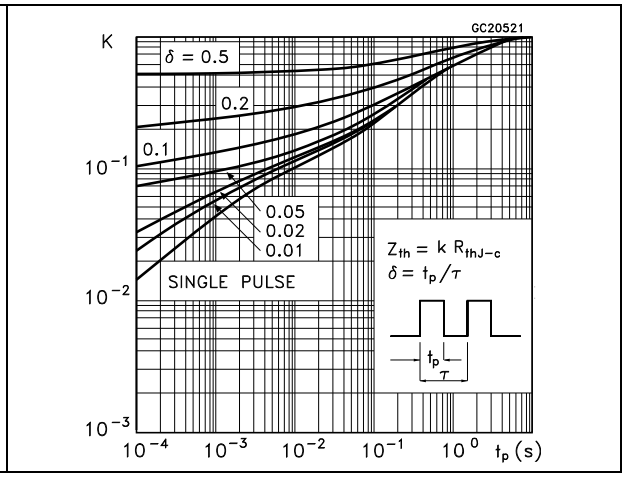


Figure 4. Output characteristics

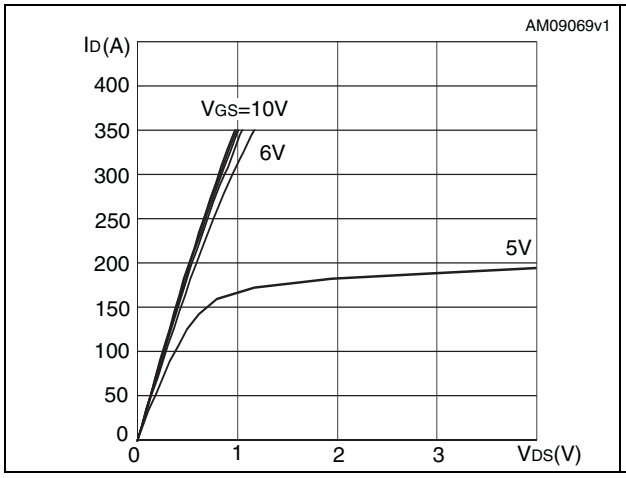


Figure 5. Transfer characteristics

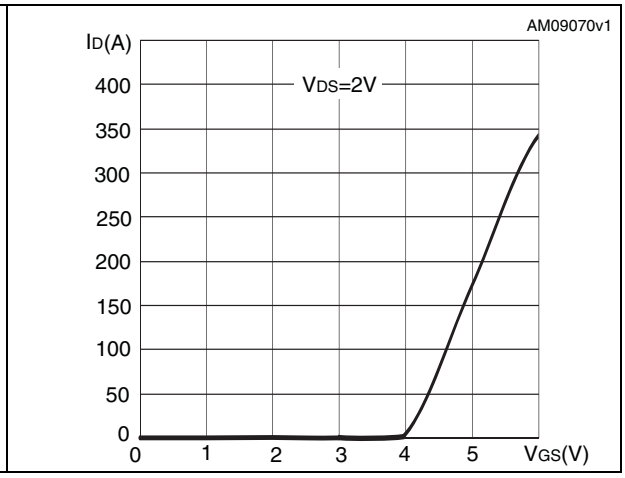


Figure 6. Normalized B_{VDSS} vs. temperature

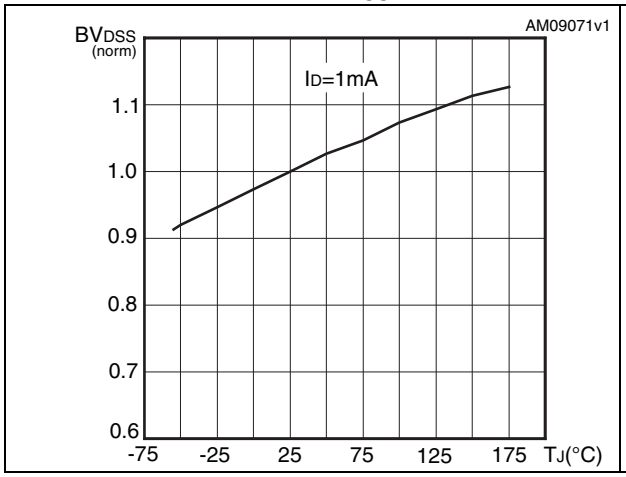


Figure 7. Static drain-source on-resistance

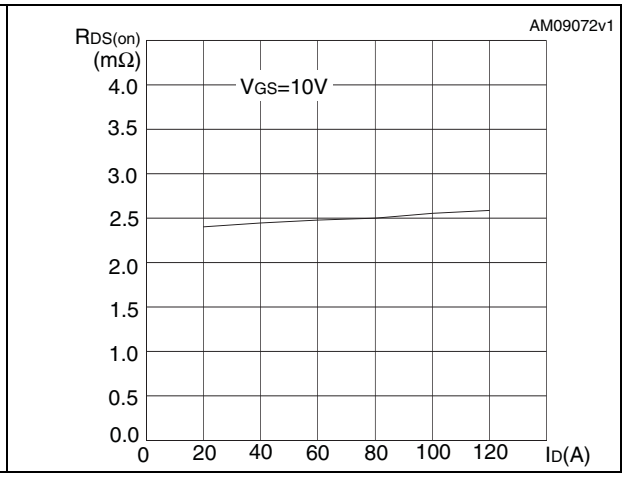


Figure 8. Gate charge vs. gate-source voltage

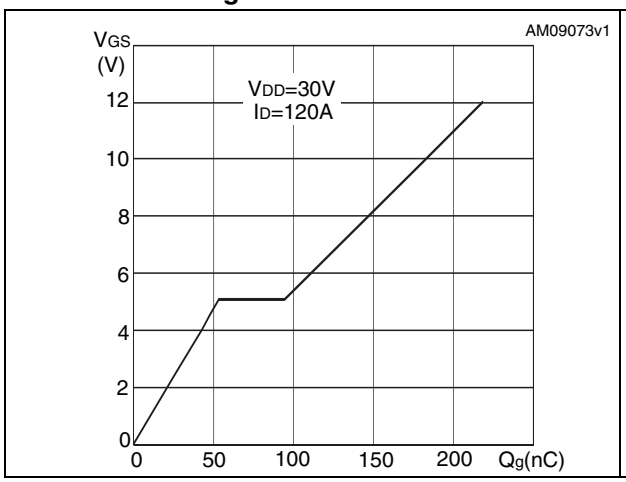


Figure 9. Capacitance variations

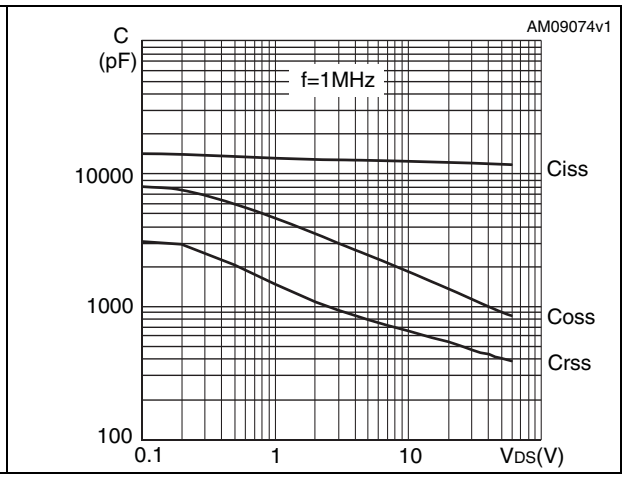


Figure 10. Normalized gate threshold voltage vs. temperature

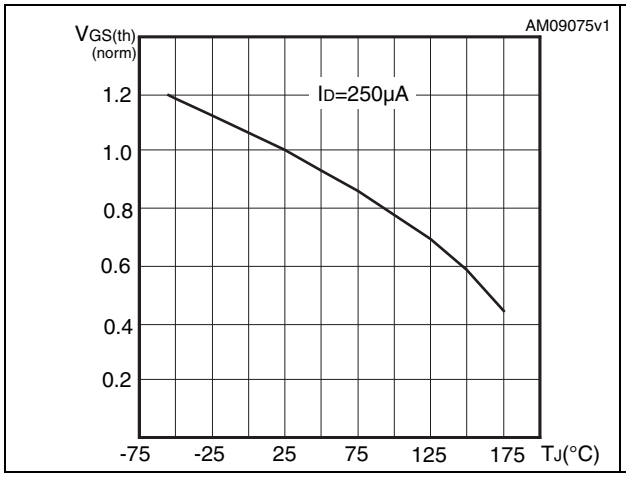


Figure 11. Normalized on-resistance vs. temperature

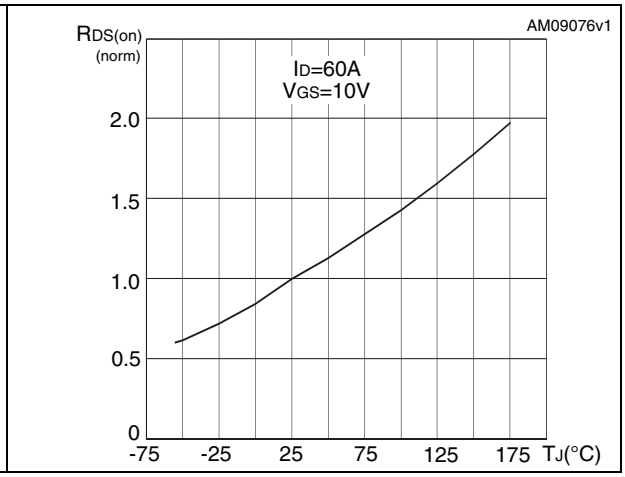
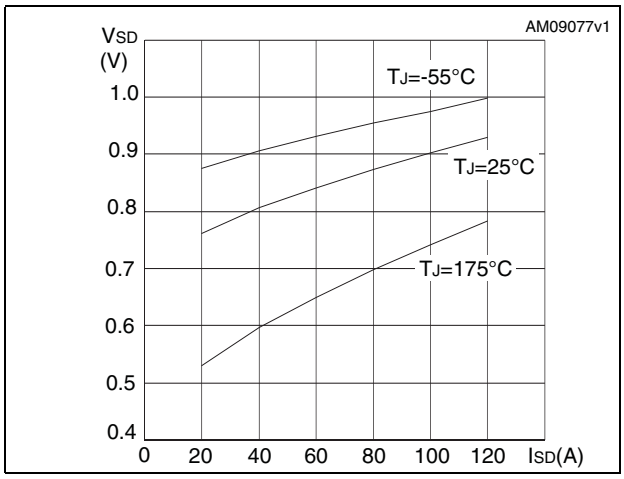


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

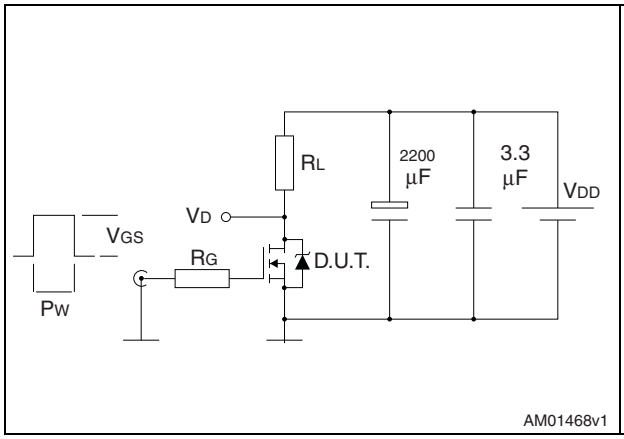


Figure 14. Gate charge test circuit

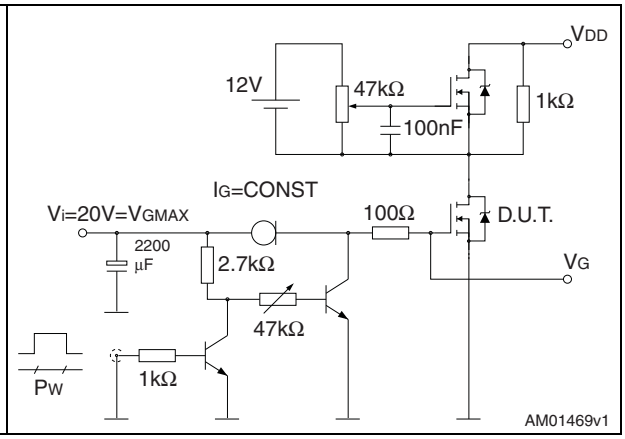


Figure 15. Test circuit for inductive load switching and diode recovery times

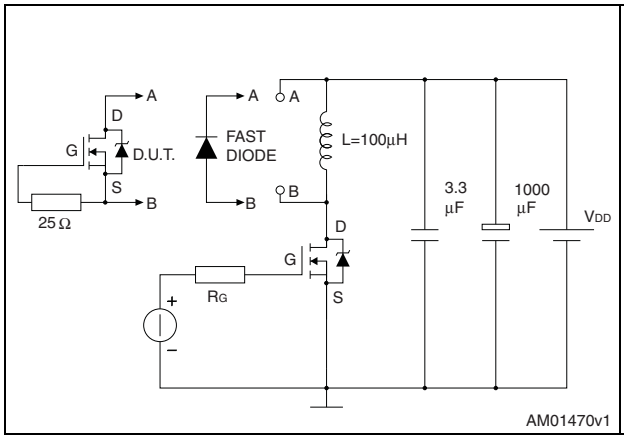


Figure 16. Unclamped inductive load test circuit

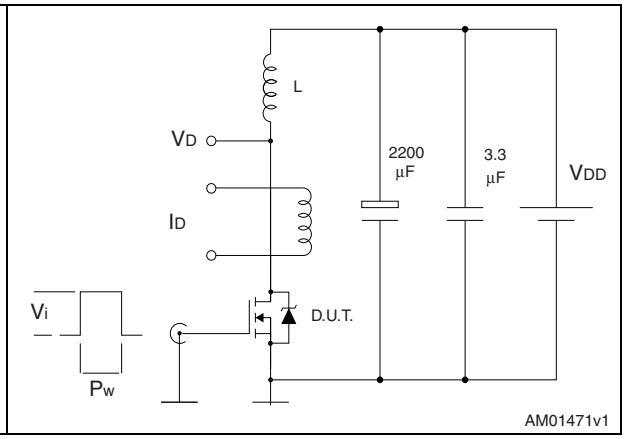


Figure 17. Unclamped inductive waveform

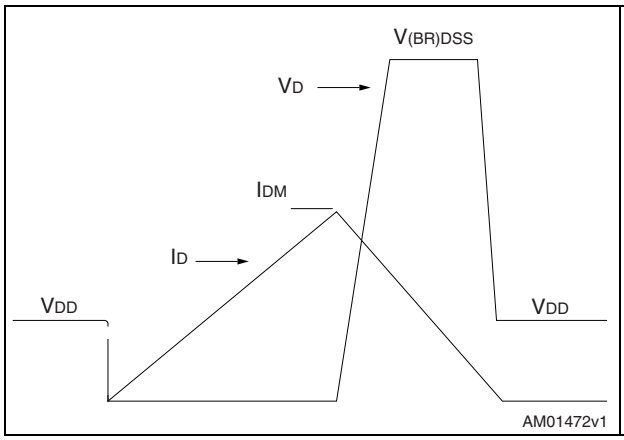
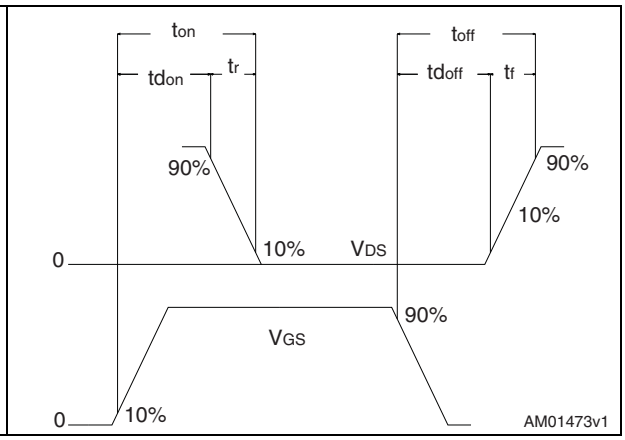


Figure 18. Switching time waveform



4 Package mechanical data

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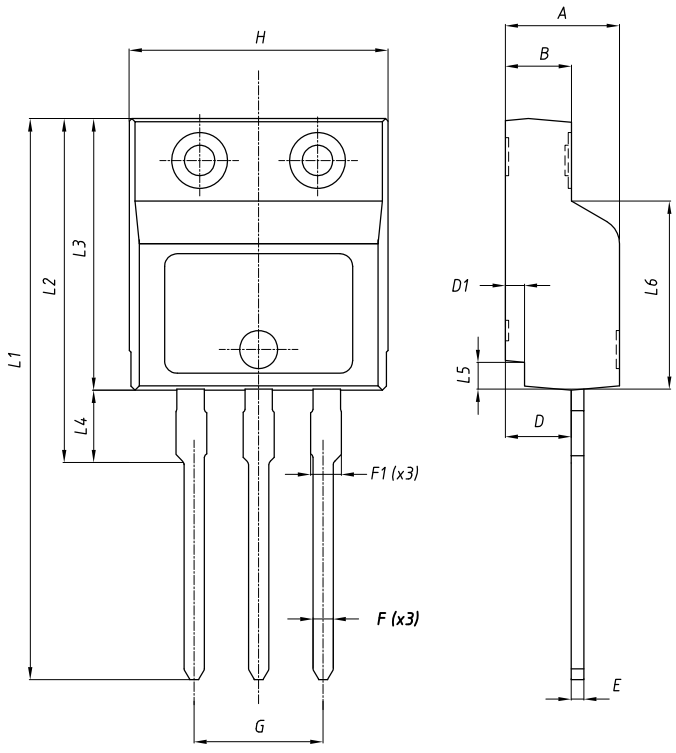
Table 8. I^2PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 19. I^2PAKFP (TO-281) drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
13-Apr-2012	1	First release.

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